	Monday - July 31	Tuesday - Aug 1	Wednesday- Aug 2	Thursday - Aug 3	Friday - Aug 4
9:00am to 10:20am		LaLeh Behjat (Univ. Calgary)	LaLeh Behjat part 2	Evangeline Young (CUHK)	Patrick Groeneveld (formerly Synopsys)
10:20am		coffee break	coffee break	coffee break	coffee break
10:50am to 12:10pm		Mark Lin (NCCU)	Mark Lin part 2	Evangeline Young part 2	Patrick Groeneveld part 2
12:10pm		lunch	lunch	lunch	lunch
1:20pm	Opening				
1:40pm to 3:10pm	William Swartz (TimberWolf/UTDallas)	Ulrich Brenner (Univ. Bonn)	Andrew Kahng - I (UCSD)	Andrew Kahng - II	Ricardo Reis (UFRGS) Marcelo Johann (UFRGS)
3:10pm	coffee break	coffee break	coffee break	coffee break & poster session	coffee break
3:30pm to 4:40pm	William Swartz part 2	Ulrich Brenner part 2	Patrick Madden (SUNY Binghamton)	4:00pm to 5:30pm IEEE Design&Test RoundTable	Patrick Madden part 2
4:40pm to 5:30pm	José Güntzel (UFSC) Renan Netto (UFSC)	André Reis (UFRGS)	Rsyn Team (UFRGS)		4:40pm Closing
5:40pm	pkt show Vinícius Santin and welcome reception		technology interactive music jam session	7:00pm Dinner	

Mon 1:40pm	**William Swartz**	It is all in the details of routing
Tue 9:00am	**Laleh Behjat**	Optimization Methods for CAD Tools
Tue 10:50am	**Mark Lin**	Layout Synthesis for Analog, Mixed-Signal, and RF Integrated Circuits
Tue 1:40pm	**Ulrich Brenner**	Placement and legalization
Wed 1:40pm	**Andrew Kahng - I**	On Evaluation Methodology, Platforms and Standards for PD Research
Thu 1:40pm	**Andrew Kahng - II**	Machine Learning in Physical Design
Wed 3:30pm	**Patrick Madden**	Local Optimization for Physical Design
Thu 9:00am	**Evangeline Young**	Placement and Routing Towards Manufacturability
Fri 9:00am	**Patrick Groeneveld**	Design closure: efficiently meeting relevant constraints in an IC design flow

Mon 4:40pm	**José Güntzel**	Exploiting Flow Conservation Conditions for Effective Timing-Driven Layer Assignment
Mon 5:05pm	**Renan Netto**	Applying Game Development Design Patterns to Physical Design Automation
Tue 4:40pm	**André Reis**	Bringing Technology Information into Early Steps of Logic Synthesis
Wed 4:40pm	**Rsyn Team**	Rsyn - A framework for Physical Design Research and Education
Fri 1:40pm	**Ricardo Reis**	Using Network of Transistors to Reduce Power and to Improve Routing
Fri 2:25pm	**Marcelo Johann**	Discrete Gate Sizing by Lagrangian Relaxation and ISPD Contests