

iberchip

XVI Workshop

Iguaçu Falls, Brazil - February 23-25, 2010



IWS'2010



LASCAS 2010

IEEE Latin American Symposium on
Circuits and Systems
Iguaçu Falls, Brazil - February 24-26, 2010



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Foreword

The Iberchip Workshop (IWS'2010) is back to Brazil. The 16th edition will happen in Iguazu Falls, the border with Argentina and Paraguay. This is a very special place to group the Iberoamerican community in a convergence point of three countries with a wonderful natural scenery. We hope that this privileged location inspire the participants to enlarge the collaborative works within the Iberchip Network. We also desire a very fruitful event, sharing and discussions. Iberchip 2010 is collocated with the first edition of LASCAS, the IEEE Latin American Symposium on Circuits and Systems. This collocation will allow an increase in the international visibility of the work developed in this region. This Iberchip edition is also organized in cooperation with the INCT-NAMITEC (The Brazilian National Institute of Science and Technology dedicated to Micro and Nanoelectronics). The first day of Iberchip will include some special activities organized by NAMITEC. The IBERCHIP Program includes a selection of 69 papers for oral presentation and 35 papers for presentation as posters. These papers came from 10 different countries and they were evaluated by an average of 3.5 reviewers. A special session dedicated to the memory of Tere Osés will occur in the first day of the workshop. We would like to thank all individuals and organizations that helped to make this event possible. Special thanks go to the authors, reviewers and speakers that spent precious time on the preparation of their works and helped to improve the quality of the event.

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Committees

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UFRGS- Universidade Federal do Rio Grande do Sul
UFPel - Universidade Federal de Pelotas

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CAPES

LASCAS

Foreword

The first edition of the IEEE Latin American Symposium on Circuits and Systems takes place in Iguazu Falls, the triple border between Brazil, Argentina and Paraguay. The LASCAS goal is to be the flagship conference of IEEE Circuits and Systems in Latin America. A set of 125 papers with authors from 32 countries were submitted to this first edition. The Program includes a selection of 53 papers for oral presentation and 21 papers presented as posters. A special session dedicated to Biomedical Circuits & Systems happens in the second day of the symposium. The authors of papers come from 25 countries. The symposium also include a Keynote Talk, 2 Invited Talks and 3 Embedded Tutorials. We want to thank all individuals and organizations that helped to set up this first LASCAS, specially the authors, speakers and members of the organizing committee. The organizers invite all of you to keep participating in next LASCAS editions to consolidate the symposium as the international symposium on circuits and systems in Latin America. We wish a very fruitful symposium to all participants.

LASCAS General Chair & Program Chairs

Committees

General Chair:

Ricardo Augusto da Luz Reis, UFRGS, Brazil

Program Chairs:

Antonio Garcia Rozo, Uniandes, Colombia

Eric Kerhervé, IMS, France

Special Sessions Chair:

Maciej Ogorzalek, Jagiellonian Univ., Poland

Tutorials Chair:

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Finance Chair:

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Tuesday

February 23

Iberchip

8:30	IBERCHIP and Namitec Opening	
9:00	Keynote Speaker: Room1	Chair: Sergio Bampi
	Can Fractal Microelectronics Solve Nano-Tera Problems? <i>Maciej Orgozalek, Jagiellonian University, Poland</i>	
10:00	Invited Speaker: Room 1	
	Fabricação de nanoestruturas semicondutoras auto-organizadas e sua aplicação em dispositivos. <i>Patrícia Lustoza de Souza, INCT de Nanodispositivos Semicondutores</i>	
10:30	Invited Speaker: Room 1	
	Eletrônica orgânica. <i>Roberto Mendonça Faria, INCT de Eletrônica Orgânica</i>	
11:00	Coffee Break	
11:20	Round Table Namitec : Microeletrônica: Tendências e Contribuições dos INCT	
	Chair. Raimundo C. S. Freire, UFCG, Brazil	
12:40	Lunch	
14:00	I1: Arithmetic Circuits - Room1 Chair: Sergio Bampi	I2: CAD Tools 1 - Room2 Chair: José Rapallini
	Efficient Pipelined Radix-2m Wallace Multiplier <i>João Altermann, Leandro Zafalon and Eduardo da Costa</i> Somadores Tolerantes a Falhas Usando BSD e Codificação 1 de 3 <i>Helen Franck, José Güntzel, Gustavo Wilke and Ricardo Reis</i> Diseño hardware de un multiplicador de matriz dispersa - vector usando la representación CSR <i>Jorge Eduardo Guerrero Ramirez and Jaime Velasco-Medina</i> Aritmética RNS y caos aplicados para generar números pseudoaleatorios en dispositivos programables <i>Carlos Arturo Gayoso</i> Síntesis Física del Módulo de División de N bits con Segmentación v1.10 <i>Walter Calienes Bartra, Manuel Monge Osorio, Carlos Silva Cárdenas and Ricardo Reis</i>	Migração de Circuitos VLSI 2D para 3D Dirigida a Redução de Interconexões Verticais (TSV) <i>Sandro Sawicki, Marcelo Johann and Ricardo Reis</i> A 3D Symbolic Routing Viewer of Digital Integrated Circuits <i>Erico Nunes and Reginaldo Tavares</i> On Methods for Extraction of Typical Linear Driver Resistance <i>Tiago J. Reimann, Glauco B. V. Santos and Ricardo Reis</i> Estudo do impacto da variabilidade em um conjunto de blocos básicos para composição de leiautes regulares <i>Cristina Meinhardt, Jerson Paulo Guex and Ricardo Reis</i> Estimador de Potência e Atraso em Standard-Cells Utilizando Redes Neurais Artificiais <i>Daniel Guimarães Jr, Ulisses Correa, Luigi Carro and Ricardo Reis</i>
15:40	Poster Session 1 and Coffee Break	
16:30	I4: Video Coding - Room1 Chair: Carlos Silva-Cardenas	I5: CAD Tools 2 - Room2 Chair: Carlos Gayoso
	Controlador DDR SDRAM Multicanal de Alta Velocidade Aplicado à Decodificação H.264/AVC <i>Alexsandro Cristovão Bonatto, André Borin Soares and Altamiro Amadeu Susin</i> Arquitetura em Hardware para a Estimção de Movimento de Blocos de Tamanhos Variáveis do Padrão H.264/AVC <i>Roger Porto, Luciano Agostini and Sergio Bampi</i> An H.264 Deblocking Filter in FPGA with RGB Video Output <i>Vagner Rosa, Leandro Silva and Sergio Bampi</i> Avaliação de Eficiência e Desenvolvimento de Arquiteturas de Calculadores de SSD Segundo o Padrão H.264/AVC <i>Felipe Sampaio, Gustavo Sanchez, Robson Dornelles and Luciano Agostini</i> Desenvolvimento de uma Arquitetura para Interpolação de Half-Pixels segundo o padrão H.264/AVC <i>Marcel Corrêa, Mateus Schoenknecht, Robson Dornelles and Luciano Agostini</i>	Synthesis by Direct Mapping of Asynchronous Controllers from Extended Burst-Mode Specification <i>Duarte Oliveira, Lidia Shibuya and Osamu Saotome</i> A Technique for Accurate Capacitance Ratio Measurements in CMOS Integrated Circuits <i>Antonio Petraglia and Carlos Fernando Teodósio Soares</i> On Structure of the Control Vector for Minimal-Time Circuit Design Process <i>Alexander Zemliak and Miguel Torres</i> Síntese Multiobjetivo de Sistema Composto por Elementos Multifuncionais <i>Adriane Belle, Alice Tokarnia and José R. de Oliveira</i> Influencia de la caracterización en el flujo de diseño de circuitos CMOS nanométricos <i>Gashaw Sassaw Teshome, Carlos Jesús Jiménez Fernández and Manuel Valencia Barrero</i>
18:10	Special Session Dedicated to Tere Osés	Chair: Jordi Aguiló, CNM, Spain
	Acto homenaje en memoria de Tere Osés, la gestora de los PMU y de las licencias, la científica colaborando en el diseño del ILA9200 y en la organización e partición de numerosos cursos de circuitos analogicos, el alma de los primeros Workshops y la incomparable amiga que estuvo siempre junto al grupo Iberchip en sus primeros tiempos.	



Round Table Namitec: Microeletrônica: tendências e contribuições dos INCT

Chair: Raimundo C. S. Freire

Jacobus W. Swart - INCT - NAMITEC

Roberto Mendonca Faria - INCT DE ELETRÔNICA ORGÂNICA

Patricia Lustoza de Souza - INCT DE NANODISPOSITIVOS SEMICONDUTORES

Oscar Manoel Loureiro Malta - INCT DE NANOTECNOLOGIA PARA MARCADORES INTEGRADOS

Marcos Assunção Pimenta - INCT DE NANOMATERIAIS DE CARBONO

14:00 I3: Analog Design 1 Room 3

Chair: Antonio Garcia Rozo

VGA lineales en dB con corriente de control exponencial
PWL

David Moro-Frias, Ma. Teresa Sanz-Pascual, Carlos Aristoteles De la Cruz-Blas and Arturo Sarmiento-Reyes

Design procedure of a linearized OTA based on transconductance, harmonic distortion and mismatch specification

Julio Saldaña-Pumarica and Emilio Del-Moral-Hernandez

Diseño de un OTA de baja transconductancia para el acondicionamiento de señales ECG

Mikel Ormazabal

Módulo multi-função para interface entre fotodetectores e circuitos analógicos condicionadores de sinal

Lester de Abreu Faria, Fabio Durante Pereira Alves and Newton Gomes

Special Session Namitec: Room 4

Chair: Raimundo Freire

RSSF: aplicações e estudos de caso

Linnyer Beatrys

Empacotamento Eletrônico: sua importância, projeto e apresentação de alguns estudos de caso

Márcio Tarozzo Biasoli

Sigma Delta de RF

Nicolas Banlieu and Vincent Bourguet

Switched-Capacitor Integrating ADC with Programmable Input Range

Sebastian Y. C. Catunda

Uma Técnica para a Verificação Experimental do Casamento de Capacitâncias em Arranjos Automáticos de Capacitores Unitários Idênticos

Antonio Petraglia

15:40 Poster Session 1 and Coffee Break

16:30 I6: Analog Design 2 - Room 3

Chair: Jaime Velasco-Medina

Local biasing of negative feedback amplifiers via a graph-theory approach

Arturo Sarmiento Reyes, Miguel Angel Gutierrez de Anda, Luis Hernandez Martinez, Ma. Teresa Sanz and Hector Yair González Ramos

Redes Mobile MOS-NDR Operando con Reloj de una Fase

Juan Nuñez, María J. Avedillo and José M. Quintana

Methodology to Improve the Functional Verification of Analog Mixed Signal Circuits

Jofre Bartnik and Jose Luis Gomez-Cipriano

Analysis and Optimization of a DAR IMPATT Diode for High Frequency Part of Millimetric Region

Alexander Zemliak and Santiago Cabrera

Design Issues and Experimental Characterization of a Continuously-Tuned Adaptive CMOS LNA

Edwin Becerra-Alvarez, Federico Sandoval-Ibarra and Jose M. de la Rosa

Special Session Namitec: Room 4

Chair: Raimundo Freire

Avanços em Hardware para Codificação Avançada de Vídeo Digital

Sergio Bampi e Altamiro Susin

Caracterização de filtros e sensores para radiometria em bandas discretas no infravermelho distante

Pierre Kaufmann

Sensores Químicos para Detecção de Hidrogênio e Acetileno

Sebastião Gomes dos Santos Filho

Circuitos de SAW - blocos para desenvolvimento de Lab-on-Chip

Sergey Balashov

Desenvolvimento de microreatores baseados em carbono nanoestruturado (nanotubos e grafenos)

Stanislav Moshkalev

FRINGE MEETINGS:

Monday, February 22, 3^o Workshop INCT- NAMITEC- 8:30 to 18:00 (open to NAMITEC members)

Tuesday, February 23, 19:10 - IBERCHIP Steering Committee Meeting (open to Iberchip Steering Committee members)

Thursday, February 25, 12:10 - IEEE CASS R9 Chapter Chairs Meeting (open to Chapter Chairs and representatives)

Wednesday

February 24

LASCAS

8:30 **LASCAS Opening Session**

9:00 **Keynote Speaker: Room1**

Chair: Marcelo Johann

Nano-architectures for Tera-scale systems

Keynote Speaker: Giovanni De Micheli - EPFL, Switzerland

10:00 **Coffee Break**

10:30 **L1: C&S Applications - Room 1**

Chair: Raoul Velazco

Digital Control System Using a Thermoelectric Cell for Temperature Electronic Devices Testing

João Bazzo, Jean Carlos Cardozo da Silva, Emerson Geovani Carati, Marcio Vogt and Tiago Lukasiewicz.

A Fuzzy Control for Optimizing the Design of Passive Electrical Circuits

N. Hernández-Romero, P.A. Miranda-Romagnoli and J.C. Seck-Tuoh-Mora.

On Restoring Data Coherence in a GALS System for Medical Imaging

Carlos Leong, João Teixeira, Isabel Teixeira, Pedro Machado, Vasco Bexiga, Ricardo Bugalho, Miguel Ferreira, Pedro Rodrigues, José Silva, João Varela and Pedro Lousã.

Image Interpolation Using Cosine-Sine Modulated Filter Bank

Shusnuke Iwamura, Seisuke Kyochi, Naoto Kaneko and Masaaki Ikehara

Hardware/Software Implementation of an on-line Machine Learning Algorithm

Carlos Quintero, Lorena Garcia, Fernando Lozano and Mauricio Guerrero.

L2: Data Converters - Room 2

Chairs: Andre Mariano

Design of a 12.5 GS/s 5-bit Folding A/D Converter

Antonio Surano and Franco Maloberti.

A Clock-less 8-bit A/D Converter

Sabiniano Araujo Rodrigues, Jose Ivan Carnauba Accioly, Hassan Aboushady, Marie-Minerve Louerat and Raimundo Carlos Silverio Freire.

A noise-insensitive offset calibration technique for time interleaved SAR ADC

Ding Li, Sin Sai Weng, U Seng Pan and Rui Martins

An Area-Efficient Coarse-Fine Resistor-String D/A Converter

Byung-Do Yang, Young-Kyu Shin, Keun-Chul Ryu, Jae-Joong Min, Si-Woo Sung and Jae-Mun Oh

An Architecture for First-Order Tunable Mismatch Shaping in Oversampled Data Converters

Waqas Akram and Earl E. Swartzlander, Jr.

12:10 **Lunch**

14:00 **Embedded Tutorial: Room 1**

Chair: Jorge Juan

3D-CMOS Neuromorphic Imager with Cortical Layer Interconnects

Pedro Julian, UNS, Argentina

15:15 **Poster Session and Coffee Break**

16:15 **L3: Power Electronics - Room 1**

Chair: Pedro Julian

Design Methodology for ZCT and ZCZVT Inverters

Jean Gazzoni, Cristiano Piva, Paulo Ferla, Carlos Stein and Mario Martins

An Energy Based LQR Tuning Approach Applied for Uninterruptible Power Supplies

João Marcos Kanieski, Emerson Giovani Caratti and Rafael Cardoso

A Hardware DC Motor emulator

Vagner Rosa, Vitor Gervini, Sebastiao Gomes and Sergio Bampi.

A Lightweight Mechanism for Dynamic Linking in Wireless Sensor Networks

Carlo Brandolese, Luigi Rucco and William Fornaciari.

A 128 FFT Core Implementation for Multiband Full-Rate

Ultra-Wideband Receivers

Bruno Fernandes and Helena Sarmiento.

L4: RF Amplifiers - Room 2

Chair: Sergio Bampi

A Novel Notch Filter LNA for Use in Multi-Band, Multi-Standard Cellular Receivers

Dirk Bormann, Stefan Kaehlert, Tobias D. Werth and Stefan Heinen.

A Fully Integrated 65 nm CMOS cascode HSFDS PA Dedicated to 802.11n Application

Yohann luque, Eric Kerhervé, Nathalie Deltimple and Didier Belot.

Characterization Methodology of a Millimeter-Wave 65nm

CMOS PA Dedicated to 60GHz WPAN Standard

Sofiane Aloui, Nicolas Delaunay, Eric Kerherve, Nathalie Deltimple, Robert Plana and Didier Belot.

Automatic Design of RF Linear Transconductor

Diomadson Belfort.

Low Voltage High performance Current Mirrors

Prateek Vajpayee, A. Srivastava, S. S. Rajput and G. K. Sharma.

20:30

Conference Dinner

The LASCAS and IBERCHIP Dinner will take place at the Mabu Hotel, including Live Music to listen, to dance.

9:00	Keynote Speaker: Room1		Chair: Marcelo Johann
	<p>Nano-architectures for Tera-scale systems <i>Keynote Speaker: Giovanni De Micheli - EPFL, Switzerland</i></p>		
10:00	Coffee Break		
10:30	I7: Digital Design 1 - Room 3 Chair: Arturo Sarmiento	I8: DSP - Room 4 Chair: Raoul Velazco	
	<p>Procesador para la Emulación de Circuitos Cuánticos basados en Compuertas Toffoli <i>Jorge Duarte-Sanchez, John Michael Espinosa-Duran and Jaime Velasco-Medina</i></p> <p>A General-Purpose Hardware Implementation of a SVM-SMO Algorithm <i>Jonas Gomes Filho, Raul Acosta Hernandez, Marius Strum and Jiang Chau Wang</i></p> <p>Implementation of the JasPer Encoder in a NIOS II Processor <i>Jaime Andres Arteaga-Molina and Jaime Velasco-Medina</i></p> <p>Codiseño Hardware-Software de Sistemas de Control Difusos Sobre FPGAS <i>Santiago Sánchez Solano, María Brox Jiménez, Ernesto del Toro Hernández and Alejandro Cabrera Sarmiento</i></p> <p>A Comparison between Hardware and Software Full Duplex Internet Protocol Version 4 Implementations <i>Lucas Teixeira, Paulo César Comassetto de Aguirre and Crístian Müller</i></p>	<p>Heuristic-Based Algorithms for the Ordering and Partitioning of the Coefficients in FIR Filter Architectures <i>Angelo Luz, Eduardo Costa and Marilton Aguiar</i></p> <p>Architectural Exploration in the Butterflies of the Radix-2 Decimation in Time FFT Algorithm <i>Mateus B. Fonseca, Eduardo A. C. da Costa and João B. dos S. Martins</i></p> <p>Implementation of Split-Radix Fast Fourier Transform on FPGA <i>Cynthia Watanabe, Joel Muñoz and Carlos Silva</i></p> <p>Sistema para el Tratamiento de Interferencia de 60 Hz y Desplazamiento de la línea de Base del ECG Implementado en Plataformas DSP <i>Javier Enrique González Barajas and Jaime Barrero</i></p> <p>Diseño e Implementación de Algoritmos para el Cálculo de la Entropía en DSP para el Estudio Señales Electroencefalográficas <i>Javier Enrique González Barajas, Iván Torres and Andrés Granados</i></p>	
12:10	Lunch		
14:00	Embedded Tutorial: Room 1		Chair: Jorge Juan
	<p>3D-CMOS Neuromorphic Imager with Cortical Layer Interconnects <i>Pedro Julian, UNS, Argentina</i></p>		
15:15	Poster Session and Coffee Break		
16:15	I9: Digital Design 2 - Room 3 Chair: José Luis Güntzel	I10: MEMS and Nanoelectronics Room 4 Chair: Altamiro Susin	
	<p>Circuitos Integrados para la Enseñanza de Electrónica <i>Jose Daza, Antonio Garcia and Lorena Garcia</i></p> <p>Gestión del Diseño de Circuitos/Sistemas Monochip <i>María Isabel Schiavon, Daniel Alberto Crepaldo and Raúl Lisandro Martín</i></p> <p>An Educational NoC-based MP-SoC Reconfigurable Platform Targeted to FPGA Implementation <i>Ivan Saraiva Silva, Tadeu Ferreira de Oliveira and Miklecio Bezerra da Costa</i></p> <p>Implementação e Avaliação de um MPSoC Homogêneo Interconectado por NoC <i>Odair Moreira and Fernando Moraes</i></p> <p>Implementación sobre FPGA de un cliente SNTP usando MicroBlaze <i>Juan Quiros, Julian Viejo, Alejandro Muñoz, Alejandro Millan, Enrique Ostua and J. Ignacio Villar</i></p>	<p>Detección de nanoestructuras con el AFM basado en diapasón de cuarzo <i>Juan Pablo Ruiz, John Alexander Aponte and Alba Avila</i></p> <p>Micromaquinado Superficial con Polisilicio y su Aplicación en Microestructuras Joule <i>Fernando Quiñones Novelo and Wilfrido Calleja-Arriaga</i></p> <p>Energy Harvesting from Low Amplitude Mechanical Vibrations Using a Piezoelectric Transducer <i>Adilson Jair Cardoso and Carlos Galup Montoro</i></p> <p>Desarrollo de un Procedimiento para la Fabricación de Microcanales en PDMS <i>Andres Gaona Barrera, David Olea and Dora Ballesteros</i></p> <p>Concepción y Puesta a Punto de un Micro-Sistema para el Estudio de Estructuras Biológicas Mediante Impedancia Eléctrica <i>Paul Tiburcio and Jordi Aguiló</i></p>	



Thursday

February 25

LASCAS

9:00 **Invited Talk: Room1**

Chair: Eric Kerhervé

Block-Based Transceivers for Wireless Networks

Paulo Diniz - UFRJ, Brazil

10:00 **Coffee Break**

10:30 **Session L5: CAD & FPGAs - Room 1**

Chair: Carlos Silva-Cardenas

An Experimental Study of Interconnection Length in 3D and 2D VLSI

Prasun Ghosal, Hafizur Rahaman and Parthasarathi Dasgupta
Piecewise Linear-based Hybrid Simulation of MOS and Single-Electron Circuits

Arturo Sarmiento, Francisco Javier Castro, Luis Hernández-Martínez and Miguel Angel Gutiérrez.

Optimized Large Size Signed Multipliers and Applications in FPGAs

Shuli Gao, Dhamin Al-Khalili and Noureddine Chabini.

A Parallel Architecture for Ray-Tracing for FPGA Implementation

Alexandre Nery, Nadia Nedjah and Felipe M. G. França.

Implementing and testing the FPGA prototype of a DCM demodulator using the Matlab/Simulink environment

Mário Véstias, Hugo Santos and Helena Sarmento.

L6: DAC & Bio Applications Room 2

Chair: Paulo Diniz

Accurate Multi-bit Feedback DAC Dedicated to High-speed Continuous-time delta-sigma Converters

Andre Mariano, Cédric Majek, Dominique Dallet, Yann Deval and Jean-Baptiste Begueret.

A Short-Channel Silicon-Based Split-Drain MAGFET Measuring from 90 μT

Gerard Santillan, Victos Champac and Roberto Murphy.

How can Electrosurgical Sparks Generate Undesirable Effects?

Bertoldo Schneider Jr., Elton Dias Jr. and Paulo José Abatti.

A Carbon Nanotube Spiking Cortical Neuron with Tunable Refractory Period and Spiking Duration

Jonathan Joshi, Alice C. Parker and Chih-Chieh Hsu.

Selectable Gain Amplifier for Inductive Sensor used to Measure Human Motion

Gustavo Theodoro Laskoski, Sérgio Francisco Pichorim and Paulo José Abatti.

12:10 **Lunch**

14:00 **Embedded Tutorial: Room 1**

Chair: Daniel Lupi

Integrated Systems Security: Hardware-Based Threats and Solutions

Regis Leveugle - TIMA, France

15:15 **Poster Session and Coffee Break**

16:15 **L7: Video - Room1**

Chair: Roberto Murphy

Motion Vector Predictor Architecture for H.264/AVC Main Profile Targeting HDTV 1080p

Franco Valdez, Bruno Zatt, Arnaldo Azevedo, Luciano Agostini and Sergio Bampi.

A MIPS-based ASIP to Accelerate the Inverse Hadamard Transform for H.264/AVC Video Coding

Gracieli Posser, Guilherme Corrêa, Ricardo Reis, Luigi Carro and Sergio Bampi.

Comparative Analysis of Parallel SAD Calculation Hardware Architectures for H.264/AVC Video Coding

Cláudio Diniz, Guilherme Corrêa, Altamiro Susin and Sergio Bampi.

Analysis of the Conditions for Worst Case Switching Activity in Integrated Circuits

Carlos Sampaio, Jose Monteiro and L. Miguel Silveira.

**Special Session: Room 2
Biomedical Circuit & Systems**

organizers: Angel Rodríguez-Vázquez
and Manuel Delgado-Restituto

chair: Angel Rodríguez-Vázquez

Development of a Signal Acquisition Platform for Respiratory Assistance

Antonio García Roza, Diego Méndez Chávez, Lina Peñuela, Jaime Rivera and Jorge Torres

Impact of parasitic capacitances on the performance of SAR ADCs based on capacitive arrays

Alberto Rodríguez-Pérez, José A. Rodríguez, Fernando Medeiro and Manuel Delgado-Restituto

A CMOS QFG ECG amplifier with baseline stabilization

Antonio Lopez-Martin, Jaime Ramirez-Angulo, Ramon G. Carvajal

Design of a versatile voltage based output stage for implantable neural stimulators

Marijn N. van Dongen and Wouter A. Serdijn

18:20: Visit to the ITAIPU DAM with Light Show over the DAM.

This is a unique experience, specially organized to LASCAS and IBERCHIP participants.

The Dam is 8km long.



9:00	Invited Talk: Room1		Chair: Eric Kerhervé
	Block-Based Transceivers for Wireless Networks <i>Paulo Diniz - UFRJ, Brazil</i>		
10:00	Coffee Break		
10:30	I11: Digital Design 3 - Room 3 Chair: Daniel Lupi	I12: NOC and MPSOC - Room 4 Chair: Ivan Saraiva Silva	
	<p>Acelerador em Hardware para Resolução do Despacho de Métodos Polimórficos em Programas Java <i>Tomás Garcia Moreira, Daniel Guimarães Júnior, Marco Aurélio Wehrmeister, Carlos Eduardo Pereira and Ricardo Reis</i></p> <p>Controlador de Processos Dinâmicos a Partir de Modelos Difusos Interpretáveis <i>Luis Murillo and Juan Contreras</i></p> <p>Asynchronous Pipeline Digital Design using FPGA Implementation <i>Duarte Oliveira and Eduardo Lussari</i></p> <p>Revisiting clock-gating: the Common Place for Power Reduction <i>Javier Castro, Pilar Parra and Antonio Acosta</i></p> <p>Synthesis of Low-Power Synchronous Controllers Operating with Local Clock <i>Duarte Oliveira and Luiz Sergio Ferreira</i></p>	<p>Utilizando protótipos virtuais para avaliação do impacto do DMA no desempenho de sistemas MPSoC <i>Marcelo Schuck, Marcio Oyamada and Maxiwell Garcia</i></p> <p>Hierarquia de Memória em MPSoC Baseado em NoC – Implementação e Avaliação <i>Fernando Moraes and Tales Chaves</i></p> <p>A Simulation Methodology for a NoC-Based Dynamically Reconfigurable System <i>Mario Raffo, Wang Jiang Chau and Marius Strum</i></p> <p>An Hybrid Switching Approach for NoC-Based Systems to avoid Denial-of-Service SoC Attacks <i>Martha Johanna Sepulveda, Marius Strum and Wang Jiang</i></p> <p>Desenvolvimento de Aplicação com Requisitos de QoS para SoC baseado em NoC <i>Douglas Melo, Marcelo Berejuck and Cesar Zeferino</i></p>	
12:10	Lunch		
14:00	Embedded Tutorial: Room 1		Chair: Daniel Lupi
	Integrated Systems Security: Hardware-Based Threats and Solutions <i>Regis Leveugle - TIMA, France</i>		
15:15	Poster Session and Coffee Break		
16:15	I13: FPGA Based Design - Room 3 Chair: María Isabel Schiavon	I14: Wireless and Cryptography - Room 4 Chair: Jorge Juan	
	<p>Implementações em FPGA do Protocolo de Sincronização e Codificação de Canal de Telemetria Recomendado pelo CCSDS <i>Fábio B. Armelin and Roberto d'Amore</i></p> <p>A Reed-Solomon CODEC for OTN G.709 Standard with Reduced Decoder FPGA Area <i>Tiago Barbosa, Robson Moreno and Tales Pimenta.</i></p> <p>An FPGA Implementation of a Kernel Function for Support Vector Machines <i>Jonas Gomes Filho, Raul Acosta Hernandez, Marius Strum and Jiang Chau Wang</i></p> <p>FPGA implementation: A multiple-stage converter control for a pulsed current source <i>Nicolas Wassinger, Rogelio Garcia Retegui, Marcos Funes and Mario Benedetti</i></p> <p>Estocasticidad de un atractor caótico determinista implementado en FPGA <i>Luciana De Micco, Omar G. Zabaleta, Claudio M. Gonzalez, Constancio M. Arizmendi and Hilda Angela Larrondo</i></p>	<p>TLM and VHDL-AMS Co-Simulation of a System on Chip for Wireless Sensor Networks <i>Gilmar S. Beserra, Juan F. Eusse, João V. B. Pimentel, Arthur M. Sampaio, Ricardo P. Jacobi and José C. da Costa</i></p> <p>Sistema de medida en ambientes industriales basado en redes de sensores inalámbricos <i>Alfonso González, Natacha Leone, Mauricio Murdoch, Pablo Maz-zara and Julián Oreggioni</i></p> <p>Diseño en Hardware para los cifradores de flujo Grain-128, Mickey-128, Decim-128 y Trivium <i>Juan Manuel Marmolejo, Vladimir Trujillo-Olaya and Jaime Velasco-Medina</i></p> <p>Hardware Architectures for Inversion in GF(2m) <i>Vladimir Trujillo-Olaya and Jaime Velasco-Medina.</i></p>	

The departure from the Mabu Hotel will be at 18:20 (sharp), by shuttle. The visit to Itaipu will finish at 21:15. From there a shuttle will go to a Barbacue Restaurant. Or if you prefer, the shuttle will bring you back to the conference hotel. The participants that want to do the visit will have to sign a list at the conference registration desk including the ID Number (Passport or National ID for Brazilians).



9:00 **Keynote Speaker: Room1**

chair: Sergio Bampi

Ultra-low power logic circuits: From voltage-mode to current-mode

Massimo Alioto - University of Siena, Italy

10:00 **Coffee Break**

10:30 **L8: Hot Topics - Room 1**

Chair: Arturo Sarmiento

Stepped Triangular CIC Decimation Filter for SDR Applications

Gordana Jovanovic Dolecek and Alfonso Fernandez- Vazquez.

On the Normalized Minimum Error-Entropy Adaptive Algorithm: Cost Function and Update Recursion

Wallace Martins, Paulo Diniz and Yih-Fang Huang.

Cross-Layer Constrained Power Management: Application to a Multimedia Mobile Platform

William Fornaciari, Patrick Bellasi, David Siorpaes, Stefano Bosisio and Matteo Carnevali.

Delay Sensing for Parametric Variations and Defects Monitoring in Safety-Critical Applications

Júlio Vazquez, Victor Champac, Adriel Ziesemer Jr., Ricardo Reis, Isabel Teixeira, Marcelino Santos and Paulo Teixeira

Traffic Modeling and Analysis of PLC Networks using Markov Chains

Christiane Borges Santos, Flávio Henrique Teles Vieira, Sergio Granato de Araújo, Fabio da Silva Marques, João Batista José Pereira, Flavio Geraldo C. Rocha and Dominique Carvalho Fernandes.

L9: Analog Circuits - Room 2

Chair: Antonio Acosta

Design of a high-sensitivity sub-40ug capacitive accelerometer using a Multi-Project Wafer process

André Keller Abadie and Roberto d'Amore.

A Simple Approach for the Design of Operational Transconductance Amplifiers for Low Power Signal Processing

Alfonso Chacón-Rodríguez, Santiago Sondon, Pablo Mandolesi and Pedro Julián.

Offset-Compensated Comparator with Full-Input Range in 150nm FDSOI CMOS-3D Technology

Manuel Suarez, Victor Brea, Carlos Domínguez, Ricardo Carmona, Gustavo Liñán and Angel Rodríguez Vázquez.

A New Readout Circuit for Infrared Imaging Sensors

Gholamreza Akbarzadeh and Gholam Ali Rezai-rad.

Practical Considerations for the Design of Fully Differential OTAs with SC-CMFB

Carlos Bula and Manuel Jimenez.

12:10 **Lunch**

14:00 **Embedded Tutorial: Room 1**

Chair: Gustavo Wilke

Modeling Interconnect and Design-in Passives for Efficient Coupled Analysis

Luis Miguel Silveira - INESC-ID, Portugal

15:15 **Poster Session and Coffee Break**

15:45 **L10: Modeling & Simulation - Room1**

Chair: Luis Miguel Silveira

Cache Alternatives Concerning Cache Coherence in NoC-based MPSoC Platform

Ivan Saraiva Silva, Bruno Cruz de Oliveira and Gustavo Girão.

Grayscale CNN Computation of Boolean Functions

Eero Lehtonen, Jussi Poikonen, Jonne Poikonen and Mika Laiho.

A Study on the Propagation Times of Loaded CMOS Inverters

Sergio Vale Pires, Manuel Dionisio Rolo, Ernesto Ventura Martins and Luis Nero Alves.

Multi-Threaded Circuit Simulation using OpenMP

Mark Zwolinski

A Modified Izhikevich Model For Circuit Implementation of Spiking Neural Networks

Arash Ahmadi and Mark Zwolinski.

L11: Critical Circuits - Room 2

Chair: Luciano Agostini

Impact of Compilation Options on the Criticality of Registers in a Microprocessor-based System

Salma Bergaoui and Regis Leveugle.

A New Automated Instrumentation for Emulation-based Fault Injection

Regis Leveugle and Adrien Prost-Boucle.

Performance Evaluation of Hybrid ANN Based Time Series Prediction on Embedded Processor

Rafael Trapani Possignolo and Omar Hamammi.

Design and Simulation of a Unit Cell for a QWIP-FPA

Lester de Abreu Faria, Fabio Durante Pereira Alves and Newton Gomes.

17:25 **Closing**

LASCAS 2011
Colombia - February 22-25, 2011

ISCAS 2011
Rio de Janeiro, May 15-18, 2011

Posters IBERCHIP

Poster Session Tuesday

February 23th

IP-Core para Compressão Sem Perdas de Sinais Biológicos (DEMO)
Daniel Soares e Marques, Yuri Gonzaga Gonçalves da Costa, Bruno Maia de Moraes, João Janduy Brasileiro Primo, Igor Gadelha Pereira, Lucas Lucena Gambarra, José Antônio Gomes de Lima, Antônio Carlos Cavalcanti and Leonardo Vidal Batista

Implementación en Hardware de Algoritmos Para Efectos de Audio Usando FPGAs
Pedro Pablo Lievano-Torres, John Michael Espinosa-Duran and Jaime Velasco-Medina

Reconocimiento de Voz Aplicando Mapas Auto-Organizativos
Matias Namiot, Laura Lanzarini, José A. Rapallini and Antonio A Quijano

Uso de DSP para Análisis de Ruidos en Señales de Baja Frecuencia
Julián Marchueta, José A. Rapallini and Antonio A. Quijano

Implementação de microcontrolador 8051 reconfigurável em FPGA
Remy Eskinazi, Onesimo Ximenes and João Paulo

Parallel Communication Architecture based on Microcontrollers for P-Systems Simulation
Abraham Gutierrez and Jesus Bobadilla

Implementação de uma Unidade de Ponto Flutuante para uma Arquitetura Reconfigurável
Mateus Silva, Bruno Hecktheuer, Julio Mattos, Antonio Beck Filho, Mateus Rutzig and Luigi Carro

Propuesta didáctica para la enseñanza de arquitecturas de procesadores con lógica programable
José A. Rapallini, Héctor Hugo Mazzeo, Walter Aroztegui and Antonio A. Quijano

Projeto de uma FPU considerando Área, Frequência e Potência
Gracieli Posser, Ricardo Reis and Sergio Bampi

Ferramenta ASTRAN: para Geração Automática de Circuitos VLSI
Felipe Nesello, Charles Leonhardt, Adriel Ziesemer and Ricardo Reis

Paralelização do Posicionador PlaceDL através de primitivas OpenMP
Lucas Cavalheiro, Felipe Pinto and Ricardo Reis

Roteamento detalhado usando Pathfinder e A*
Charles Leonhardt, Felipe Nesello, Adriel Ziesemer and Ricardo Reis

Poster Session Wednesday

February 24th

Metodología orientada a la elección de FPGAs con prioridad en el consumo de potencia
Jose Miguel Mora Gutierrez, Gashaw Sassaw Teshome, Carlos Jesús Jiménez Fernández and Manuel Valencia Barrero

Energy-Aware System Level Evaluation Method for Coarse-grained Hybrid VLIW Architectures
Gustavo Adolfo Cerezo Vásquez and Wilhelmus A. M. van Noije

Diseño de un Criptoprocador RSA de 8192 bits usando un Multiplicador Sistólico
Claudia Patricia Renteria, Vladimir Trujillo-Olaya and Jaime Velasco-Medina

Implementação de uma Unidade em Ponto Flutuante para Operações Aritméticas em FPGA
Iuri Castro, Raphael Neves, Alessandro Girardi, Jeferson Marques, Edson Schlosser, Dion Lenon Prediger and Sidinei Ghissoni

Especificação em LOTOS de requisitos de QoS para Redes-em-Chip
Dayanne K. F. Rocha, Karla D. N. Ramos and Claudia M. F. Araujo Ribeiro

Verificação Funcional Aplicada a Redes-em-Chip
Pablo Pires and Cesar Zeferino

A Multi-parent Genetic Algorithm for Searching for the Pair of Inputs that Cause the Maximum Number of Switching Gates in a Combinational Circuit
Norimasa Yamada and Alberto Palacios Pawlovsky

Diseño de una Estación de Bombeo Controlada por Computadora para la Caracterización de Estructuras Microfluídicas
Houari Cobas Gomez, Marcio Rodrigues da Cunha, Izabela Dutra Alvim, José E. Eirez Izquierdo, Sonnia Pavoni Oliver and Mario R Gongora-Rubio

Estudo e Simulação de um Acelerômetro MEMS
Carolina Metzler, Ricardo Reis and Gilson Wirth

Diseño de un Microsistema usando FPGAs para Medir el Área de una Lamina de Cuero
Johann Fabian Salazar and Jaime Velasco-Medina

Chip para el análisis de parámetros sanguíneos
Matias Namiot, Alejandro Mut, José A. Rapallini and Antonio A Quijano

Poster Session Thursday

February 25th

Circuito de Polarización con independencia de Tensión de Alimentación y cancelación parcial del efecto de la temperatura
Pablo Petrashin, Walter Lancioni, Luis Toledo and Carlos Vazquez

Sistema de Monitoramento de Qualidade de Energia Elétrica em Baixa Tensão
Carlos Eduardo Fusinato Magnani, Carlos Eduardo Maffini Santos, Ivan Jorge Chueiri and Valter Klein Jr.

Corrector del Factor de Potencia de Desplazamiento para Instalaciones Eléctricas de Baja Tensión
Enrique Montoya Suarez

System of quality monitoring and faults in the network of secondary power lines
Valter Klein Jr., Ivan Jorge Chueiri, Carlos Eduardo Fusinato Magnani and Carlos Eduardo Maffini Santos

Estado del arte de las redes de sensores inalámbricos (wsn)
Federico Fernández and Juan Carlos Fabero

Neuronal and Programmable Circuit with Floating-Gate Transistor Multiple Input Four Bits
Alejandro Medina Santiago and Mario Alfredo Reyes Barranca

Using statistical simulations for improving IIP2 in direct conversion receivers
Antonio Felipe Freitas Silva, Fernando Sousa and Sebastian Catunda

Poster Session Wednesday

February 25th

Implementação de um Multiplicador Sobre GF(2⁴) Utilizando Portas de Limiar Linear
Cristóvão Filho, Alan Sá, Karolie Nobre, Raimundo Freire and Francisco Marcos

Diseño de una Arquitectura para la Solución de la Ecuación de Schrödinger usando el Método de Numerov
Victor Alfonso Rodriguez-Toro, Fabio Noguera-Leon and Jaime Velasco-Medina

Dispositivo Electrónico para la Medición de Variables Biomédicas Correlacionadas en la Inferencia de Estrés
Antonio Garcia and Juan David Fonseca

A Mixed-Signal Interface for Low-Cost Sensors in Battery-Operated Multi-sensor Systems
Alberto Bayo, Nicolás Medrano, Belén Calvo, Santiago Celma, María Teresa Sanz and Arturo Sarmiento

Desarrollo de un Dispositivo Inalámbrico para la Estimación del Gasto Energético por Actividad Física Mediante Acelerometría
Daniel Lupi, Sergio Gwirc, Diego Brengi, Fernando Marsilli and Christian Huy

Posters LASCAS

Poster Session Wednesday

February 24th

All-Pass Filter Employing Fully Balanced Voltage Differencing Buffered Amplifier
Dalibor Bialek, Viera Biolkova and Zdenek Kolka.

Incorporating Effects of Process, Voltage, and Temperature Variation in BTI Model for Circuit Design
Shreyas Kumar Krishnappa, Harwinder Singh and Hamid Mahmoodi.

Ultra Low-Power Super Class AB CMOS OTA Cells with Rail-to-Rail Operation
Mahdi Ahangarian Abhari, adib Abrishamifar and Seyed Javad Azhari.

A Framework for Circuit-Level Analog Synthesis With an Educational Approach
Tiago Oliveira Weber and Cesar Ramos Rodrigues.

Differential Continuous-Time Delta Sigma Modulator using the FGMOS Transistor
Jesus de la Cruz and Noe Oliva.

Design of Hardware Accelerators for Demanding Applications
Lech Jozwiak and Yahya Jan

An efficient technique to design linear-phase decimation filters
David Ernesto Troncoso Romero and Gordana Jovanovic Dolecek.

Formula Simplification using Two-Graph Method
Zdenek Kolka, Martin Vlk, Dalibor Bialek, Viera Biolkova and Josef Dobes

Poster Session Thursday

February 25th

Impact of different power reduction techniques at architectural level on modern FPGAs
Henryk Błasiński, Frederic Amiel and Thomas Ea

Master-Slave Flip-flop Optimization for fine-grained clock-gating Applications
Javier Castro, Pilar Parra and Antonio Acosta.

A new architecture for a FM modulator based on time-varying eigenvalues
Miguel Angel Gutierrez de Anda, Arturo Sarmiento Reyes and Alfonso Prieto Guerrero.

NOTIFY: a Network-On-chip-based Tool to Inject Faults extensively
Hananeh Aliee and Hamid R. Zarandi.

Source-Level Energy Estimation and Optimization of Embedded Software
Carlo Brandolese, William Fornaciari and Daniele Scarpazza

A Fuzzy Model for Network Traffic Prediction Using Orthonormal Basis Functions Based on Multifractal Characteristics
Flávio H. T. Vieira, Flávio G. C. Rocha, Scheila G. Garcez and Christiane B. Santos

ASIC Implementation of a Parser Module for a Minimalist H.264 Video Decoder
Leandro Silva, Fabio Pereira and Sergio Bampi.

A Comparison of Steady-State Procedures Based on Epsilon-Algorithm and Sensitivity Analysis
Josef Dobes, David Cerny, Viera Biolkova and Zdenek Kolka.

Time-Stamp of Digital Audio Recording Based on the ENF Estimated from Another Audio Signal
Isabela Apolinario and Carlos Rossi.

Evaluating the Efficiency of Software-only Techniques to Detect SEU and SET in Microprocessors
José Rodrigo Azambuja, Fernando Sousa, Lucas Rosa and Fernanda Lima Kastensmidt.

High Efficiency Reference Frames Storage for H.264/AVC Decoder Hardware Implementation
Alexsandro C. Bonatto, Andre B. Soares and Altamiro A. Susin.

A Study on Clock Mesh Size Selection
Guilherme Flach, Gustavo Wilke, Marcelo Johann and Ricardo Reis.

Cascade dynamic current calibration: A new scheme for implementation of highly accurate current memories
Jaime Ramirez-Angulo, Enrique Lopez-Morillo, Ramon G. Carvajal and Antonio J. Lopez-Martin.

Iberchip and LASCAS

Program at Glance

Tuesday: February 23th		Wednesday: February 24th		Thursday: February 25th		Friday: February 26th	
8:30 - 9:00	IBERCHIP and Namitec Opening	8:30 - 9:00	LASCAS Opening	9:00 - 10:00	Invited Speaker: Paulo Diniz	9:00 - 10:00	Invited Speaker: Massimo Alioto
9:00 - 10:00	Keynote Speaker: Maciel Orgozalek	9:00 - 10:00	Keynote Speaker: Giovanni De Micheli	10:00 - 10:30	Coffee Break	10:00 - 10:30	Coffee Break
10:00 - 10:30	Invited Speaker: Patricia Lustoza de Souza	10:30 - 12:10	Session 1 LASCAS	10:30 - 12:10	Session 2 LASCAS	10:30 - 12:10	Session 8 LASCAS
10:30 - 11:00	Invited Speaker: Roberto Mendonça Faria	10:30 - 12:10	Session 2 IBERCHIP	10:30 - 12:10	Session 3 LASCAS	10:30 - 12:10	Session 9 LASCAS
11:00 - 11:20	Coffee-break	12:10 - 14:00	Lunch	12:10 - 14:00	Lunch	12:10 - 14:00	Lunch
11:20 - 12:10	Round Table Namitec Microeletrônica: Tendências e Contribuições dos INCT	14:00 - 15:15	Embedded Tutorial 1 Pedro Julian	14:00 - 15:15	Embedded Tutorial 2 Régis Leuвеugle	14:00 - 15:15	Embedded Tutorial 3 Luis Miguel Silveira
12:40 - 14:00	Lunch	15:15 - 16:15	Poster Session and Coffee Break	15:15 - 16:15	Poster Session and Coffee Break	15:15 - 15:45	Coffee Break
14:00 - 15:15	Session 1 IBERCHIP	16:15 - 17:55	Session 3 LASCAS	16:15 - 17:55	Session 4 LASCAS	16:15 - 17:55	Session 10 LASCAS
14:00 - 15:15	Session 2 IBERCHIP	16:15 - 17:55	Session 4 IBERCHIP	16:15 - 17:55	Session 5 IBERCHIP	16:15 - 17:55	Session 11 LASCAS
15:40 - 16:30	Poster Session and Coffee Break	20:30	Conference Dinner	20:30	Special Session and Coffee Break	20:30	Closing
16:30 - 18:10	Session 4 IBERCHIP				Special Session Biomedical C&S	17:55	
18:10 - 19:10	Special Session dedicated to Teres Oses				Session 6 LASCAS		
					Session 7 LASCAS		
					Session 8 IBERCHIP		
					Session 9 IBERCHIP		
					Session 10 IBERCHIP		
					Session 11 IBERCHIP		
					Session 12 IBERCHIP		
					Session 13 IBERCHIP		
					Session 14 IBERCHIP		