Transistor Network Restructuring Against NBTI Degradation

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Abstract

Negative Bias Temperature Instability (NBTI) has become a critical reliability concern for nanometer PMOS transistors. A logic function can be designed by alternative transistor networks. This work evaluates the impact of the NBTI effect in the delay of CMOS gates considering both the effect of intra cell pull-up structures and the effect of decomposing the function into multiple stages. Intra cell pull-up PMOS transistor arrangements have been restructured to minimize the number of devices under severe NBTI degradation. Also, circuits decomposed into more than one stage have been compared to their single stage design version. Electrical simulation results reveal that the restructuring of intra-cell transistor networks recovers up to 15% of rise delay degradation due to NBTI, while the decomposition of single stage circuit topologies into multi-stage topologies tends to reduce the rise degradation delay at a cost of fall delay degradation.

1. Introduction

CMOS technology has been permanently scaling down during the last decades. Several aspects ignored in earlier technology nodes, such as leakage currents, variability and aging effects, are becoming critical concerns in nanoscaled design [1-5]. In particular, Negative Bias Temperature Instability (NBTI) has received an increased interest [6-12]. It refers to the generation of positive oxide charge and interface traps in metal-oxide-silicon structure under negative gate voltage bias ($V_{gs} = -V_{dd}$), in particular at elevated temperature. PMOS transistors are mostly affected, since these devices are negatively biased when they are conducting. The NBTI effect increases the PMOS transistor threshold voltage (V_{th}) over time, reducing the device drive current and circuit speed [13].

Several logic functions can be designed using different kinds of transistor networks [14]. These variations can be achieved by using different logic styles or by restructuring the transistor arrangements. For instance, Fig. 1 shows two versions of traditional CMOS AOI21 gates with restructured PMOS pull-up plane. The logic functions can also be decomposed into multiple stages, as the NAND3 gate depicted in Fig. 2. It is well known that these different approaches present different behaviours in terms of area, speed and power consumption. They also present different levels of degradation due to NBTI.

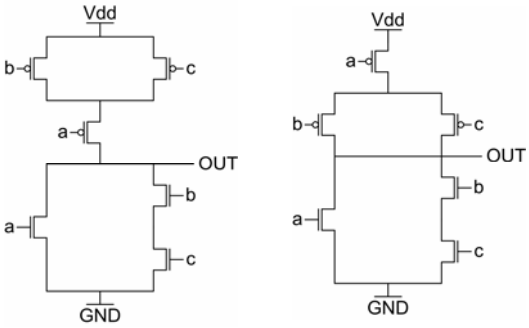
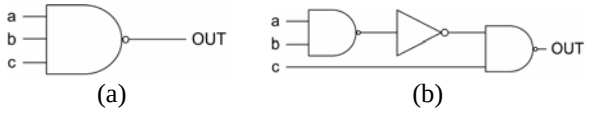


Fig. 1. Two logically equivalent AOI21 CMOS gates.

In order to achieve a robust design, different solutions to mitigate NBTI degradation have been proposed in the literature [6-10]. At circuit level, some techniques insert additional modules to explore the NBTI supply and threshold voltage dependence [7], while other ones explore the NBTI input signal dependence by reordering the gate inputs [6,9,10]. At gate level, there are techniques that add a time slack margin to compensate NBTI degradation upsizing the transistors width [8]. The proposed work evaluates the NBTI degradation at both circuit and gate levels, through a previously unexplored focus. At gate level, the transistor arrangement restructuring in the PMOS pull-up plane is investigated. At circuit level, NBTI effect is evaluated in circuits decomposed into more than one stage. Electrical simulations are performed to evaluate the proposed techniques.



(a) (b)

Fig. 2. NAND3: (a) single gate and (b) multi-stage circuit.

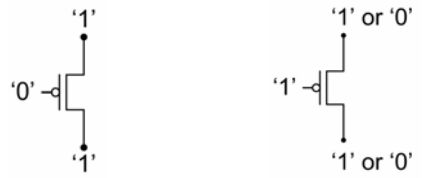
This paper is organized as follows. Section 2 presents a brief review of important points about NBTI effect, giving an overview of related works and outlining the contribution of proposed approaches. Section 3 illustrates the used methodology and Section 4 presents the obtained simulation results and analysis. Finally, the conclusions are discussed in Section 5.

2. Background and Contributions

The NBTI degradation is proportional to the temperature, power supply voltage, threshold voltage and to the probability that PMOS transistor is negative biasing. It occurs when the device presents the gate terminal in the logic value '0' and the source terminal in the logic value '1'. This probability defines the period that a PMOS device stays in the stress and recovery phases. Fig. 3 illustrates both stress and recovery PMOS transistor biasing, and Fig. 4 depicts the V_{th} variation during different bias conditions. A lower signal probability means a longer recovery time and a smaller V_{th} degradation due to the NBTI effect.

When a transistor stack is considered, as observed in AOI21 gates in Fig. 1, the steady state of the intermediate node determines whether each individual device is under negative bias stress [6]. It means that the signal probability of each PMOS transistor in a stack cannot be considered individually, but have to be associated to the probability of the other devices in the stack. PMOS transistors that are connected to the power supply (V_{dd}) suffer more V_{th} degradation due to NBTI than the ones that are not connected directly to V_{dd}. Fig. 5 shows the time under degradation (%) of a four transistor stack when all gate inputs have a signal probability of 0.5.

Several design techniques to mitigate NBTI effects are reported in the literature [6-10]. The tuning of V_{dd} and V_{th} are effective techniques to compensate the performance degradation due to NBTI, since it is exponentially dependent of these parameters [7]. Gate sizing is another technique proposed to deal with performance uncertainties. Sufficient design margin to compensate NBTI degradation can be set before fabrication by oversizing the gate properly [8]. The signal probability and the position of the device in a transistor stack are explored in several ways. Pin reordering is used to reduce NBTI degradation when the circuit is in active mode [6]. Input vector is explored in order to minimize static degradation when the circuit is in standby state [9]. Functional symmetries are explored in order to manipulate the stress probability by logic restructuring to reduce the NBTI effects in circuit critical paths [10].



(a) (b)

Fig. 3. NBTI transistor biasing: (a) stress and (b) recovery.

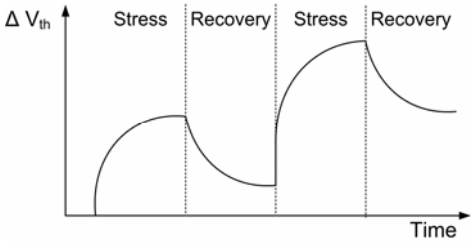


Fig. 4. Threshol voltage (V_{th}) variation during different PMOS transistor bias conditions.

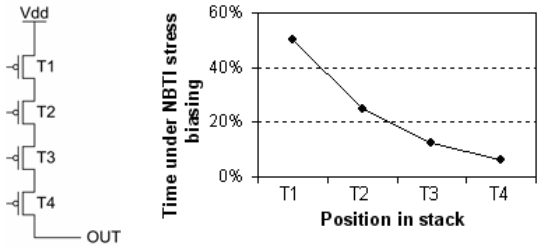


Fig. 5. Time under stress biasing versus position in a four transistor stack.

This work evaluates the delay degradation due to NBTI effect in two approaches. The first analysis explores the transistor arrangement restructuring in the PMOS pull-up plane to compare the robustness of CMOS gates in terms of the NBTI effect. This analysis considers both signal probability and position of the transistor in the network. The second analysis explores the speed degradation due to NBTI effect when circuits decomposed into more than one stage are compared to their single stage design version.

3. Methodology

The long term NBTI prediction model proposed in [11] is used to estimate the V_{th} degradation due to this effect for a given time 't' and a signal probability 'α' as described in following:

$$\Delta V_{th} = b \cdot \alpha^{n} \cdot t^{n} \qquad (1)$$

where $b = 3.9 \cdot 10^{-3}\ V \cdot s^{-1/6}$ and '*n*' is the time exponential constant and equals to *0.16*.

The threshold voltage degradation has been estimated over 10 years and for several signal probabilities using the 45nm CMOS PTM process [15]. The stress probabilities for the devices have been computed considering equal signal probability of 0.5 for all primary inputs, and the particular position of each device in the transistor stack. In logic functions designed as circuits decomposed into multiple stages, each internal circuit node also considers its previous logic gate function probability.

Electrical characterization has been executed for different design versions of logic functions, considering fanout 4 delay (nominal and degraded delay).

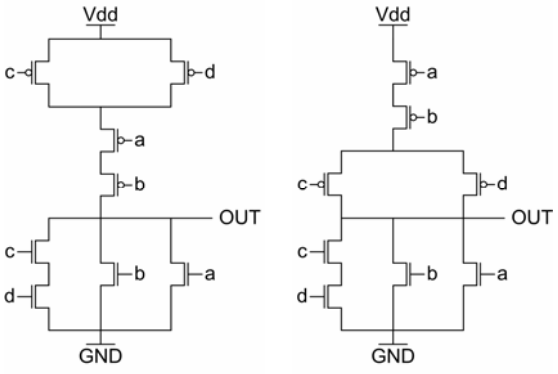
4. Simulation Results and Analysis

4.1. Transistor Network Restructuring

As mentioned previously, a logic function can be designed using different transistor networks. Fig. 1 illustrates two different pull-up PMOS designs for the AOI21 logic gate. These solutions present naturally different delay and power consumption behaviours. They also suffer different levels of degradation due to NBTI. In this section, the pull-up PMOS transistor arrangement is restructured to explore the NBTI degradation dependence.

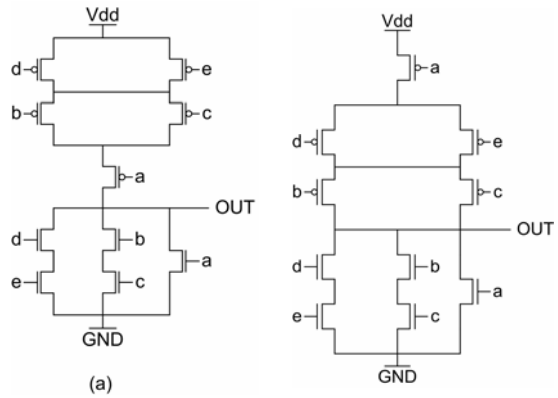
Assuming all gate inputs with equal signal probability (50%), PMOS transistors that are connected to the power supply (V_{dd}) suffer more V_{th} degradation than the ones which are not connected directly to V_{dd}, as shown in Fig. 5. Based on the previous statement, a more robust CMOS gate design, with respect to NBTI degradation, may connect as few as possible transistors to the power supply.

In the pull-up arrangement of the AOI21, AOI211, and AOI221 gates illustrated in Fig. 1(a), Fig. 6(a) and Fig. 7(a), respectively, two transistors are submitted to severe NBTI degradation since they are directly connected to V_{dd}. On the other hand, the topologies in Fig. 1(b), Fig. 6(b) and Fig. 7(b), present just one transistor connected to V_{dd} and consequently only this device suffers significant degradation. Fig. 8 illustrates two versions of a typical circuit used in carry lookahead adder unit, named here CLAunit. According to previous analysis, the gate depicted in Fig. 8(a) has more transistors close to V_{dd}, and so suffers higher NBTI degradation than the one shown in Fig. 8(b).



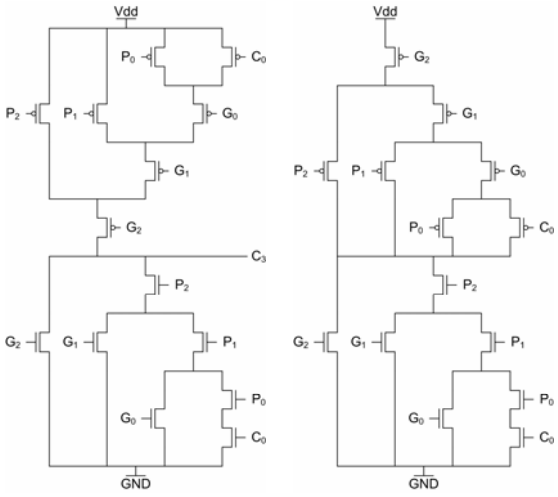
(a) (b)

Fig. 6. Two logically equivalent AOI211 CMOS gates.



(a) (b)

Fig. 7. Two logically equivalent AOI221 CMOS gates.



(a) (b)

Fig. 8. Two logically equivalent 'CLAunit' gates.

Table 1 presents the degradation on the average rise

propagation delay through gates depicted in Fig. 1, Fig. 6, Fig. 7 and Fig. 8 due to NBTI effect. The degradation recovered due to transistor arrangement restructuring is also presented. The results show that up to 15% of the NBTI speed degradation can be recovered by transistor arrangement restructuring.

Table 1
Average rise delay degradation in gates depicted in Fig. 1, 6, 7, and 8.

Gate	Average Rise Delay Degradation (%)	Average Rise Degradation Recovered (%)
AOI21 (a)	8,69	10,74
AOI21 (b)	7,76	
AOI211 (a)	8,95	15,04
AOI211 (b)	7,60	
AOI221 (a)	8,66	5,61
AOI221 (b)	8,17	
CarryOut (a)	9,13	13,97
CarryOut (b)	7,85	

4.2. Single gate versus multiple stage circuit

Table 2 shows the average delay degradation of NAND3, NOR3, AOI21, AOI211 and AOI221 gates designed as a circuit decomposed into multiple stage compared to their single stage version. The chosen single stage versions are the ones that have presented less delay degradation in previous section. The decomposed version of NAND3 referred by Table 2 is depicted in Fig. 2(b), and the decomposed version of NOR3 follows the same structure changing the NAND2 gates by NOR2 gates. The decomposed versions of AOI21, AOI211 and AOI221 are shown in Fig. 9, Fig. 10 and Fig. 11. In these figures, the difference between (b) and (c) versions is the input connections ordering on the NOR3 gate in the last stage. The up connection in the NOR3 symbol represents the one connected to the transistor closer to V_{dd}.

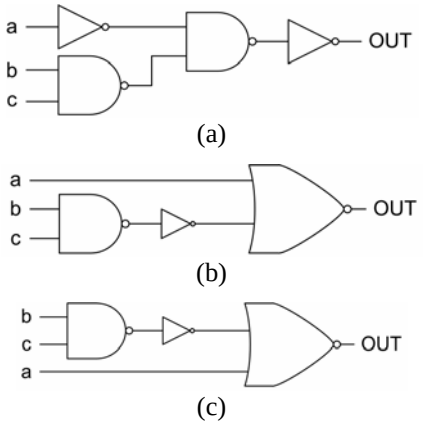


Fig. 9. AOI21 decomposed versions.

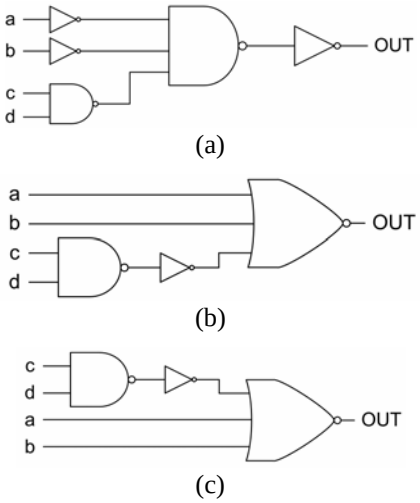
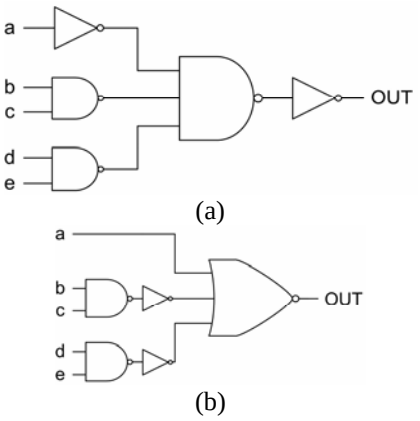
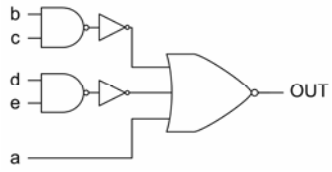


Fig. 10. AOI211 decomposed versions.

The ‘CLAunit’ circuit, depicted in Fig. 8, is also evaluated and the results are also presented in Table 2. In this analysis, two decomposed versions are evaluated. These versions are illustrated in Fig. 12. A decomposed three gate level version is depicted in Fig. 12(a), while Fig. 12(b) illustrates a decomposed seven gate level version that instantiates logic gates with just two inputs.

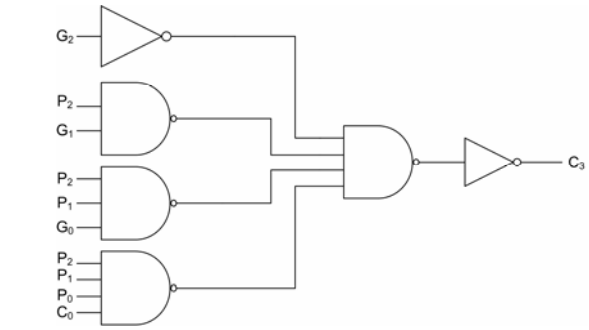
The NBTI effect just degrades the threshold voltage of PMOS transistors. Therefore, as verified in Section 4.1, the rise delay is increased in single stage design approaches. The results presented in Table 2 show that the decomposed versions present degradation in both rise and fall delay. In these multiple stage designs, the rise delay degradation may not be as severe as in single stages at the penalty of fall delay degradation. It can be explained since the fall output transition depends on at least one rise transition at an intermediate node, which is defined by a pull-up network composed by PMOS transistors.



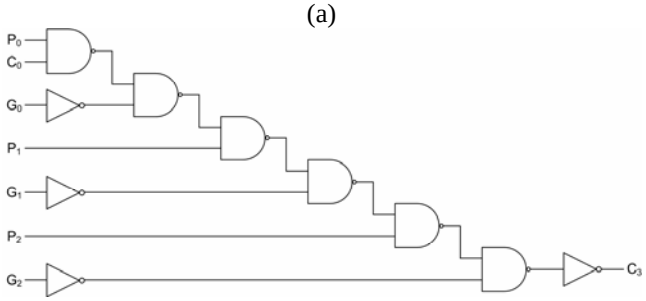


(c)

Fig. 11. AOI221 decomposed versions.



(a)



(b)

Fig. 12. 'CLAunit' decomposed versions.

In single stage CMOS gates, the logic paths responsible for the fall output transition are composed solely by NMOS transistors and should not be affected by NBTI. However, this single stage designs may even present a small improvement in fall delay. It is caused by the weakening of PMOS transistors current, reducing the influence of the pull-up network during the output fall transition.

Table 2
Average delay degradation of logic functions designed as a single CMOS gate and as a decomposed circuit in multiple stages of basic logic gates.

Logic Function		Rise delay degradation (%)	Fall delay degradation (%)
NAND3	Single gate	7,63	0,00
	Decomposed version	7,65	1,22
NOR3	Single gate	8,11	-0,18
	Decomposed version	6,28	1,35
AOI21	Single gate	7,76	-0,08
	Decomposed version (a)	6,23	2,12
	Decomposed version (b)	7,76	1,38
	Decomposed version (c)	7,90	1,10
AOI211	Single gate	7,60	-0,26
	Decomposed version (a)	5,33	2,81
	Decomposed version (b)	8,08	0,76
	Decomposed version (c)	8,48	0,59
AOI221	Single gate	8,17	-0,36
	Decomposed version (a)	5,39	2,60
	Decomposed version (b)	8,10	1,13
	Decomposed version (c)	8,59	1,02
C3	Single gate	7,85	-0,31
	Decomposed version (a)	5,59	2,35
	Decomposed version (b)	5,98	2,89

5. Conclusions

Several design solutions that can be used to represent a certain logic function are explored considering the influence in terms of the NBTI speed degradation. The results show that the transistor arrangement restructuring is a potential design solution to recover the delay degradation due to NBTI effect. This technique can be used combined with other ones already proposed in the literature to achieve better results. The use of logic functions decomposed into more than one stage can also be a solution to reduce the rise delay degradation at a cost of fall delay degradation.

Acknowledgements

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