MIC05: Teste de Circuitos Integrados

Marcelo Lubaszewski

PPGMicro - UFRGS

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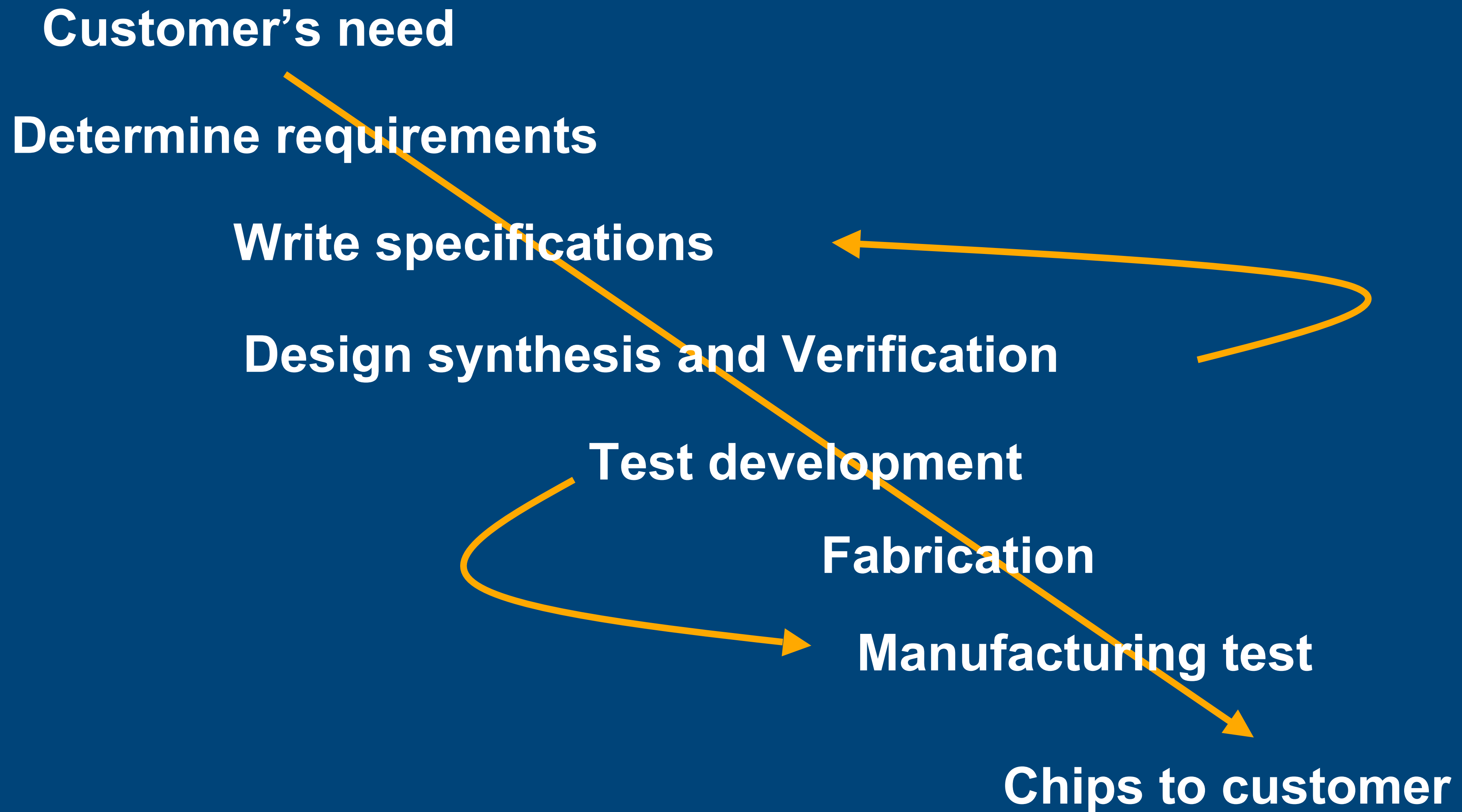
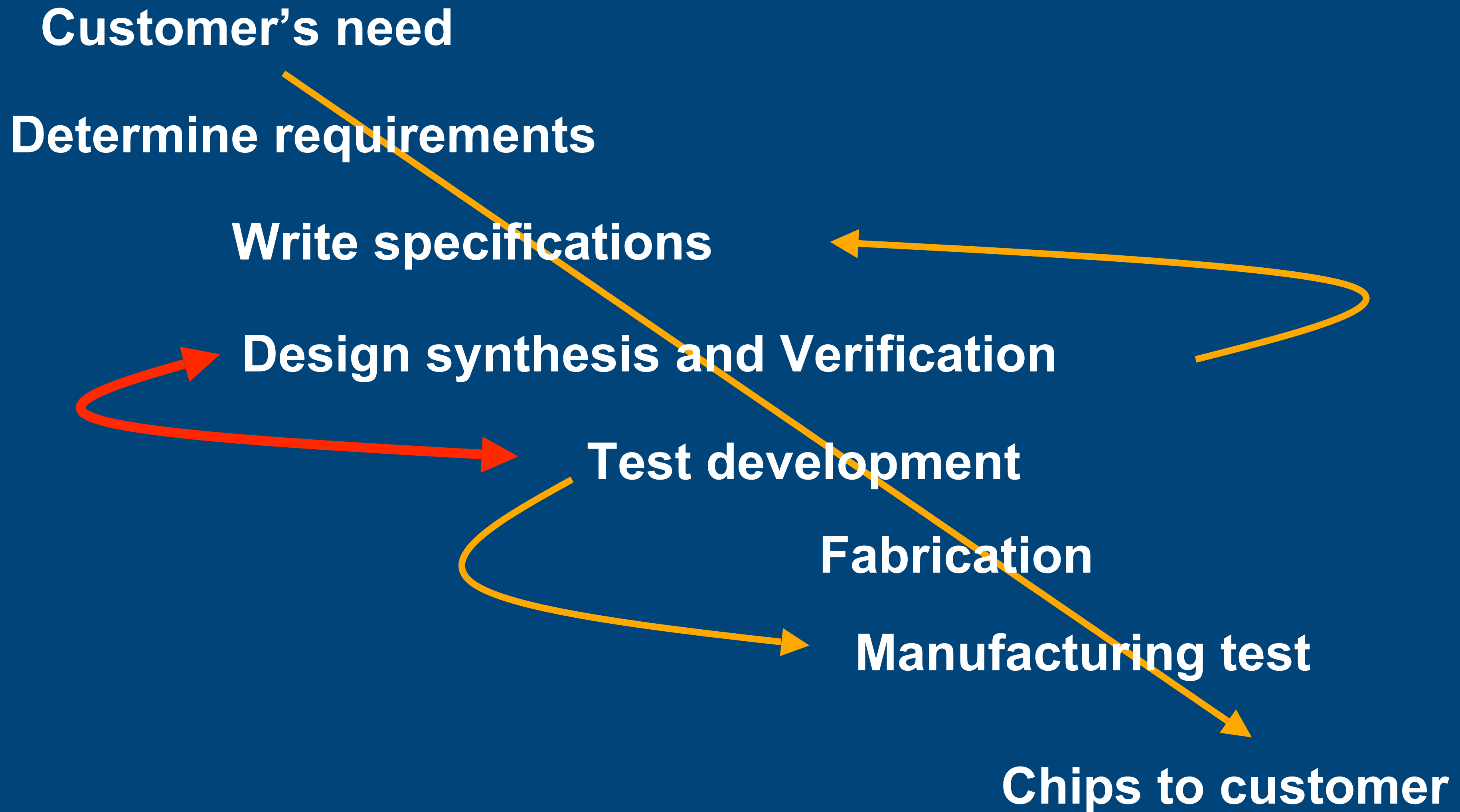
Lecture 1- Introduction

- VLSI realization process
- Verification and test
- Ideal and real tests
- Roles of testing
- Types of Testing
- Costs of testing
- Test Economics

VLSI Realization Process



VLSI Realization Process



Definitions

- Design synthesis
  - Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- Verification:
  - Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.
- Test:
  - A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

Verification vs. Test

- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

- Verifies correctness of manufactured hardware.
- Two-part process:
  1. Test generation: software process executed once during design
  2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.

Problems of Ideal Tests

- Ideal tests detect all defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.
- Very large numbers and varieties of possible defects need to be tested.
- Difficult to generate tests for some real defects. *Defect-oriented testing is an open problem.*

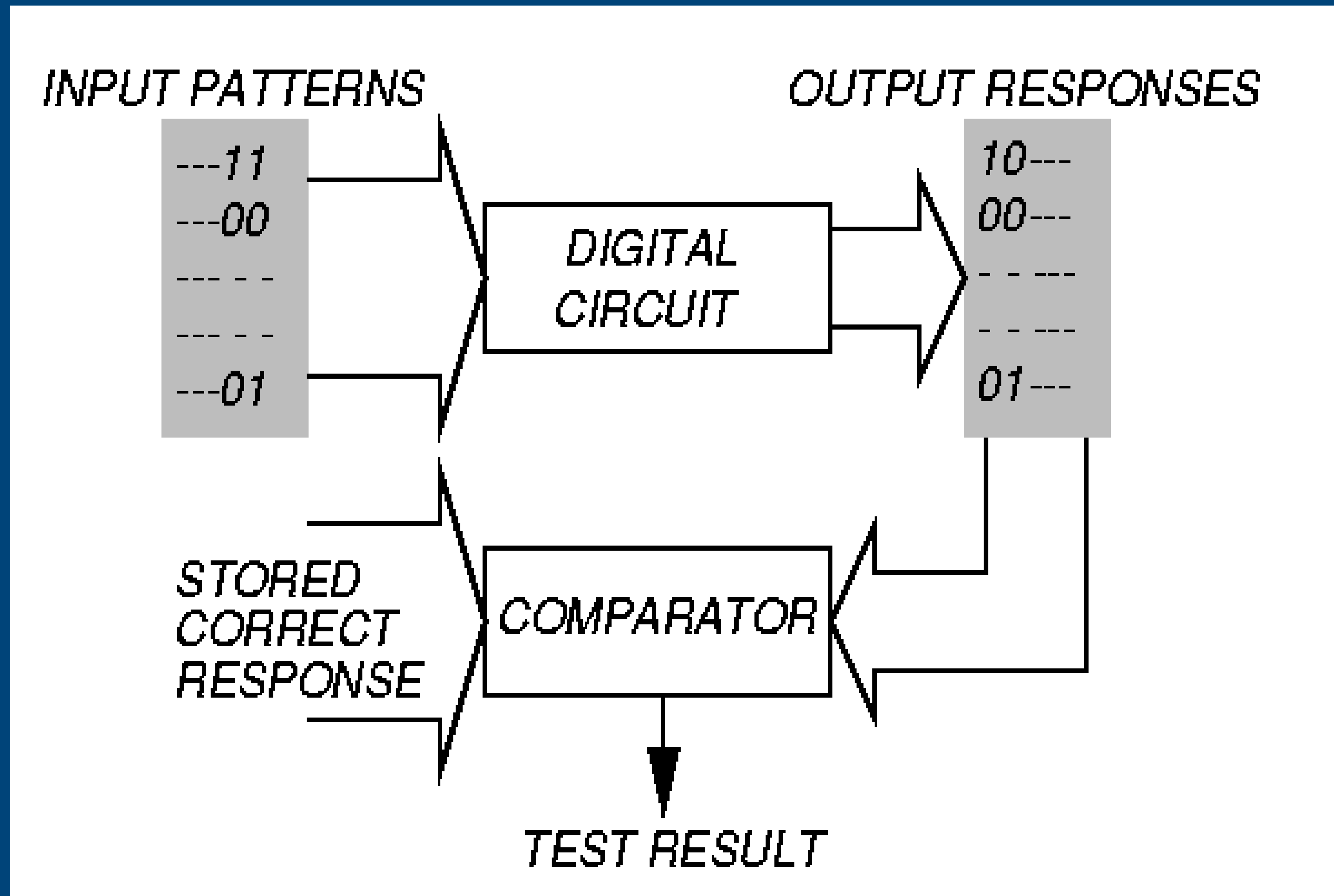
Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the *yield loss.*
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the *defect level.*

Trade-off

- Good chips pay for the failed ones
  – increase product costs
- Low yield loss and low defect level
- Low yield loss
  – less rigorous test
  – increases defect level
- Low defect level
  – rigorous test
  – increases yield loss

Testing Principle



Roles of Testing

- Detection: Determination whether or not the *device under test* (DUT) has some fault.
- Diagnosis: Identification of a specific fault that is present on DUT.
- Device characterization: Determination and correction of errors in design and/or test procedure.
- *Failure mode analysis* (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.

A Little Bit of History

- 1960's
  - Minicomputer controlled ATE systems (Teradyne,GenRad)
- 1970's
  - more complex sequential devices
  - algorithmic test patterns generation
  - guided probe & fault isolation via SW
  - difficult for LSI and boards
- Late 70's
  - in-circuit testing for boards
  - bed of nails

A Little Bit of History

- 1980's
  - Bed of nails difficult for surface mount devices
  - requirements for at-speed testing
- Late 80's
  - Built-in self tests (BIST)
- 1990's
  - current monitoring techniques
  - E-beam testing
- Late 90's
  - system-on-chip or core-based test requirements
  - mixed-signal testing

Types of Testing

- *Verification testing*, *characterization testing*, or *design debug*
  - Verifies correctness of design and of test procedure – usually requires correction to design
- *Manufacturing testing*
  - Factory testing of all manufactured chips for parametric faults and for random defects
- *Acceptance testing* (*incoming inspection*)
  - User (customer) tests purchased parts to ensure quality

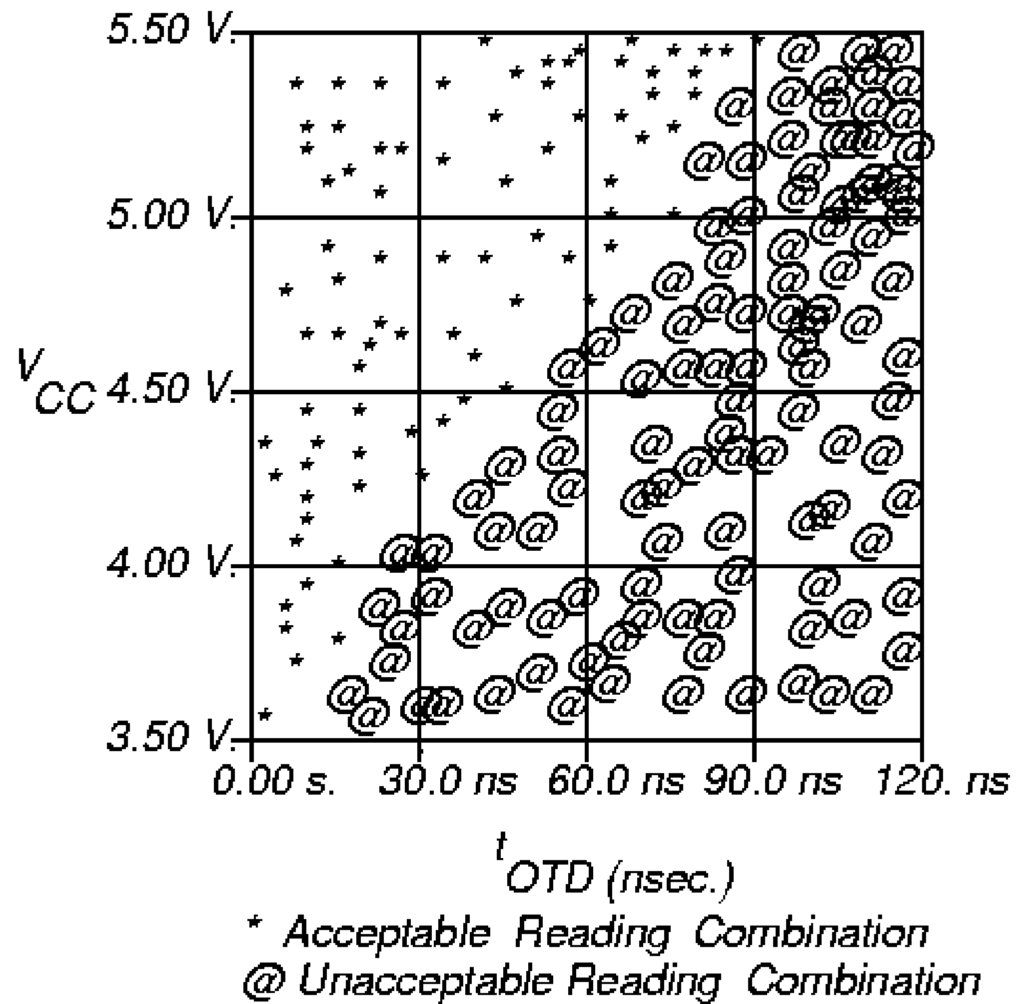
Verification Testing

- Ferociously expensive
- May comprise:
  - Electron beam testing
  - Artificial intelligence (expert system) methods
  - Repeated functional tests

Characterization Test

- Worst-case test
  - Choose test that passes/fails chips
  - Select statistically significant sample of chips
  - Repeat test for every combination of 2+ environmental variables
  - Plot results in *Shmoo plot*
  - Diagnose and correct design errors
- Continue throughout production life of chips to improve design and process to increase yield

Shmoo Plot



Incoming Inspection

- Can be:
  - Similar to production testing
  - More comprehensive than production testing
  - Tuned to specific systems application
- Often done for a random sample of devices
  - *Sample size* depends on device quality and system reliability requirements
  - Avoids putting defective device in a system where cost of diagnosis exceeds incoming inspection cost

Types of Manufacturing Tests

- *Wafer sort* or *probe* test – done before wafer is scribed and cut into chips
  - Includes test site characterization – specific test devices are checked with specific patterns to measure:
    - Gate threshold
    - Polysilicon field threshold
    - Poly sheet resistance, etc.
- Packaged device tests

Sub-types of Tests

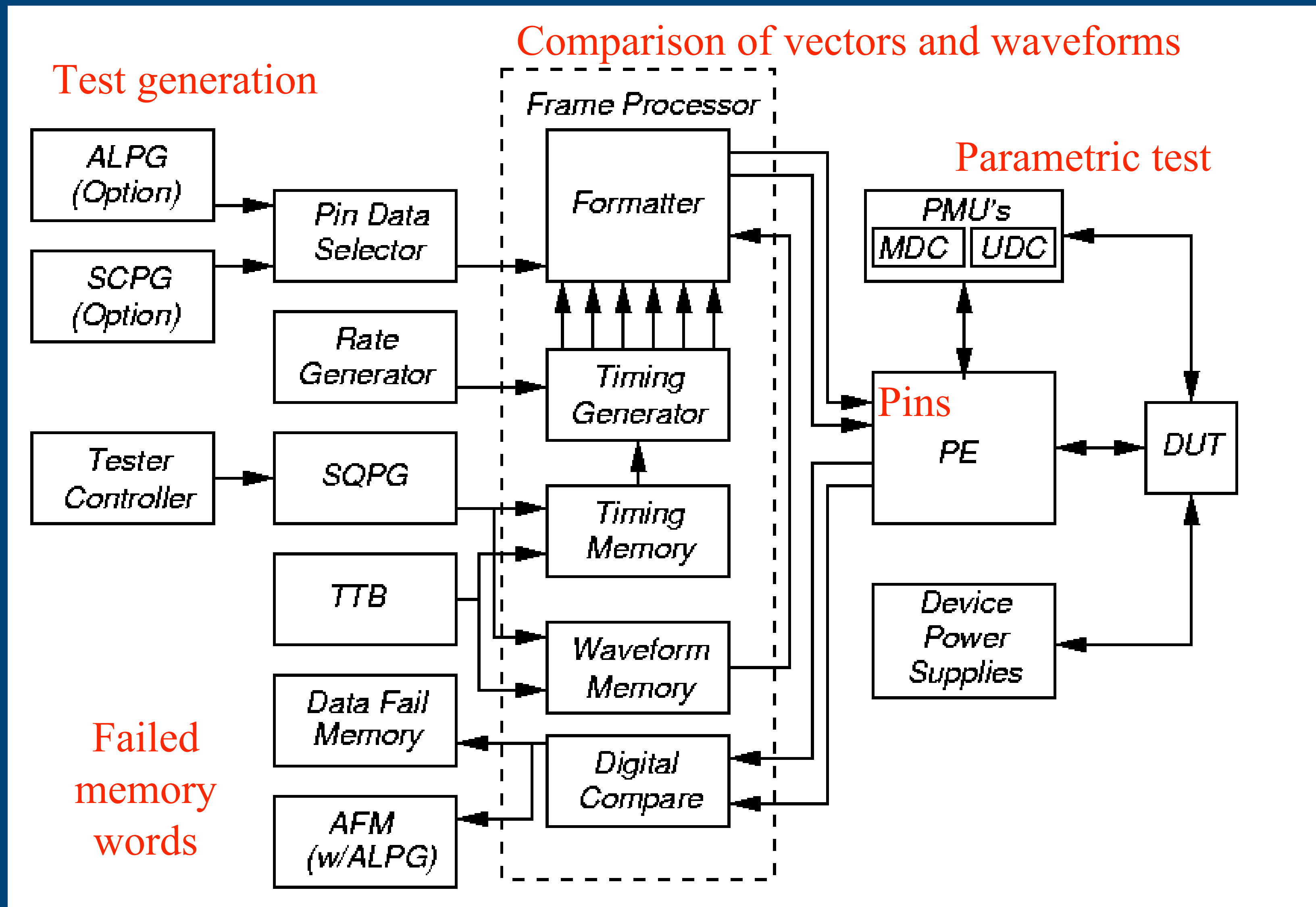
- *Parametric* – measures electrical properties of pin electronics – delay, voltages, currents, etc. – fast and cheap
- *Functional* – used to cover very high % of modeled faults – test every transistor and wire in digital circuits – long and expensive – main topic of course

Automatic Test Equipment Components

- Consists of:
  - Powerful computer
  - Powerful 32-bit *Digital Signal Processor* (DSP) for analog testing
  - Test Program (written in high-level language) running on the computer
  - Probe Head (actually touches the bare or packaged chip to perform fault detection experiments)
  - *Probe Card* or *Membrane Probe* (contains electronics to measure signals on chip pin or pad)

ADVANTEST Model T6682 ATE

T6682 ATE Block Diagram



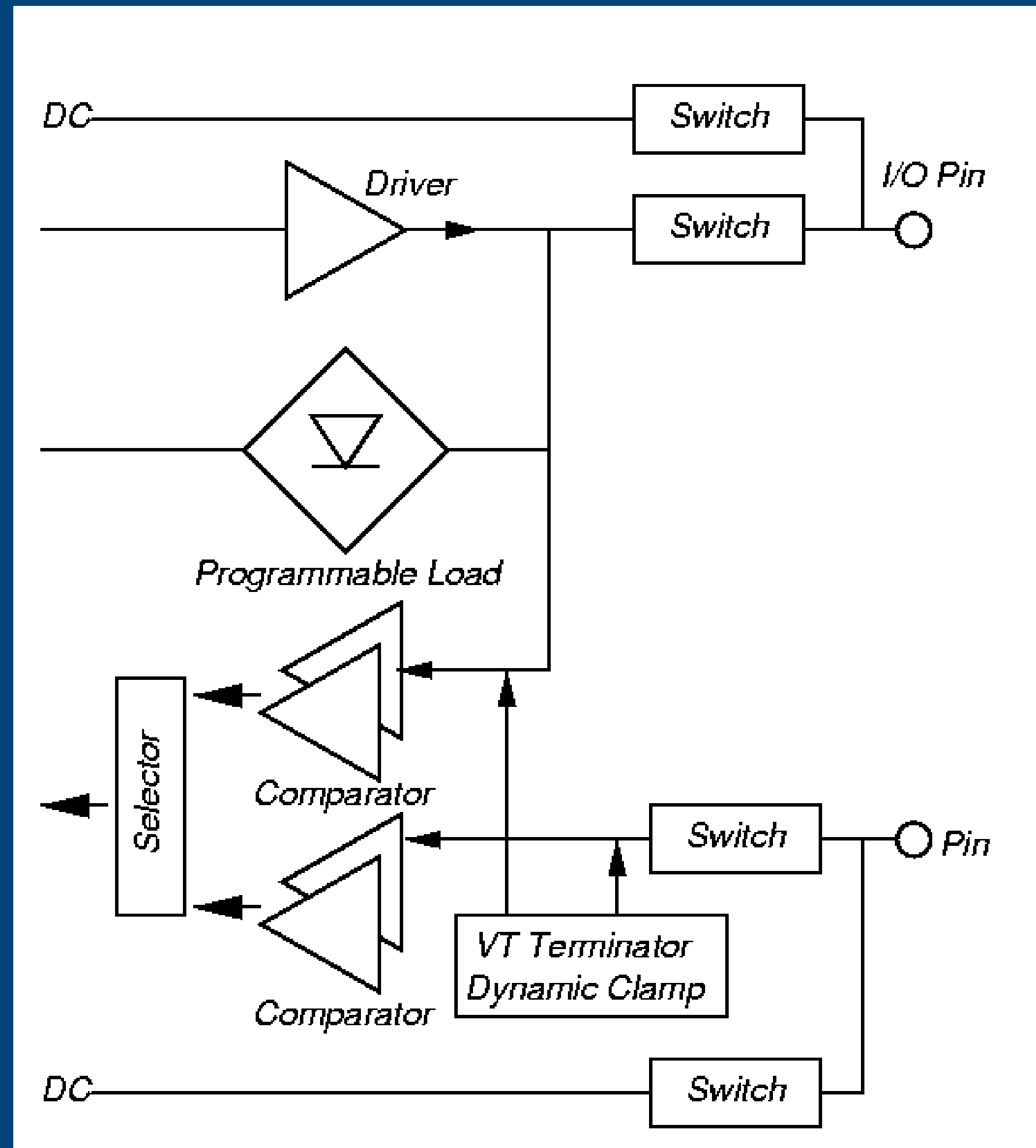
T6682 ATE Specifications

- Uses 0.35 μm VLSI chips in implementation
- 1024 pin channels
- Speed: 250, 500, or 1000 MHz
- Timing accuracy: +/- 200 ps
- Drive voltage: -2.5 to 6 V
- Clock/strobe accuracy: +/- 870 ps
- Clock settling resolution: 31.25 ps
- *Pattern multiplexing*: write 2 patterns in one ATE cycle
- *Pin multiplexing*: use 2 pins to control 1 DUT pin

Probing

- *Pin electronics* (PE) – electrical buffering circuits, put as close as possible to DUT
- Test head interface through custom printed circuit board to *wafer prober* (unpackaged chip test) or *package handler* (packaged chip test), touches chips through a socket (*contactor)*
- Uses liquid cooling
- Can independently set V_{IH} , V_{IL} , V_{OH} , V_{OL} , I_H , I_L , V_T for each pin
- *Parametric Measurement Unit* (PMU)

Pin Electronics



Probe Card and Probe Needles or Membrane

- *Probe card* – custom *printed circuit board* (PCB) on which DUT is mounted in socket – may contain custom measurement hardware (current test)
- *Probe needles* – come down and scratch the pads to stimulate/read pins
- *Membrane probe* – for unpackaged wafers – contacts printed on flexible membrane, pulled down onto wafer with compressed air to get wiping action

T6682 ATE Software

- Runs Solaris UNIX on UltraSPARC 167 MHz CPU for non-real time functions
- Runs real-time OS on UltraSPARC 200 MHz CPU for tester control
- Peripherals: disk, CD-ROM, micro-floppy, monitor, keyboard, HP GPIB, Ethernet
- *Viewpoint* software provided to debug, evaluate, & analyze VLSI chips

Cost of Testing

- Total production cost
  - fabrication + packaging + assembly + testing
- fabrication + packaging + assembly
  - per circuit cost is decreasing
- Testing
  - cost NOT decreasing
- Test Cost
  - test equipment cost, test activity cost, test controller, test pattern generator, interface drivers + receivers, cable and probe contacts, documentation, test personnel

Cost of Manufacturing Testing in 2000AD

- 0.5-1.0GHz, analog instruments,1,024 digital pins: ATE purchase price
  - = $1.2M + 1,024 x $3,000 = $4.272M
- Running cost (five-year linear depreciation)
  - = Depreciation + Maintenance + Operation
  - = $0.854M + $0.085M + $0.5M
  - = $1.439M/year
- Test cost (24 hour ATE operation)
  - = $1.439M/(365 x 24 x 3,600)
  - = 4.5 cents/second

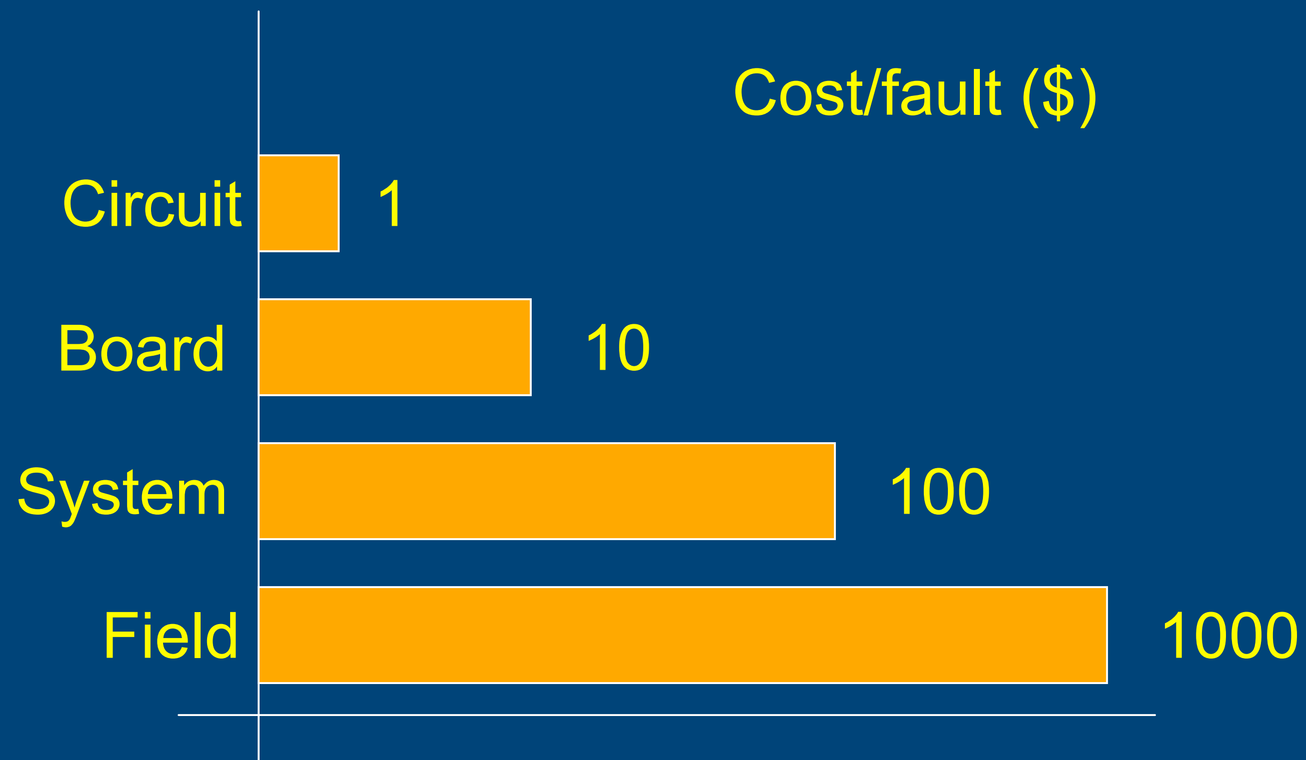
Cost per chip!

- Tester cost = 4.5 cents/second
- ASIC needs 6 seconds to be tested
- ASIC test cost = 27 cents
- If yield = 65% (good chips pay for the bad ones)
- ASIC test cost = 41.5 cents
  - 41% of a $1.00 chip
  - 8% of a $5.00 chip
- For a processor: 30s x 4.5 = $1.35 => $2.07
  - 50% of a $5.00 (Texas)

Testing Levels and Rule of 10

- Circuit/logic level
- Board level
- System level
- Field

Testing Levels and Rule of 10



Test Complexity

- CAD tools can help you design an IC in a month - but NOT TESTING!
- Intel 8080 would take over 10^{20} years at a one million tests per second!

Create adequate tests that run in limited time!