MIC05: Teste de Circuitos Integrados

Marcelo Lubaszewski

PPGMicro - UFRGS

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Design for Test

- **Definition:**

Design for test **(DFT) refers to those design techniques that make test generation and test application cost-effective.**

- **Types:**
  - **Design for Testability**
    - **Enhanced access**
  - **Built-In Self-Test**
    - **Internal test generation and response evaluation**
  - **Self-Checking Circuits**
    - **Error detection and correction codes**

Design for Testability : *Full-Scan*

- Ad-hoc methods
- *Scan design*
  - Scan register
  - Scan flip-flops
  - Scan test sequences
  - Overheads

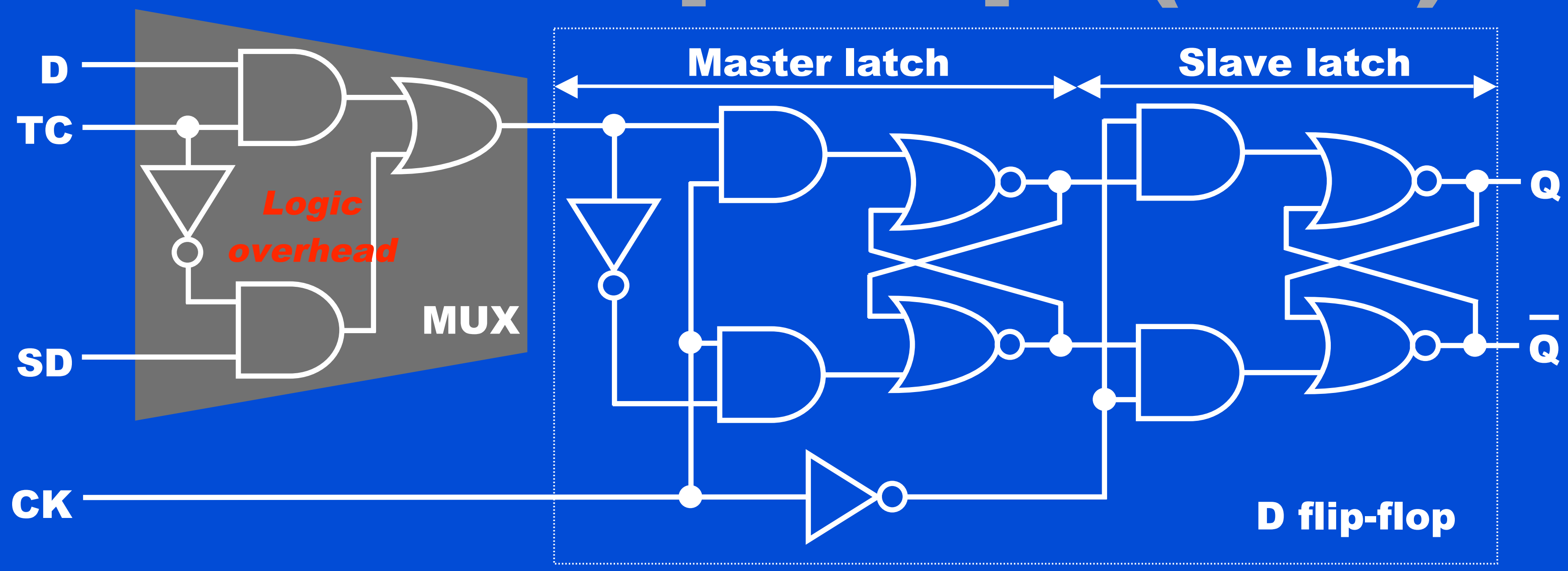
Ad-Hoc DFT Methods

- Good design practices learnt through experience are used as guidelines:
  - Avoid asynchronous (unclocked) feedback.
  - Make flip-flops initializable.
  - Avoid redundant gates. Avoid large fanin gates.
  - Provide test control for difficult-to-control signals.
  - Avoid gated clocks.
  - Consider ATE requirements (tristates, etc.)
- Design reviews conducted by experts or design auditing tools.
- Disadvantages of ad-hoc DFT methods:
  - Experts and tools not always available.
  - Test generation is often manual with no guarantee of high fault coverage.
  - Design iterations may be necessary.

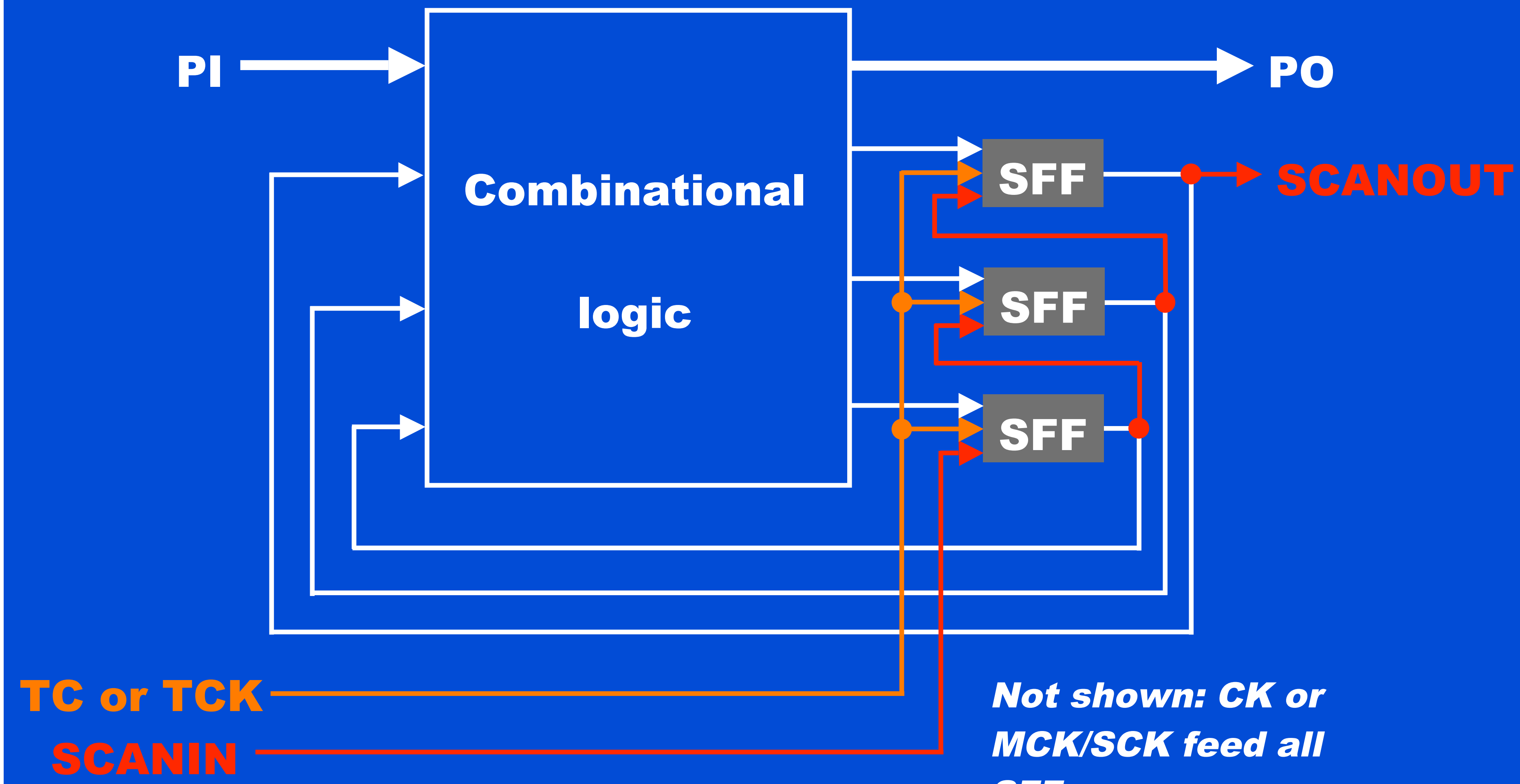
Scan Design

- Circuit is designed using pre-specified design rules.
- Test structure (hardware) is added to the verified design:
  - Add a *test control* (TC) primary input.
  - Replace flip-flops by *scan flip-flops* (SFF) and connect to form one or more shift registers in the test mode.
  - Make input/output of each scan shift register controllable/observable from PI/PO.
- Use combinational ATPG to obtain tests for all testable faults in the combinational logic.
- Add shift register tests and convert ATPG tests into scan sequences for use in manufacturing test.

Scan Flip-Flop (SFF)

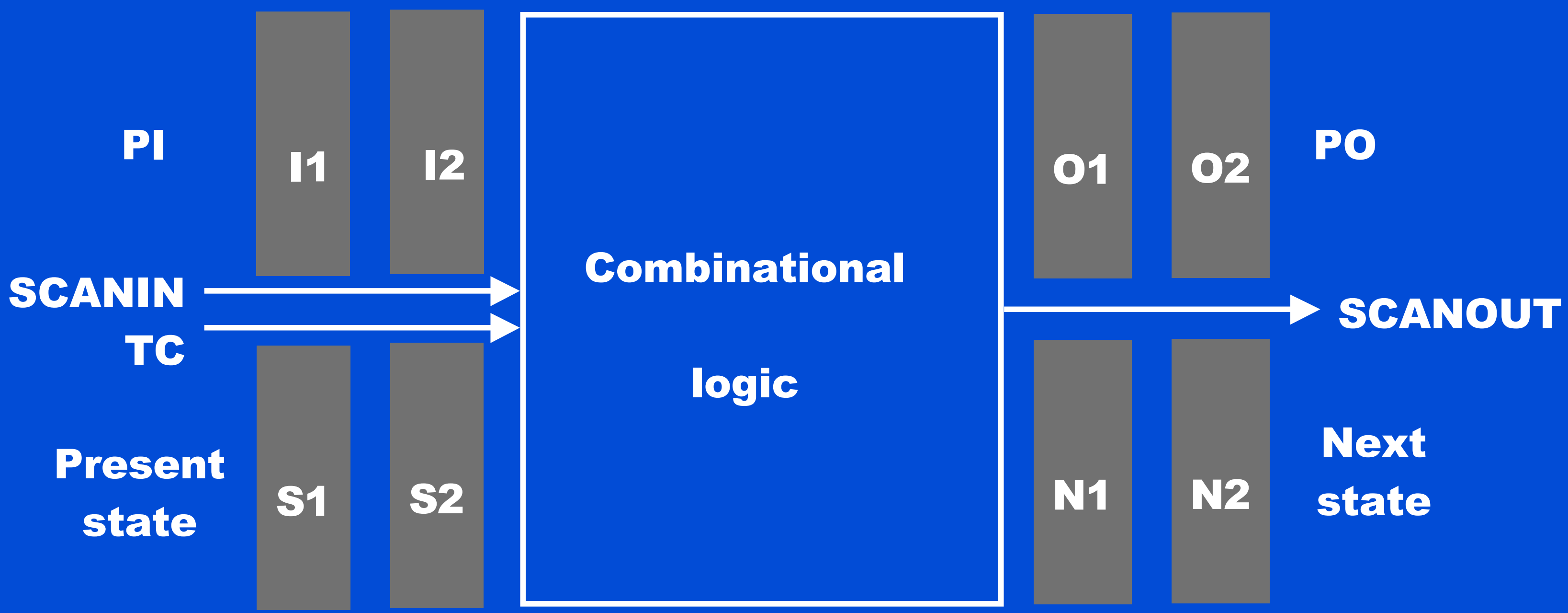


Adding Scan Structure

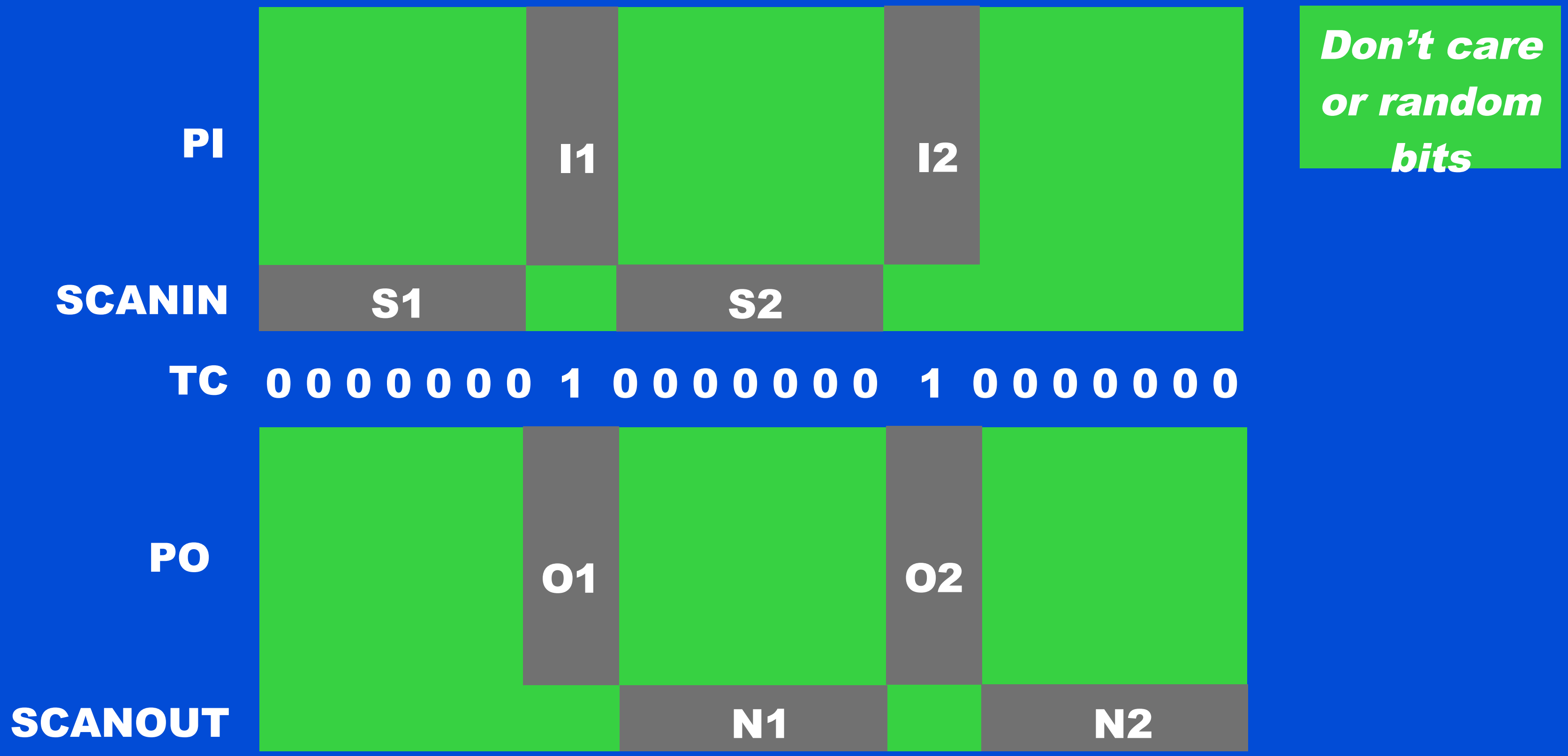


Not shown: CK or MCK/SCK feed all SFFs.

Comb. Test Vectors



Comb. Test Vectors



Sequence length **=** $(n_{comb} + 1)\, n_{sff} + n_{comb}$ ***clock periods***

n_{comb} = number of combinational vectors

n_{sff} = number of scan flip-flops

Testing Scan Register

- Scan register must be tested prior to application of scan test sequences.
- A shift sequence 00110011 . . . of length $n_{sff}+4$ in scan mode (TC=0) produces 00, 01, 11 and 10 transitions in all flip-flops and observes the result at SCANOUT output.
- Total scan test length:
  $(n_{comb} + 2)\ n_{sff} + n_{comb} + 4$ *clock periods*.
- Example: 2,000 scan flip-flops, 500 comb. vectors, total scan test length ~ 10^6 clocks.
- Multiple scan registers reduce test length.

Scan Overheads

- IO pins: One pin necessary.
- Area overhead:
  - *Gate overhead* = [4 $n_{sff}/(n_g+10n_{ff})$] x 100%, where n_g = *comb. gates*; n_{ff} = *flip-flops*; Example – n_g = 100k gates, n_{ff} = 2k *flip-flops*, overhead = 6.7%.
  - More accurate estimate must consider scan wiring and layout area.
- Performance overhead:
  - Multiplexer delay added in combinational path; approx. two gate-delays.
  - Flip-flop output loading due to one additional fanout; approx. 5-6%.

ATPG Example: S5378

	Original	Full-scan
Number of combinational gates	2,781	2,781
Number of non-scan flip-flops (10 gates each)	179	0
Number of scan flip-flops (14 gates each)	0	179
Gate overhead	0.0%	15.66%
Number of faults	4,603	4,603
PI/PO for ATPG	35/49	214/228
Fault coverage	70.0%	99.1%
Fault efficiency	70.9%	100.0%
CPU time on SUN Ultra II, 200MHz processor	5,533 s	5 s
Number of ATPG vectors	414	585
Scan sequence length	414	105,662

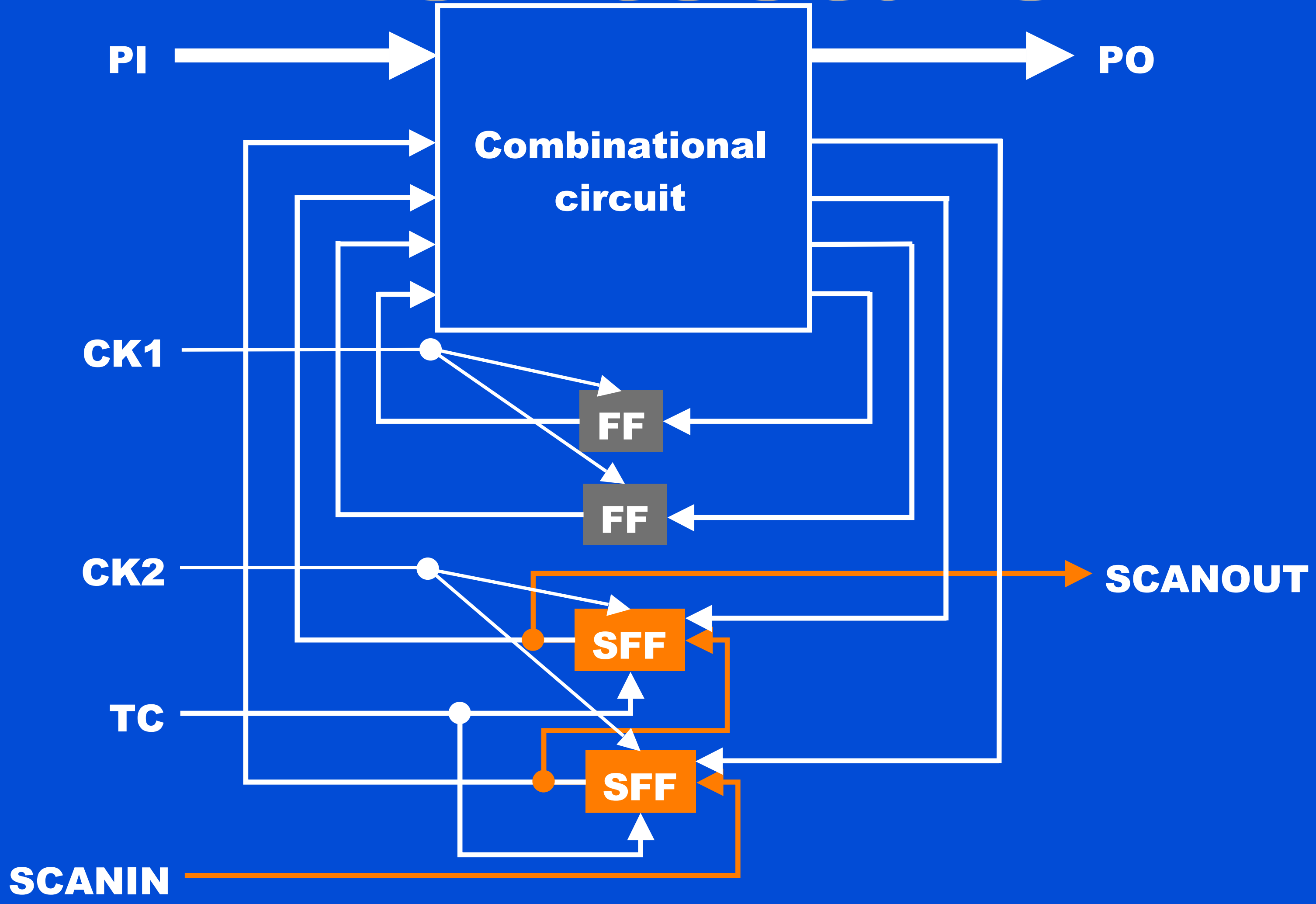
Design for Testability: *Partial-Scan*

- Definition
- *Partial-scan* architecture
- Historical background
- Cyclic and acyclic structures
- Partial-scan by cycle-breaking
  - S-graph and MFVS problem
  - Test generation and test statistics
  - Partial vs. full scan
  - Partial-scan flip-flop
- Summary

Partial-Scan Definition

- A subset of flip-flops is scanned.
- Objectives:
  - Minimize area overhead and scan sequence length, yet achieve required fault coverage
  - Exclude selected flip-flops from scan:
    - Improve performance
    - Allow limited scan design rule violations
  - Allow automation:
    - In scan flip-flop selection
    - In test generation
  - Shorter scan sequences

Partial-Scan Architecture



History of Partial-Scan

- Scan flip-flop selection from testability measures, Trischler *et al*., ITC-80; not too successful.
- Use of combinational ATPG:
  - Agrawal *et al*., D&T, Apr. 88
    - Functional vectors for initial fault coverage
    - Scan flip-flops selected by ATPG
  - Gupta *et al*., IEEETC, Apr. 90
    - Balanced structure
    - Sometimes requires high scan percentage
- Use of sequential ATPG:
  - Cheng and Agrawal, IEEETC, Apr. 90; Kunzmann and Wunderlich, JETTA, May 90
    - Create cycle-free structure for efficient ATPG

Difficulties in Seq. ATPG

- Poor initializability.
- Poor controllability/observability of state variables.
- Gate count, number of flip-flops, and sequential depth do not explain the problem.
- Cycles are mainly responsible for complexity.
- An ATPG experiment:

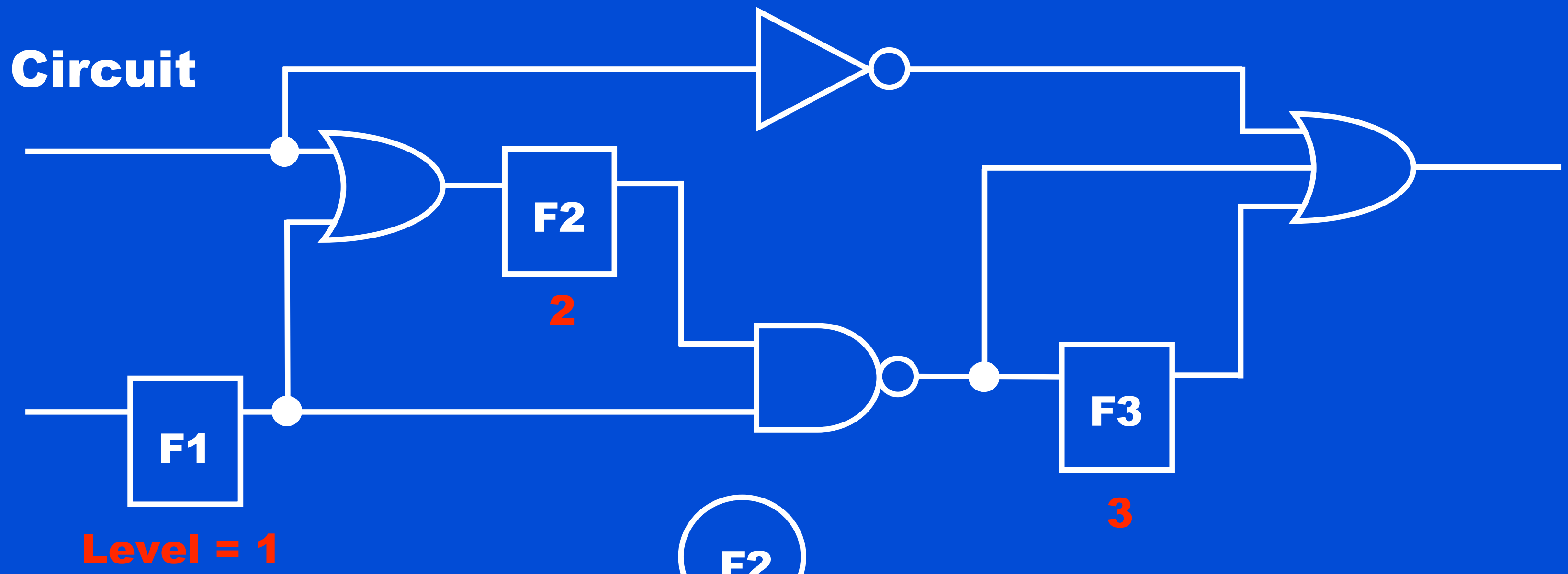
Circuit	Number of gates	Number of flip-flops	Sequential depth	ATPG CPU s	Fault coverage
TLC	355	21	14*	1,247	89.01%
Chip A	1,112	39	14	269	98.80%

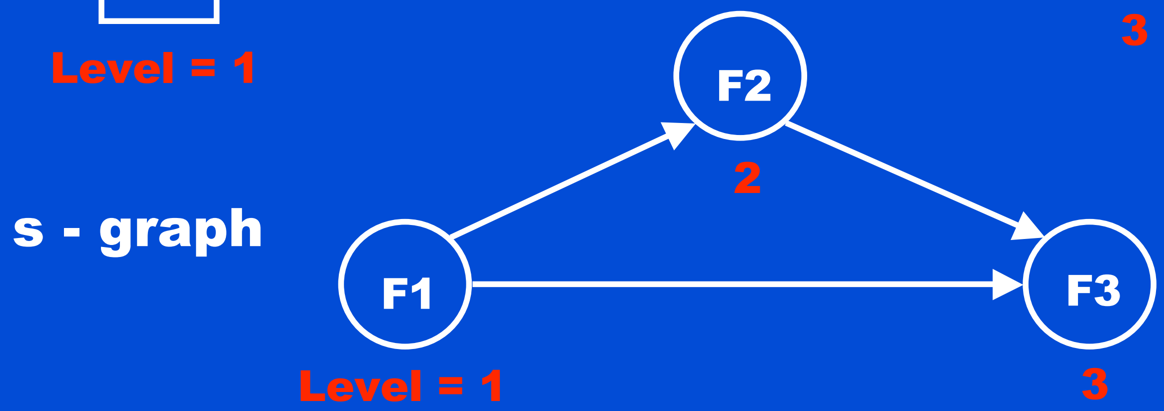
** Maximum number of flip-flops on a PI to PO path*

Benchmark Circuits

Circuit	s1196	s1238	s1488	s1494
PI	14	14	8	8
PO	14	14	19	19
FF	18	18	6	6
Gates	529	508	653	647
Structure	Cycle-free	Cycle-free	Cyclic	Cyclic
Sequential depth	4	4	--	--
Total faults	1242	1355	1486	1506
Detected faults	1239	1283	1384	1379
Potentially detected faults	0	0	2	2
Untestable faults	3	72	26	30
Abandoned faults	0	0	76	97
Fault coverage (%)	99.8	94.7	93.1	91.6
Fault efficiency (%)	100.0	100.0	94.8	93.4
Max. sequence length	3	3	24	28
Total test vectors	313	308	525	559
Gentest CPU s (Sparc 2)	10	15	19941	19183

Cycle-Free Example





$d_{seq} = 3$

All faults are testable. See Example 8.6.

Relevant Results

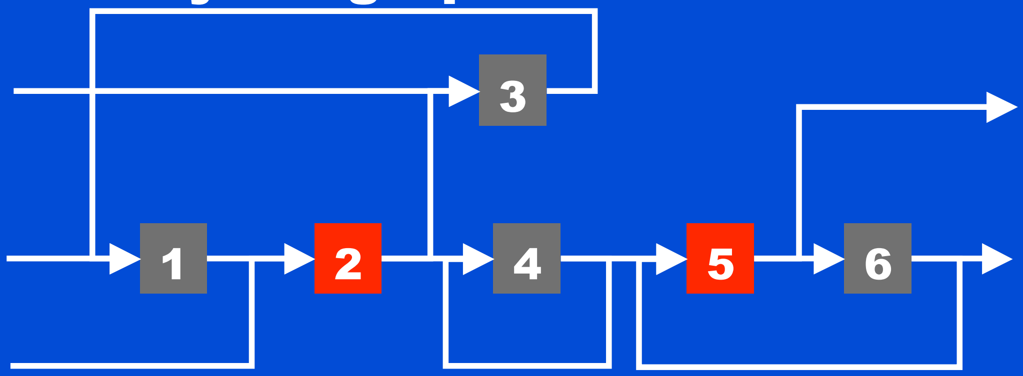
- Theorem 8.1: A cycle-free circuit is always initializable. It is also initializable in the presence of any non-flip-flop fault.
- Theorem 8.2: Any non-flip-flop fault in a cycle-free circuit can be detected by at most $d_{seq} + 1$ vectors.
- ATPG complexity: To determine that a fault is untestable in a cyclic circuit, an ATPG program using nine-valued logic may have to analyze 9^{Nff} time-frames, where Nff is the number of flip-flops in the circuit.

A Partial-Scan Method

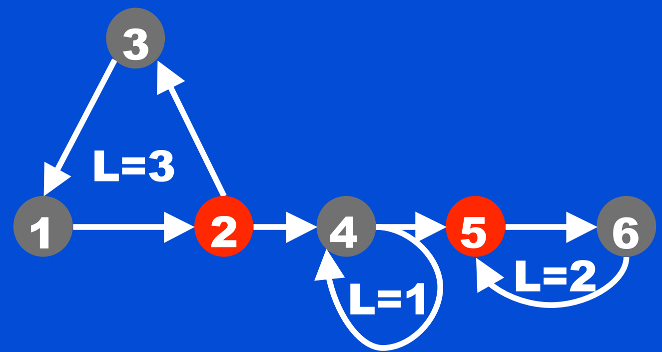
- Select a minimal set of flip-flops for scan to eliminate all cycles.
- Alternatively, to keep the overhead low only long cycles may be eliminated.
- In some circuits with a large number of self-loops, all cycles other than self-loops may be eliminated.

The MFVS Problem

- For a directed graph find a set of vertices with smallest cardinality such that the deletion of this vertex-set makes the graph acyclic.
- The *minimum feedback vertex set* (MFVS) problem is NP-complete; practical solutions use heuristics.
- A secondary objective of minimizing the depth of acyclic graph is useful.



A 6-flip-flop circuit



s-graph

Test Generation

- Scan and non-scan flip-flops are controlled from separate clock PIs:
  - Normal mode – Both clocks active
  - Scan mode – Only scan clock active
- Seq. ATPG model:
  - Scan flip-flops replaced by PI and PO
  - Seq. ATPG program used for test generation
  - Scan register test sequence, 001100…, of length $n_{sff} + 4$ applied in the scan mode
  - Each ATPG vector is preceded by a scan-in sequence to set scan flip-flop states
  - A scan-out sequence is added at the end of each vector sequence
- Test length = $(n_{ATPG} + 2)\ n_{sff} + n_{ATPG} + 4$ clocks

Partial Scan Example

- Circuit: TLC
- 355 gates
- 21 flip-flops

Scan flip-flops	Max. cycle length	Depth*	ATPG CPU s	Fault sim. CPU s	Fault cov.	ATPG vectors	Test seq. length
0	4	14	1,247	61	89.01%	805	805
4	2	10	157	11	95.90%	247	1,249
9	1	5	32	4	99.20%	136	1,382
10	1	3	13	4	100.00%	112	1,256
21	0	0	2	2	100.00%	52	1,190

* Cyclic paths ignored

Partial vs. Full Scan: S5378

	Original	Partial-scan	Full-scan
Number of combinational gates	2,781	2,781	2,781
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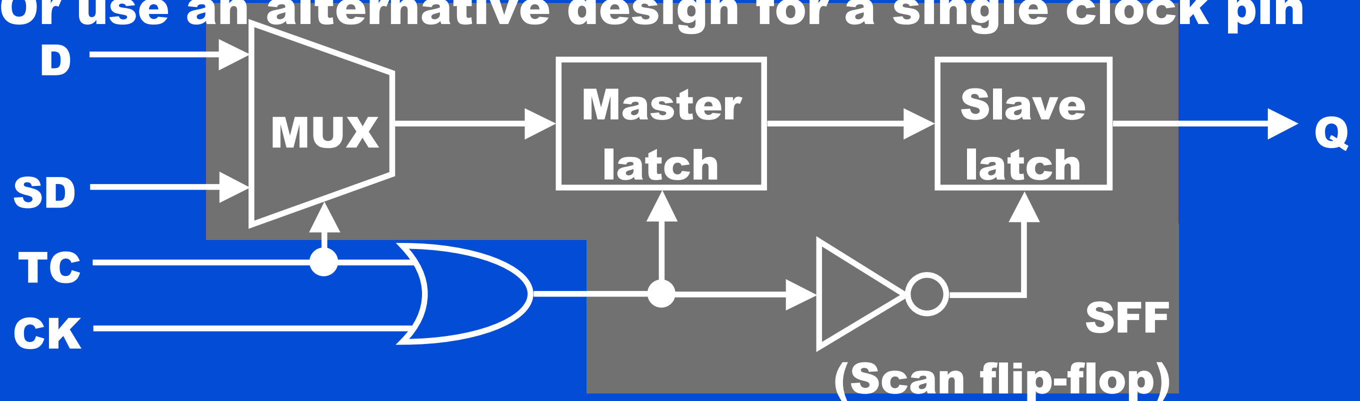
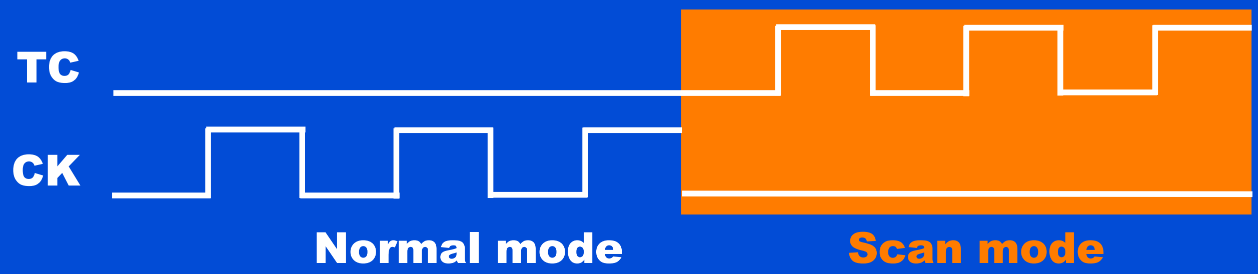
CPU time on SUN Ultra II 200MHz processor	5,533 s	727 s	5 s
Number of ATPG vectors	414	1,117	585
Scan sequence length	414	34,691	105,662

Flip-flop for Partial Scan

- Normal scan flip-flop (SFF) with multiplexer of the LSSD flip-flop is used.
- Scan flip-flops require a separate clock control:
  - Either use a separate clock pin
  - Or use an alternative design for a single clock pin





Summary

- Partial-scan is a generalized scan method; scan can vary from 0 to 100%.
- Elimination of long cycles can improve testability via sequential ATPG.
- Elimination of all cycles and self-loops allows combinational ATPG.
- Partial-scan has lower overheads (area and delay) and reduced test length.
- Partial-scan allows limited violations of scan design rules, e.g., a flip-flop on a critical path may not be scanned.