MIC05: Teste de Circuitos Integrados

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PGMicro - UFRGS

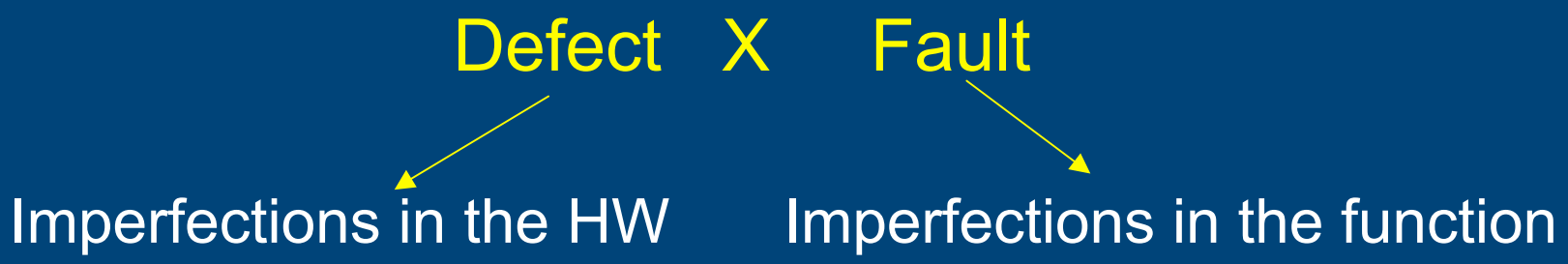
2007/II

Lecture 2 - Fault Modeling

- Defects, Errors, and Faults
- Why model faults?
- Some real defects in VLSI and PCB
- Common fault models
- Stuck-at faults
    - Single stuck-at faults
    - Fault equivalence
    - Fault dominance and checkpoint theorem
    - Classes of stuck-at faults and multiple faults
- Other Common Faults
- Faults in FPGAs

Defects, Faults, and Errors

- Defect: unintended difference between the implemented HW and its intended design
  - May or may not cause a system failure
- Fault: representation of a defect at the abstracted function level



Defects, Faults, and Errors

- Error: Manifestation of a fault that results in incorrect circuit (system) outputs or states
  - Caused by faults
- Failure: Deviation of a circuit or system from its specified behavior
  - Fails to do what it should do
  - Caused by an error
- Defect --> Fault ---> Error ---> Failure

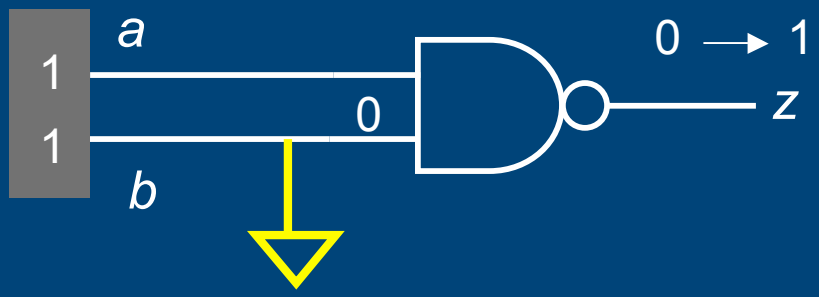
Some Real Defects in Chips

- Processing defects
  - Missing contact windows
  - Parasitic transistors
  - Oxide breakdown
  - . . .
- Material defects
  - Bulk defects (cracks, crystal imperfections)
  - Surface impurities (ion migration)
  - . . .
- Time-dependent defects
  - Dielectric breakdown
  - Electromigration
  - . . .
- Packaging defects
  - Contact degradation
  - Seal leaks. . .

Ref.: M. J. Howes and D. V. Morgan, *Reliability and Degradation - Semiconductor Devices and Circuits,* Wiley, 1981.

Example

- Defect: a short to ground
- Fault: signal b stuck at logic 0



- Error: z has the wrong value if a = b = 1

Example

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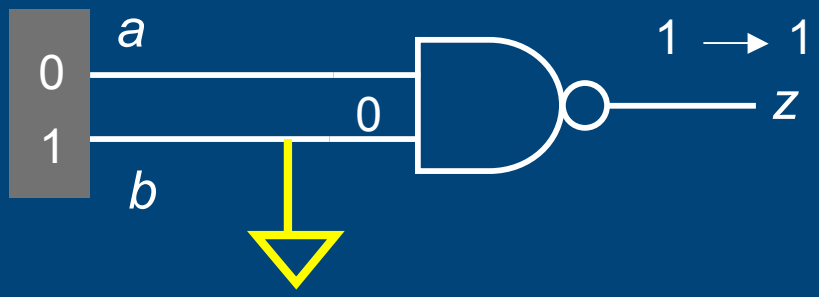

- Error: z has the wrong value if a = b = 1
- But, if a = 0, fault exists, but no error!

Why Model Faults?

- Real defects (often mechanical) too numerous and often not analyzable
- A fault model identifies targets for testing
  - Model faults most likely to occur
- Fault model limits the scope of test generation
  - Create tests only for the modeled faults
- A fault model makes analysis possible
  - Associate specific defects with specific test patterns
- Effectiveness measurable by experiments
  - Fault coverage can be computed for specific test patterns to reflect its effectiveness

Common Fault Models

- Single stuck-at faults
- Transistor open and short faults
- Memory faults
- PLA faults (stuck-at, cross-point, bridging)
- Functional faults (processors)
- Delay faults (transition, path)
- Analog faults

Single Stuck-at Fault

- Three properties define a single stuck-at fault
  - Only one line is faulty
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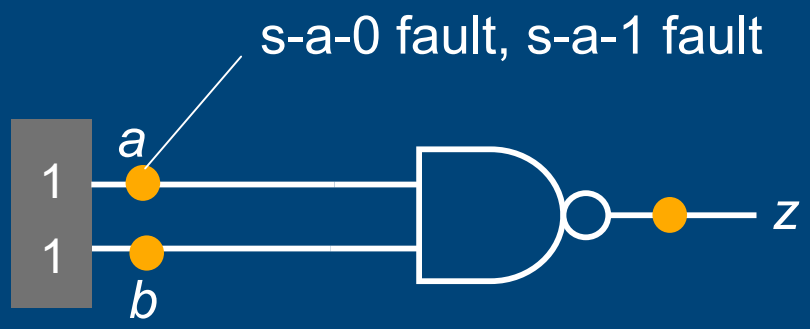

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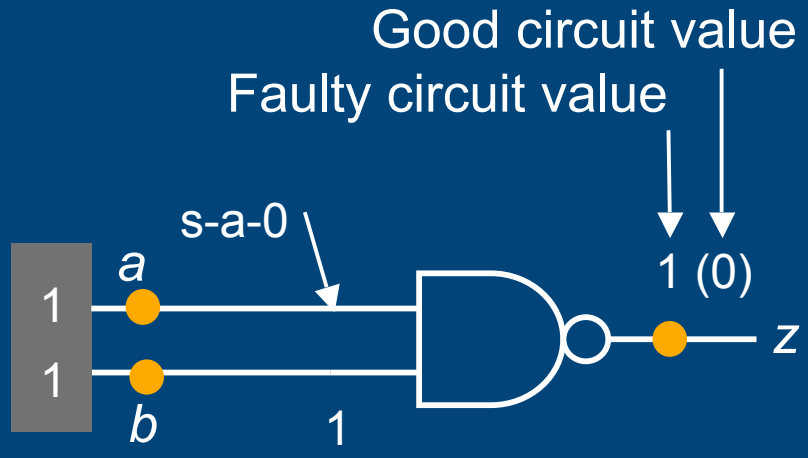

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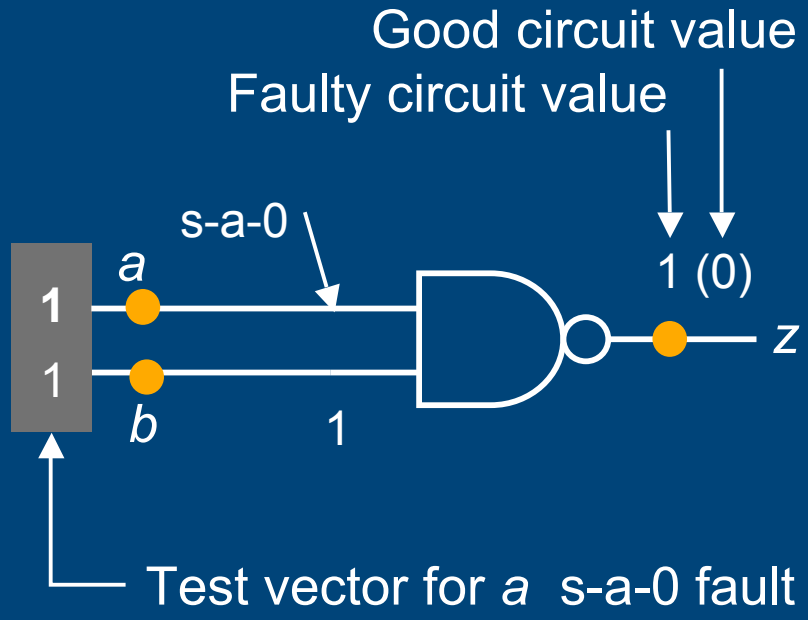
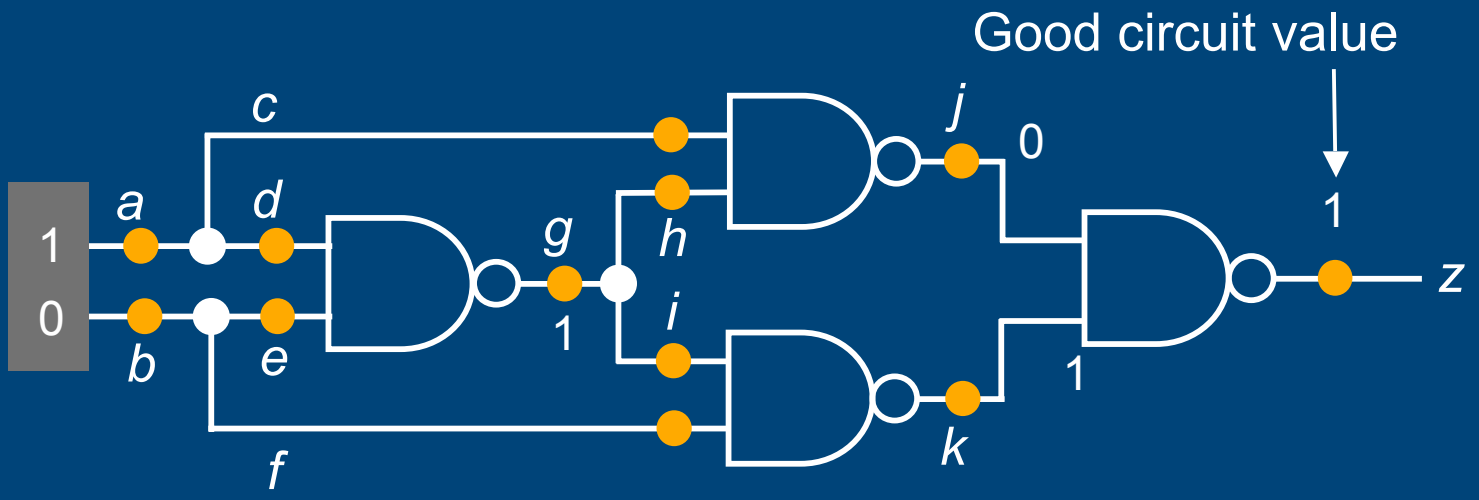


Single Stuck-at Fault

Example: XOR circuit has 12 fault sites and 24 single stuck-at faults



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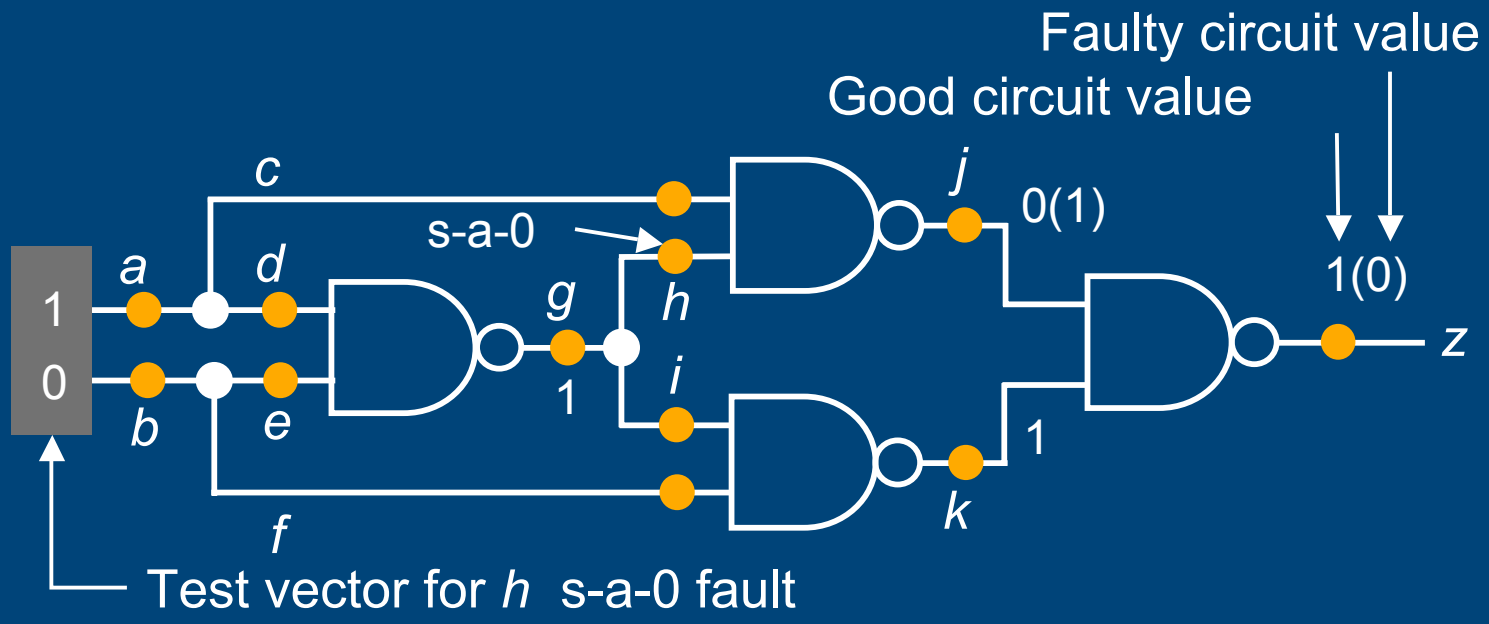
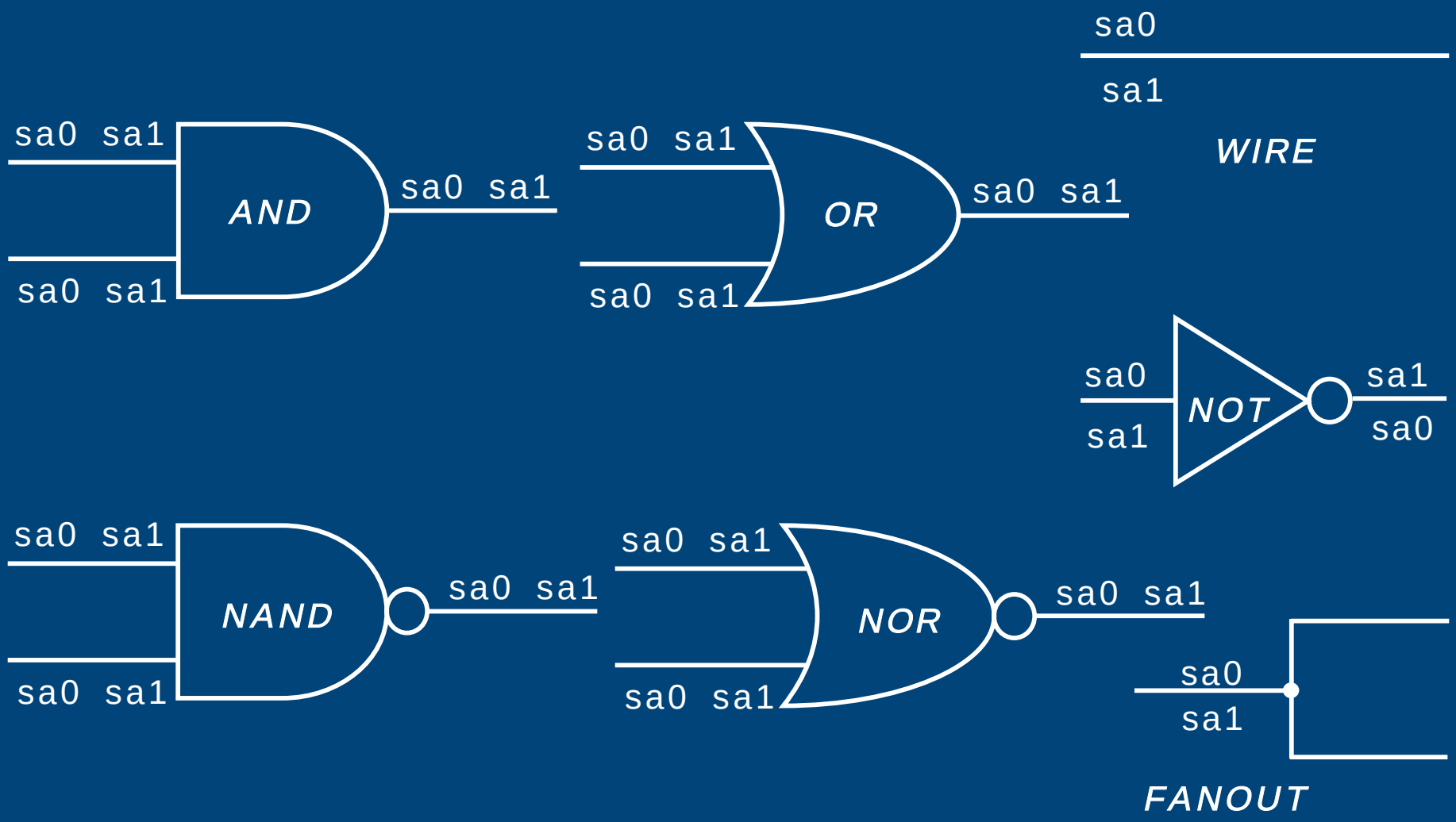


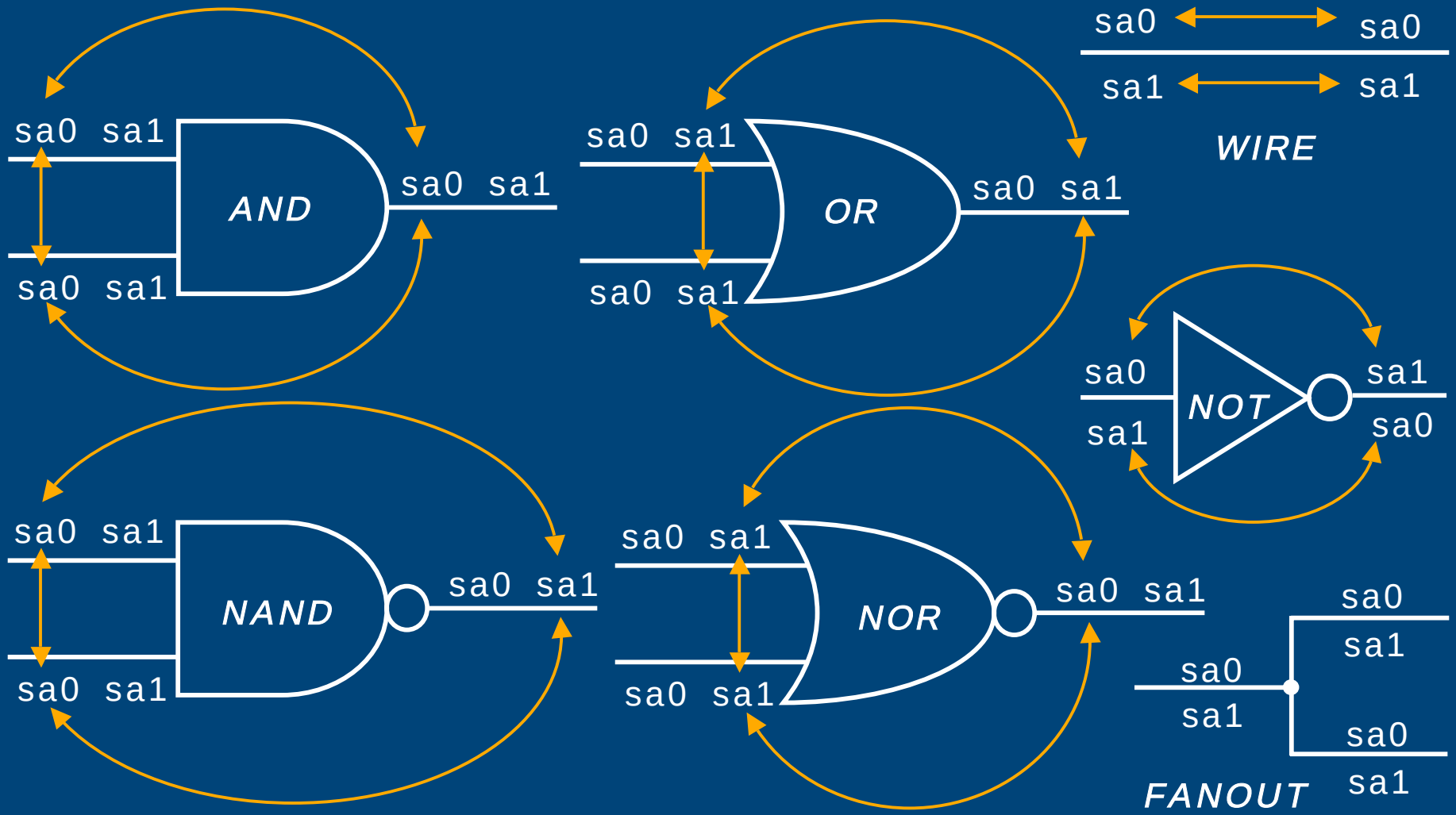
Fault Equivalence

- Fault equivalence: Two faults f1 and f2 are equivalent if all tests that detect f1 also detect f2.
- If faults f1 and f2 are equivalent then the corresponding faulty functions are identical.
- Fault collapsing: All single faults of a logic circuit can be divided into disjoint equivalence subsets, where all faults in a subset are mutually equivalent. A collapsed fault set contains one fault from each equivalence subset.

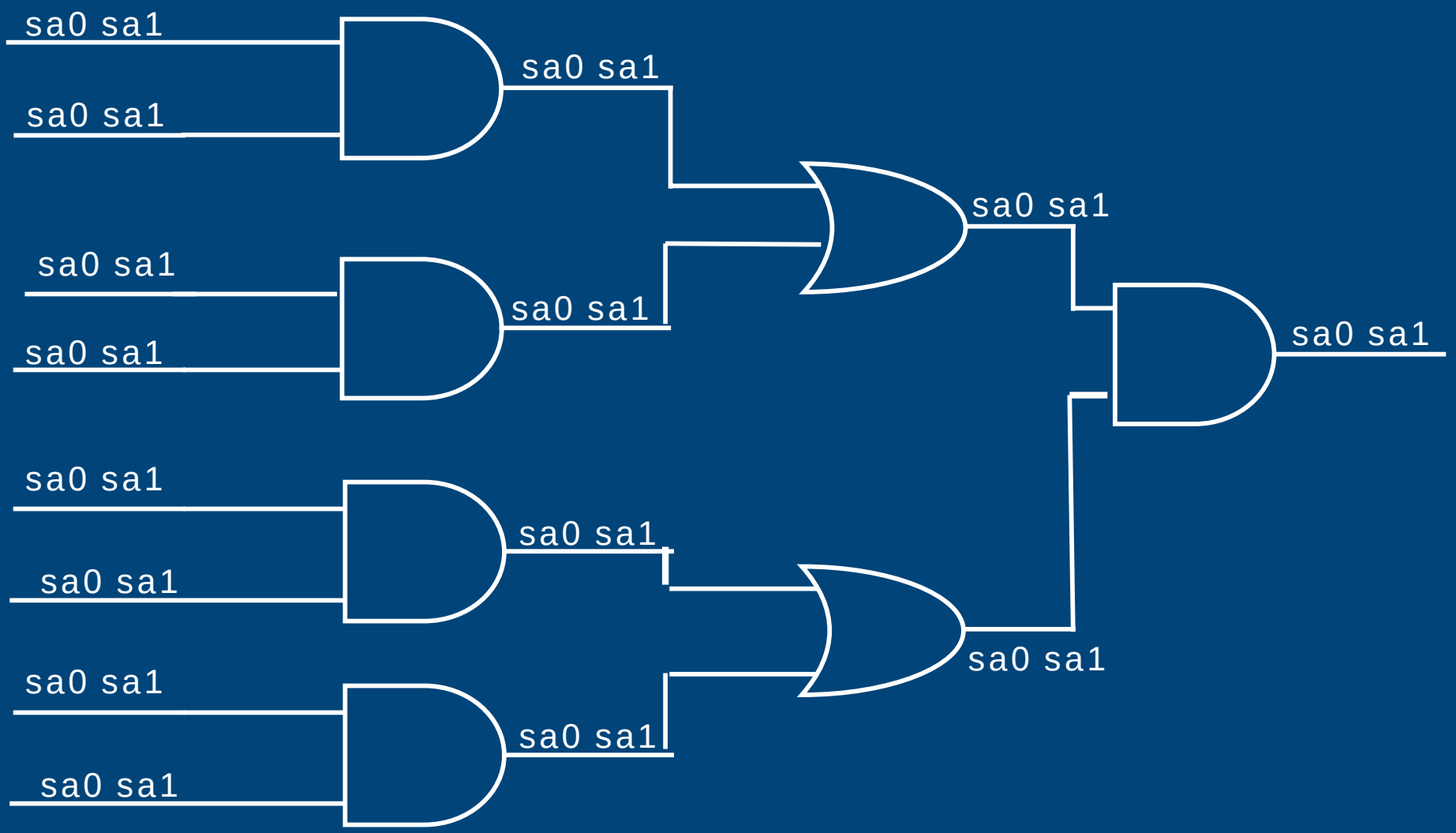
Equivalence Rules



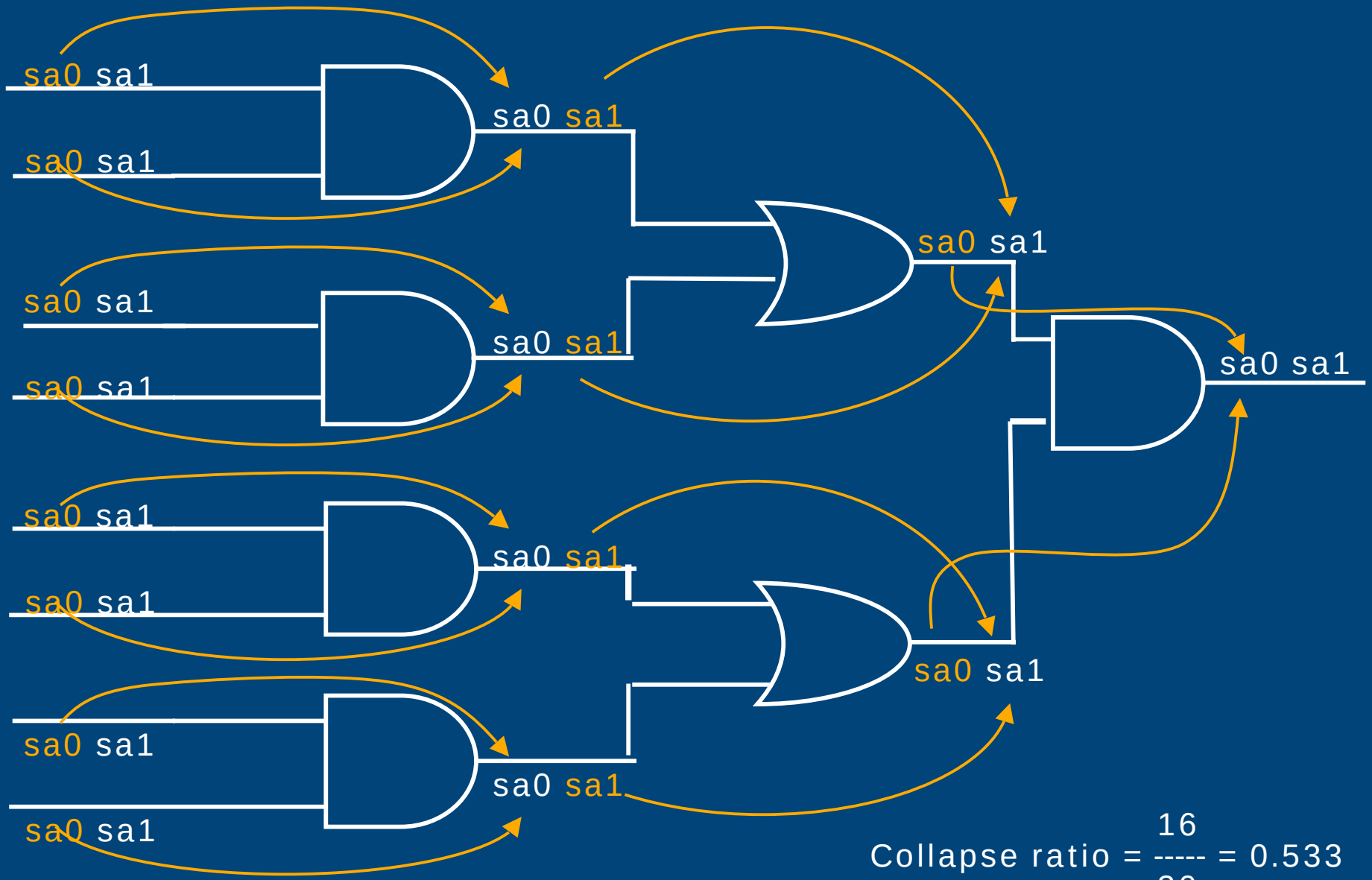
Equivalence Rules



Equivalence Example

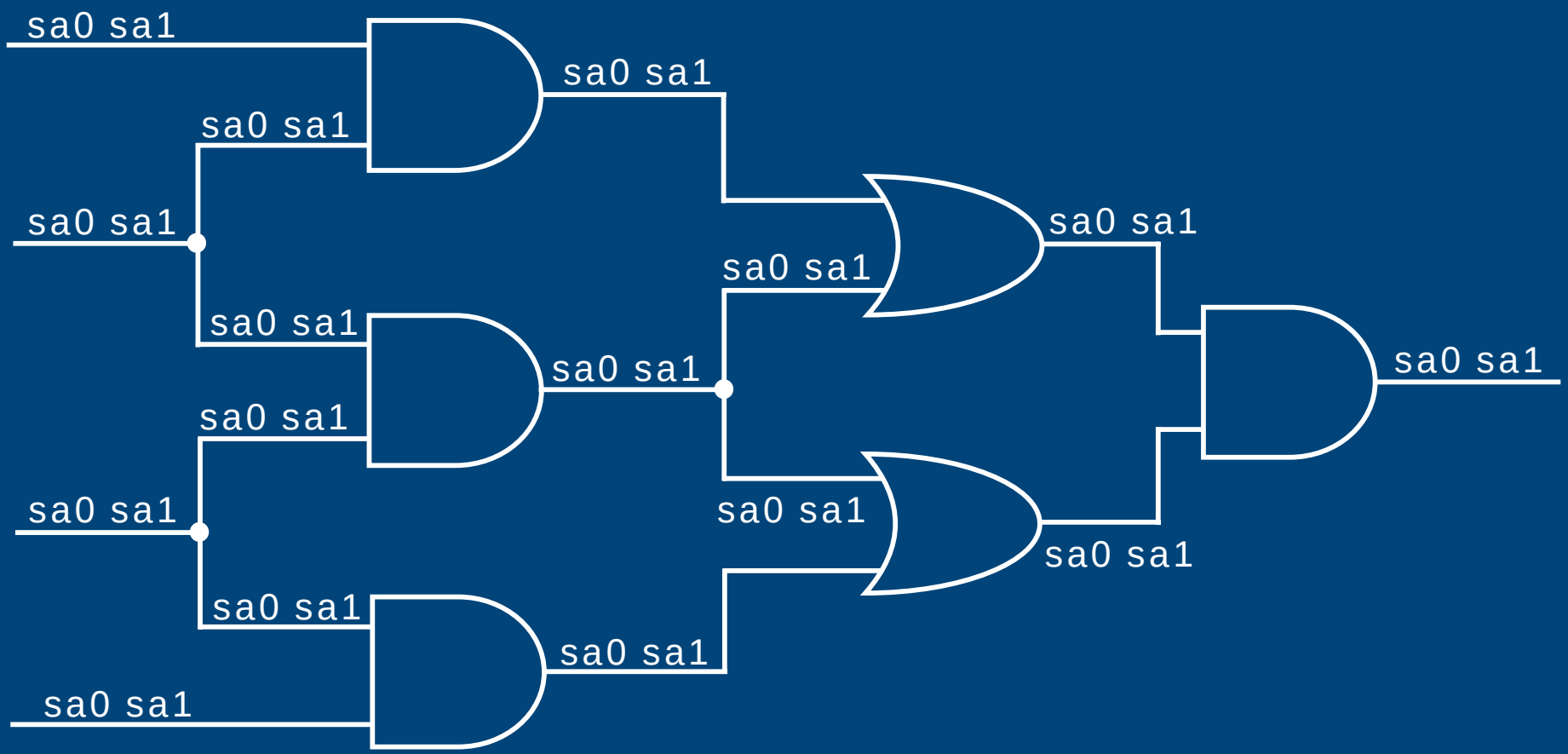


Equivalence Example

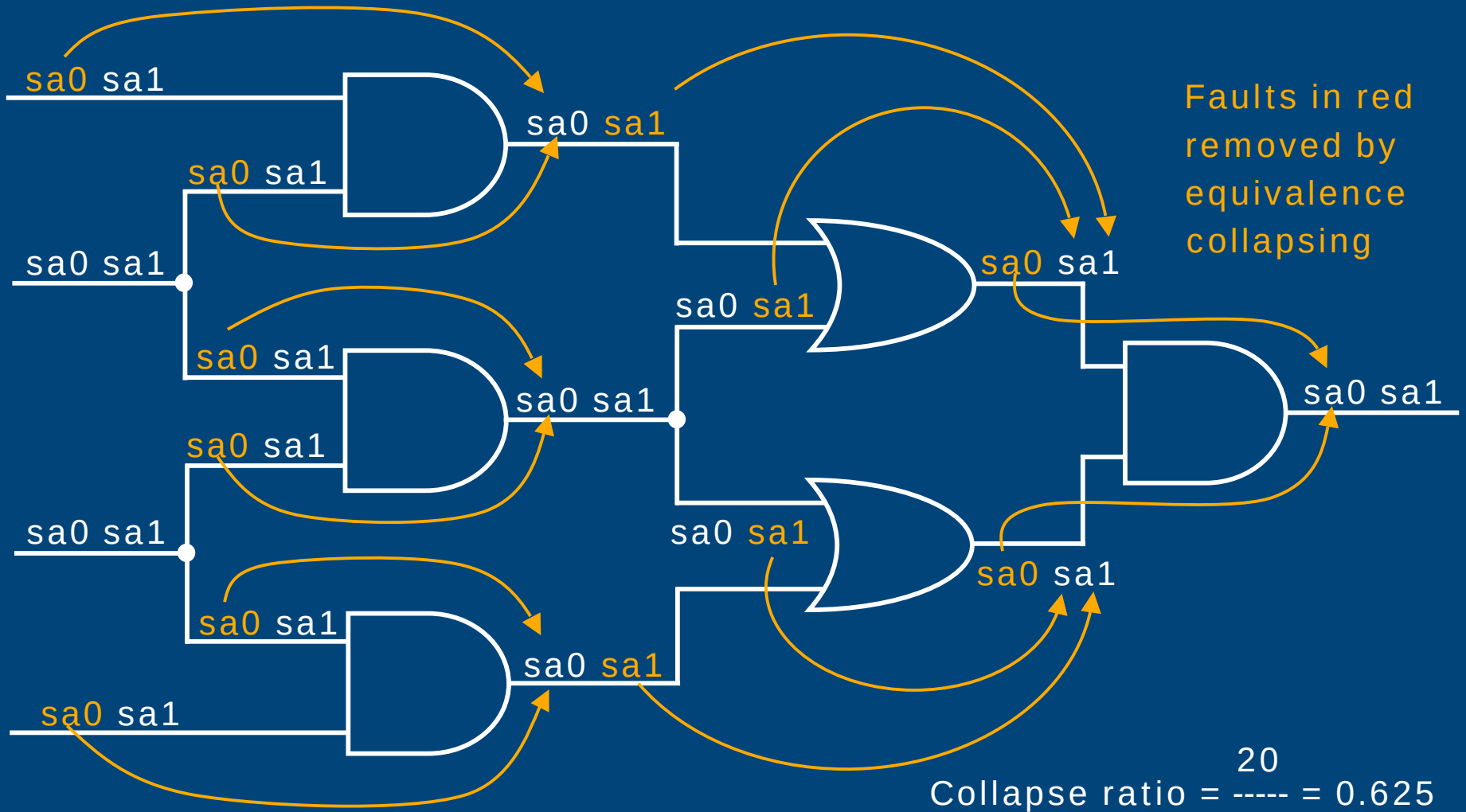


$$\text{Collapse ratio} = \frac{16}{30} = 0.533$$

Equivalence Example



Equivalence Example



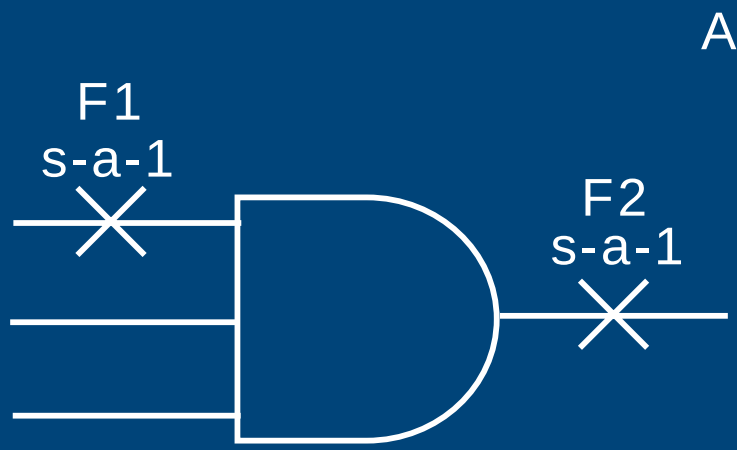
Collapse ratio = $\frac{20}{32} = 0.625$

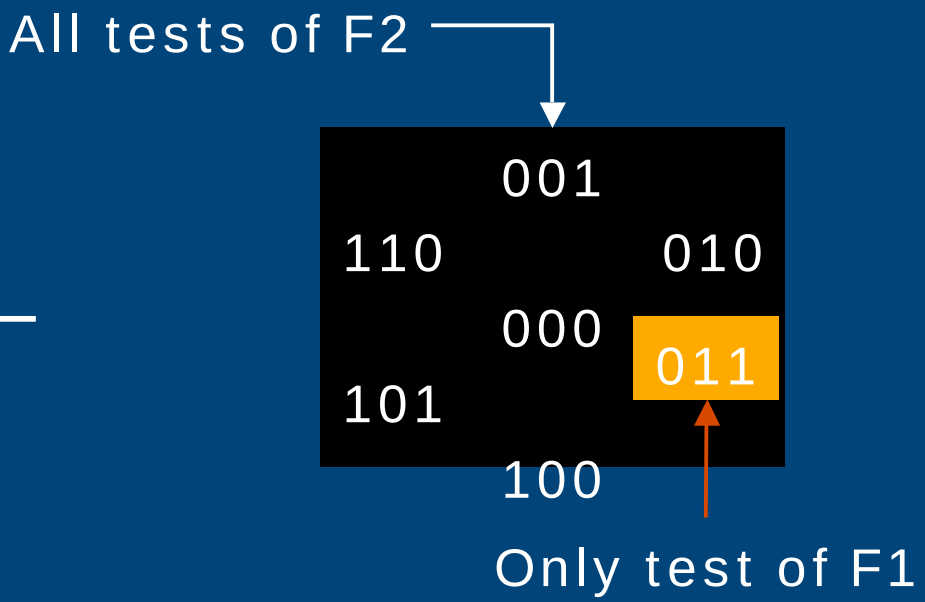
Fault Dominance

- If all tests of some fault F1 detect another fault F2, then F2 is said to dominate F1.
- Dominance fault collapsing: If fault F2 dominates F1, then F2 is removed from the fault list.
- When dominance fault collapsing is used, it is sufficient to consider only the input faults of Boolean gates. See the next example.

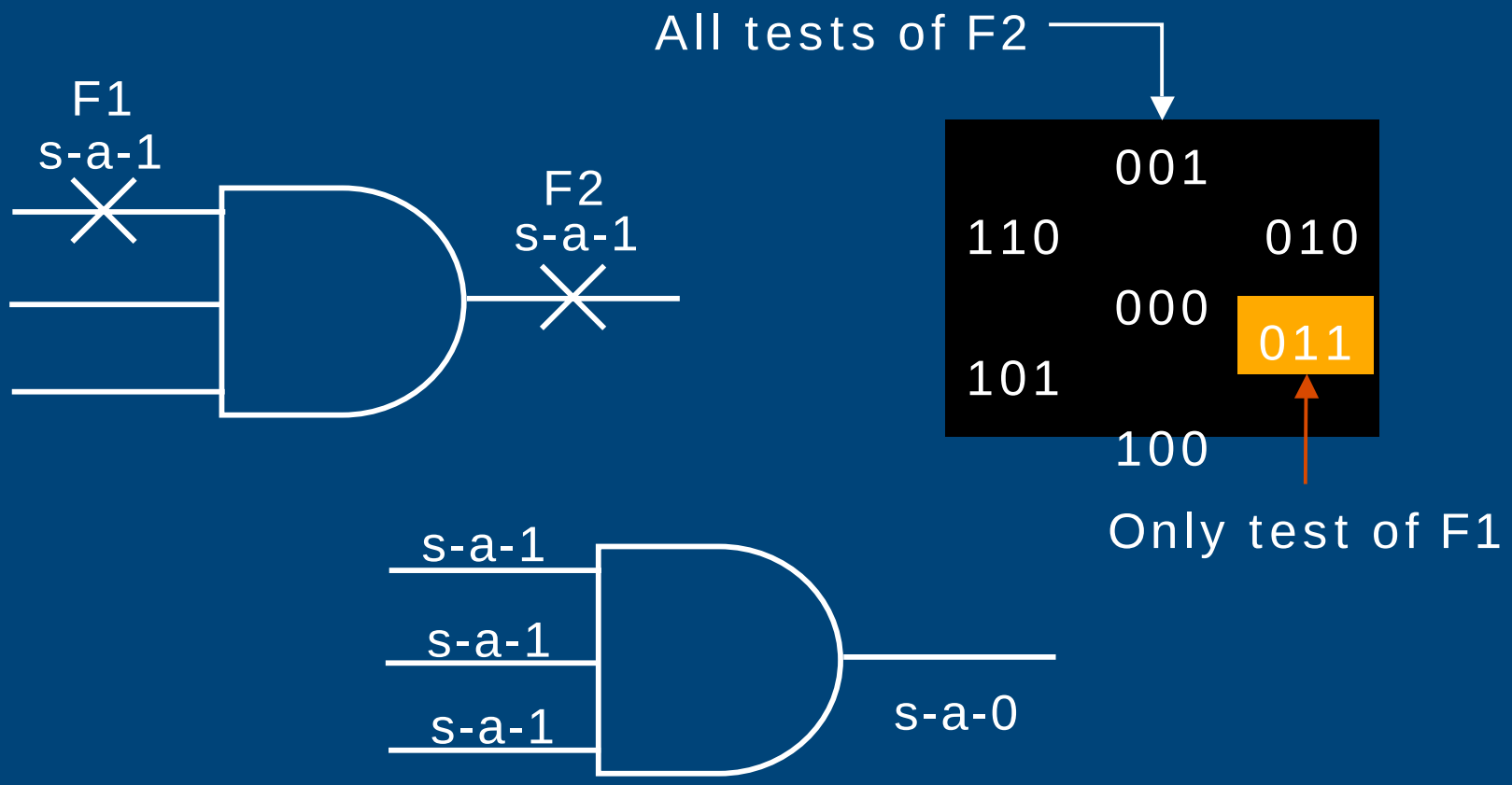
Dominance Example

Dominance Example



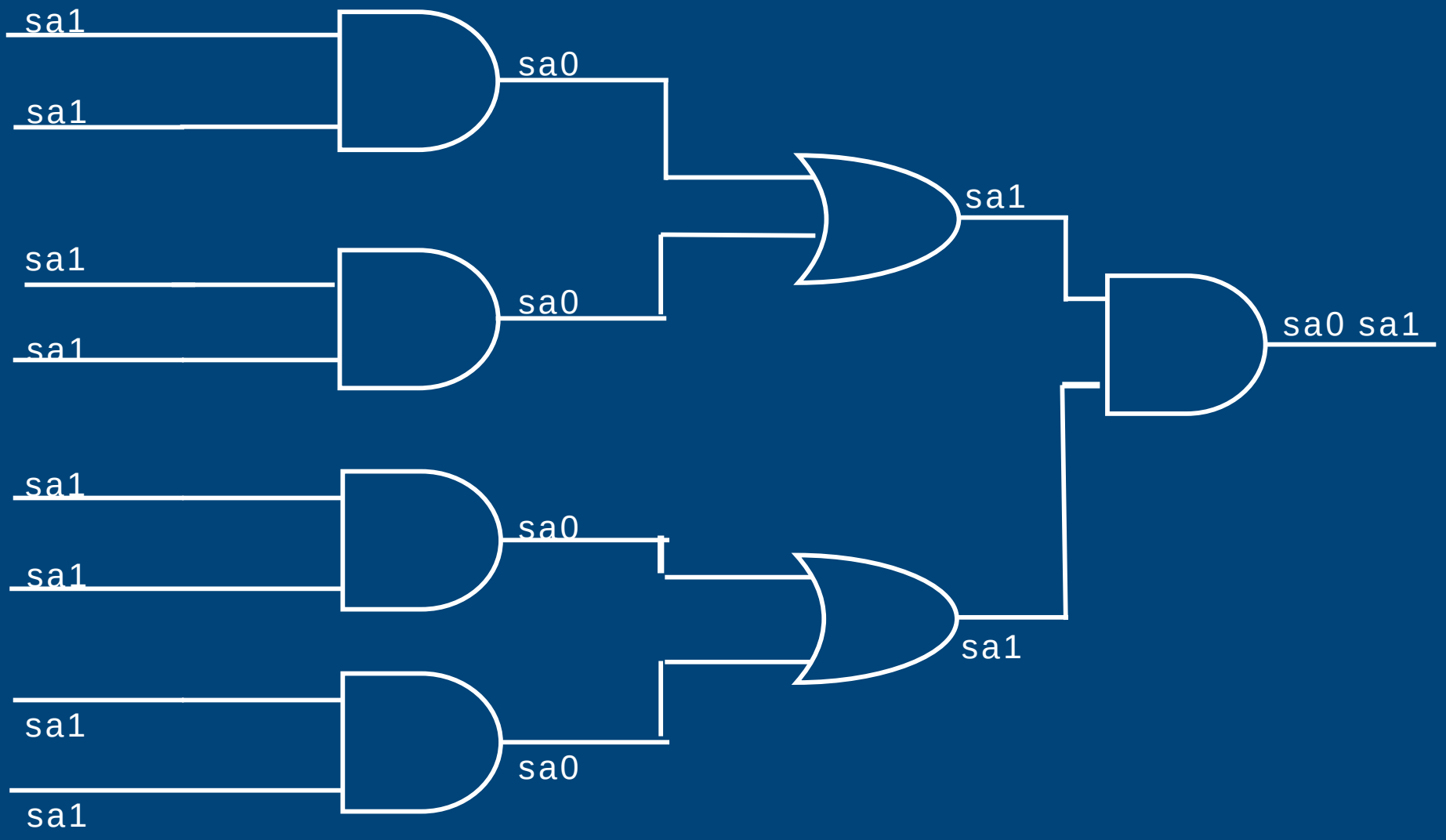


Dominance Example



A dominance collapsed fault set

Dominance Example



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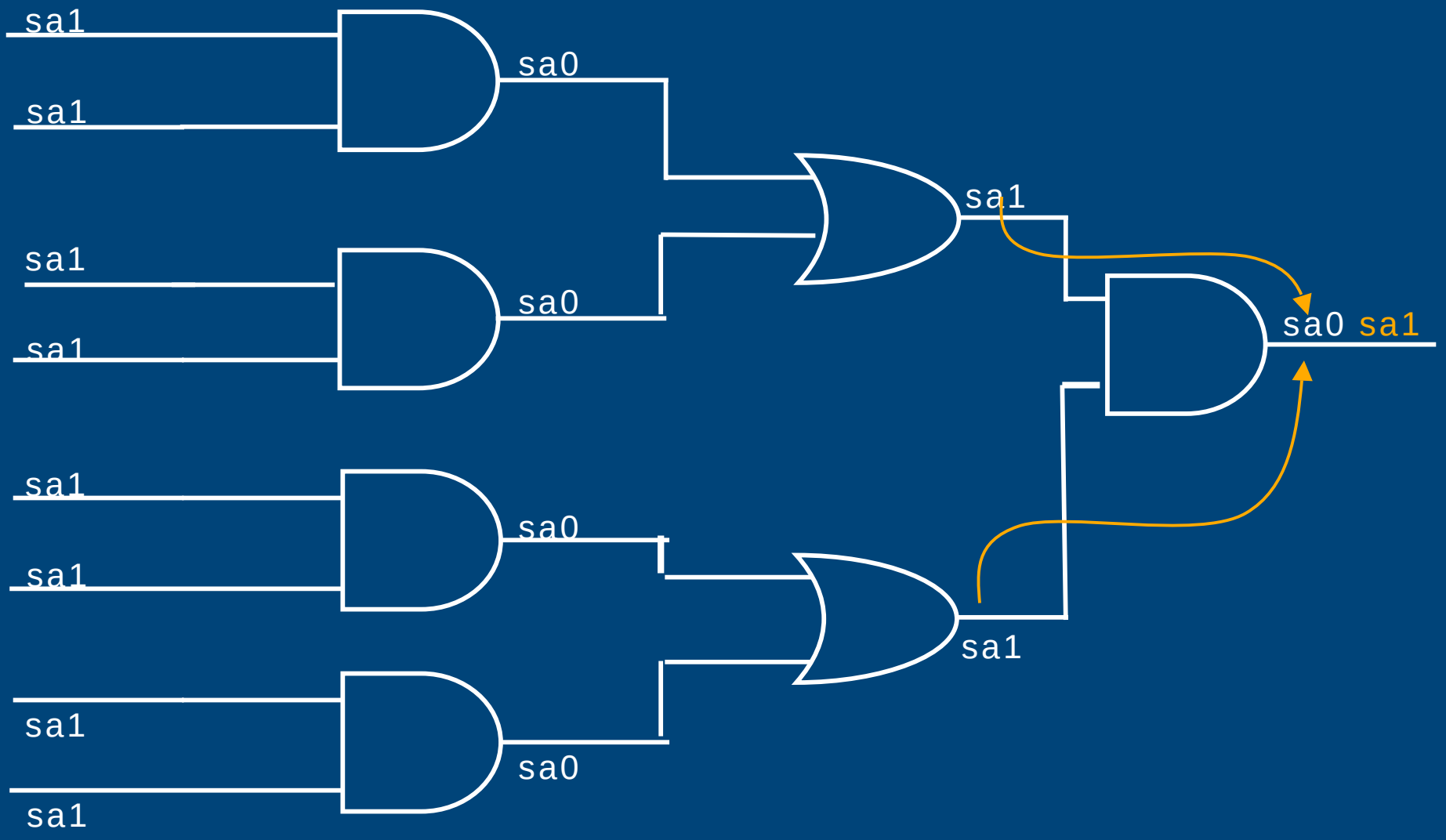

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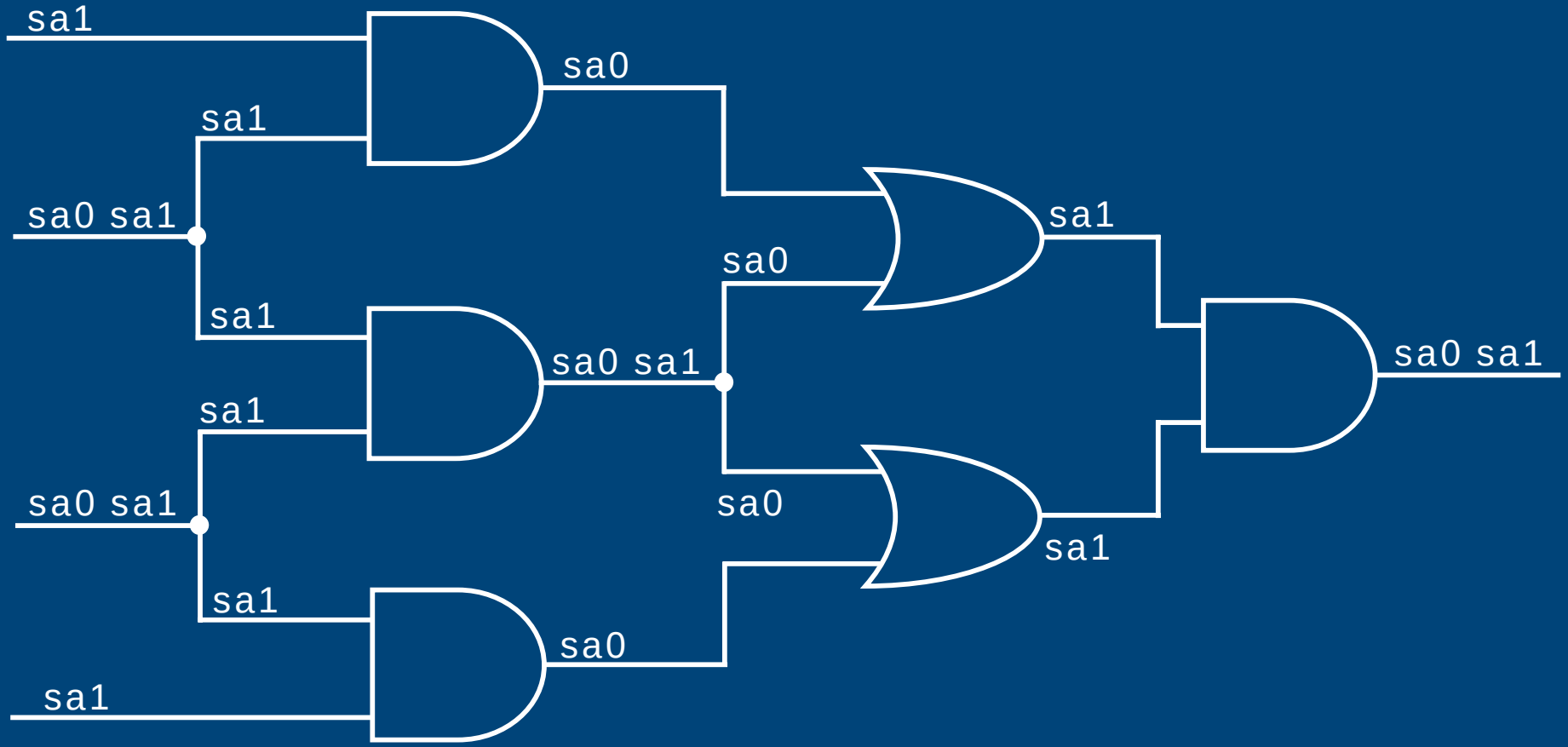

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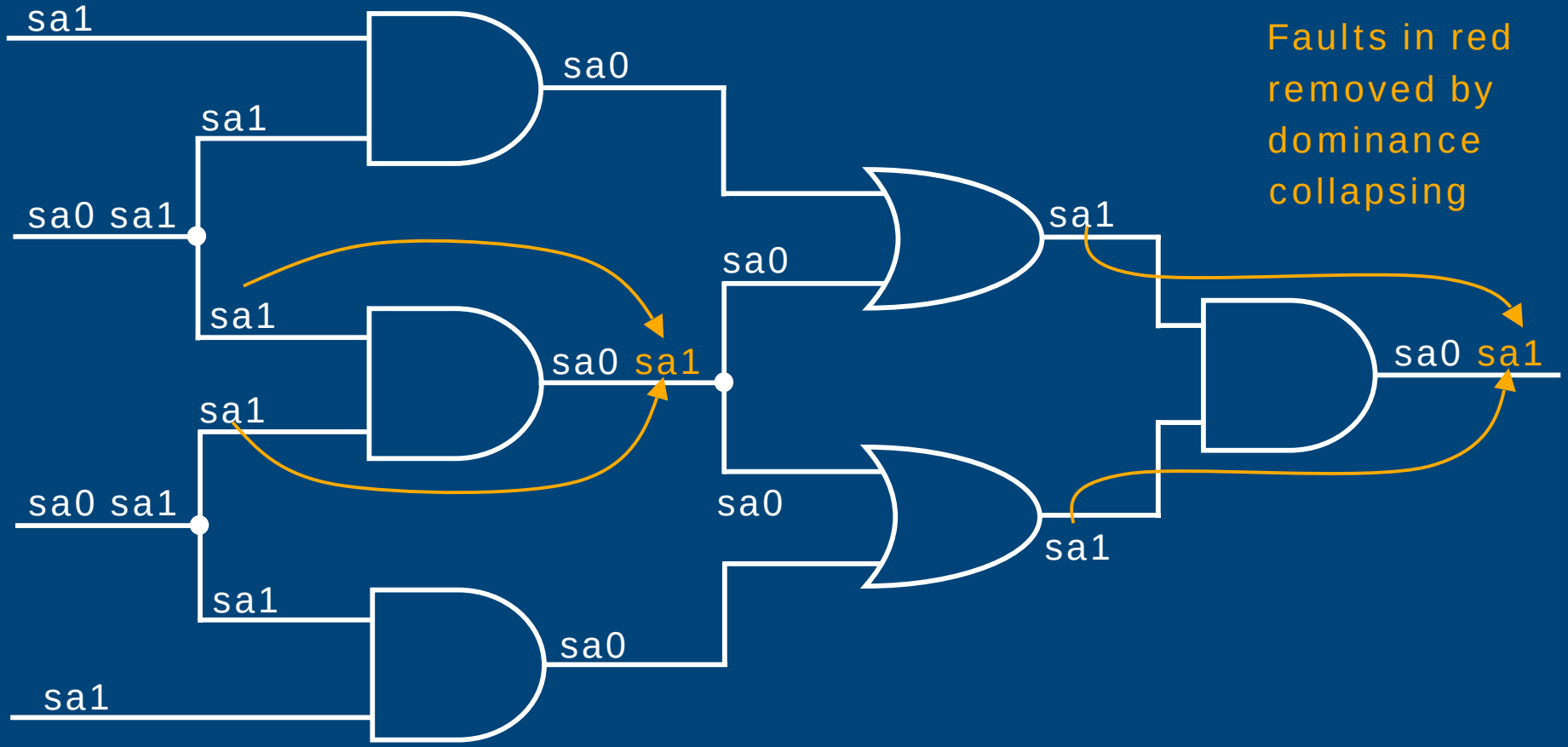
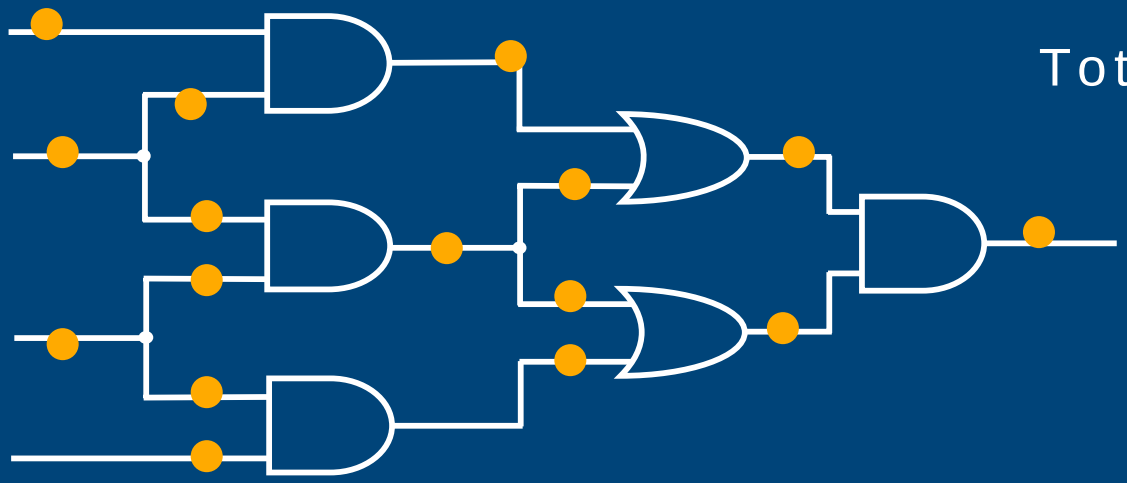


Checkpoints

- Primary inputs and fanout branches of a combinational circuit are called *checkpoints*.



Total fault sites = 16

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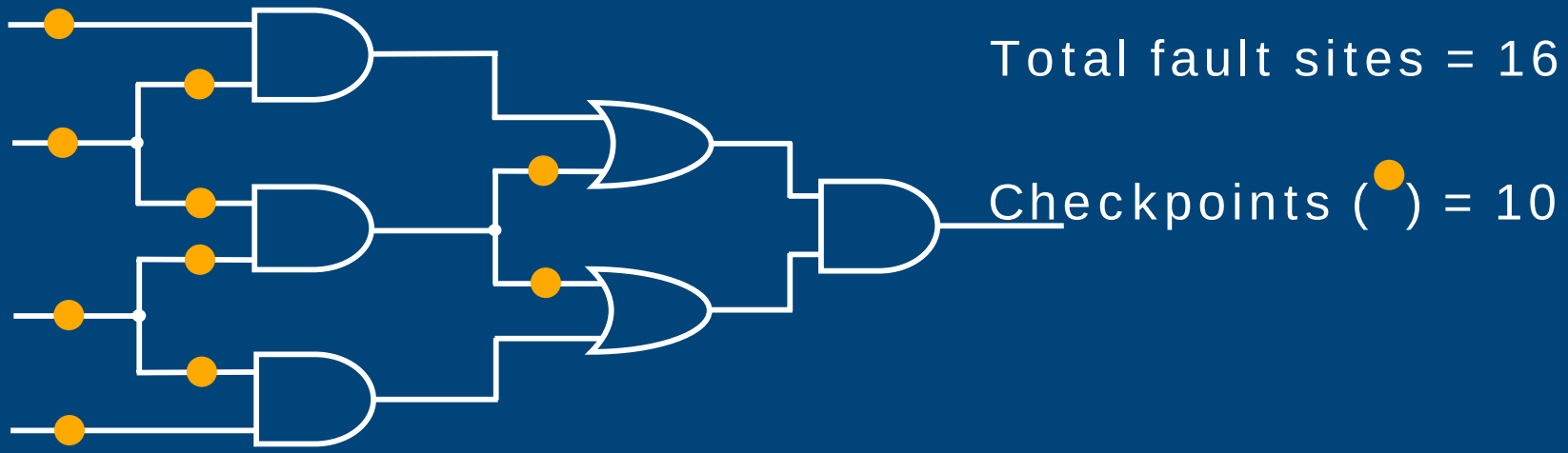

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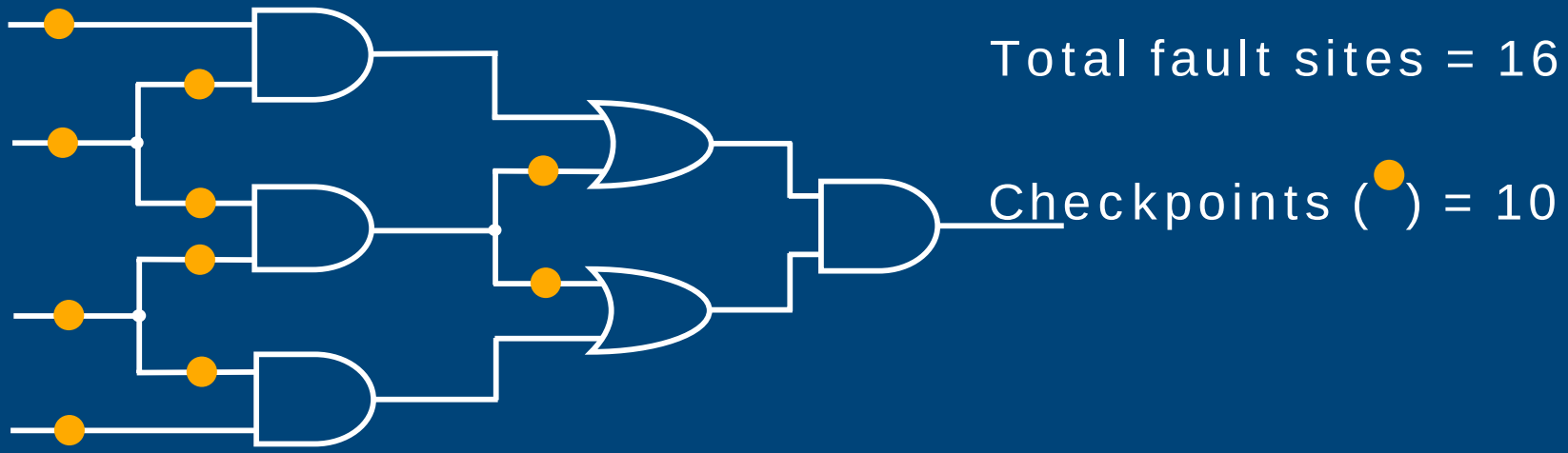
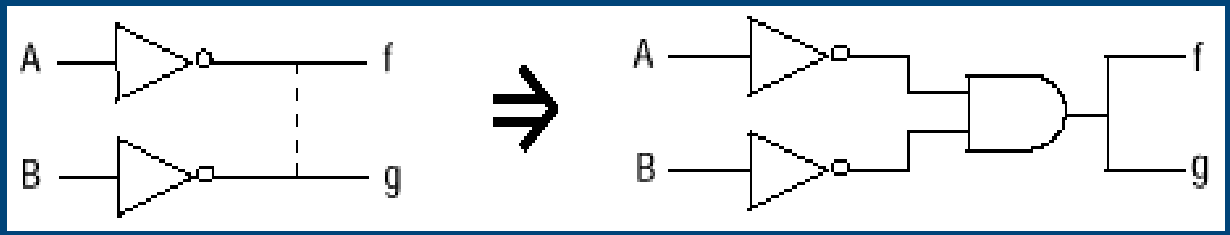


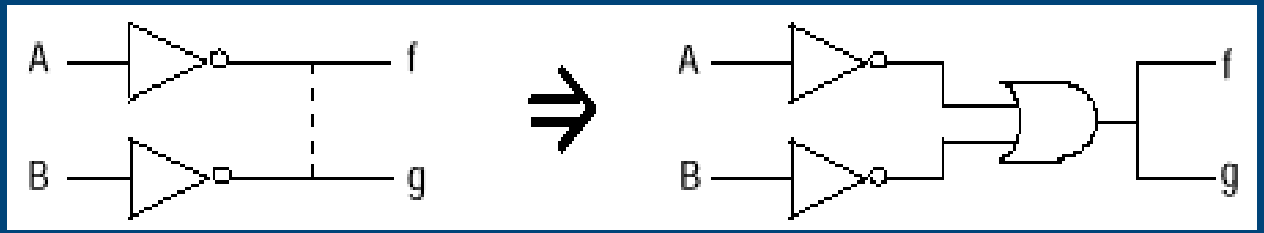
Checkpoint theorem: A test set that detects all single (multiple) stuck-at faults on all checkpoints of a combinational circuit, also detects all single (multiple) stuck-at faults in that circuit.

Bridging Faults

- Two or more normally distinct points (lines) are shorted together
  - Logic effect depends on technology
  - Wired- AND for TTL

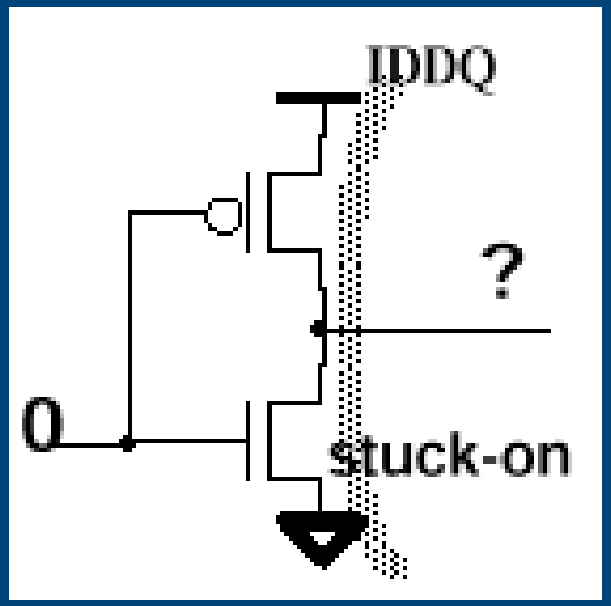


  - Wired- OR for ECL



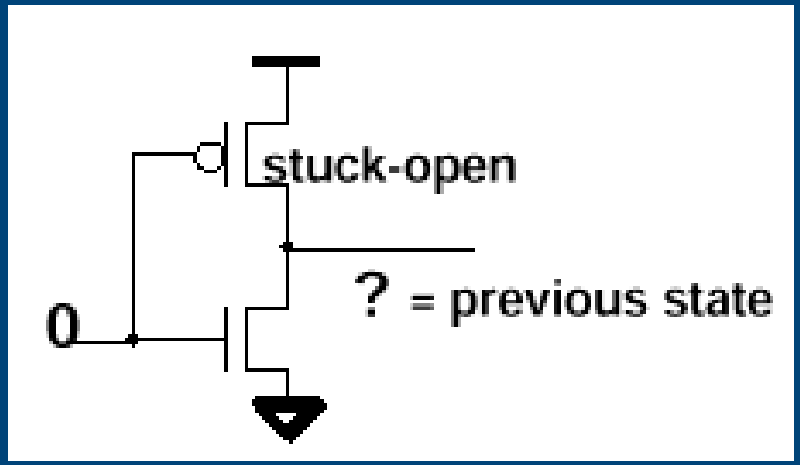
  - CMOS?

CMOS Transistor Stuck- Short



- Transistor stuck- on may cause ambiguous logic level
  - depends on the relative impedances of the pull- up & pull- down networks
- When input is low, both P and N transistors are conducting causing increased quiescent current, called IDDQ fault.

CMOS Transistor Stuck- OPEN



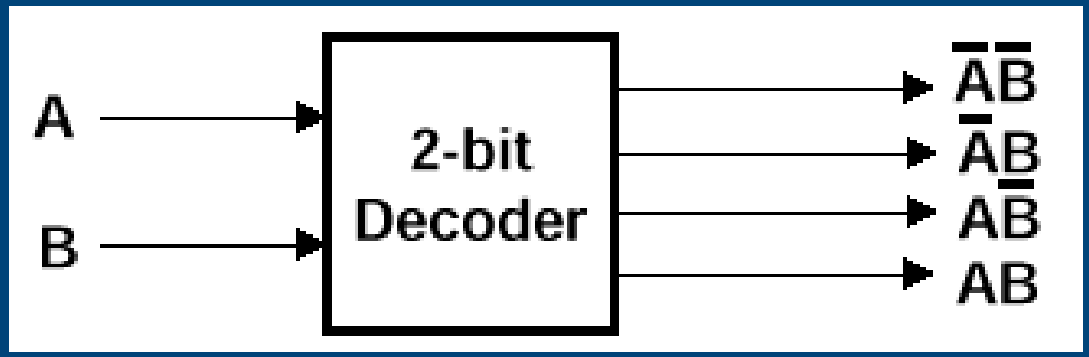
- Transistor stuck- open may cause output floating.

Functional Faults

- Fault effects modeled at a higher level than logic for function modules, such as
  - Decoders
  - Multiplexers
  - Adders
  - Counters
  - RAMs
  - ROMs

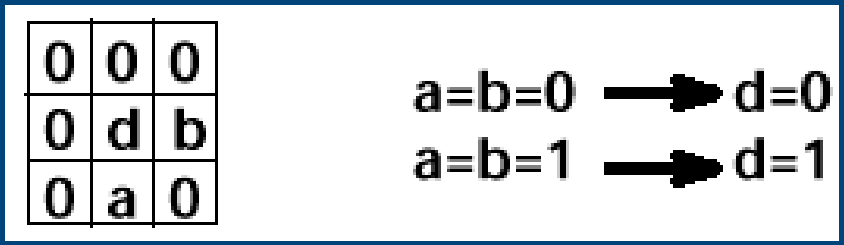
Functional Faults of Decoder

- f(L i /L j): Instead of line L i , Line L j is selected
- f(L i /L i +L j): In addition to L i , L j is selected
- f(L i /0): None of the lines are selected



Memory Faults

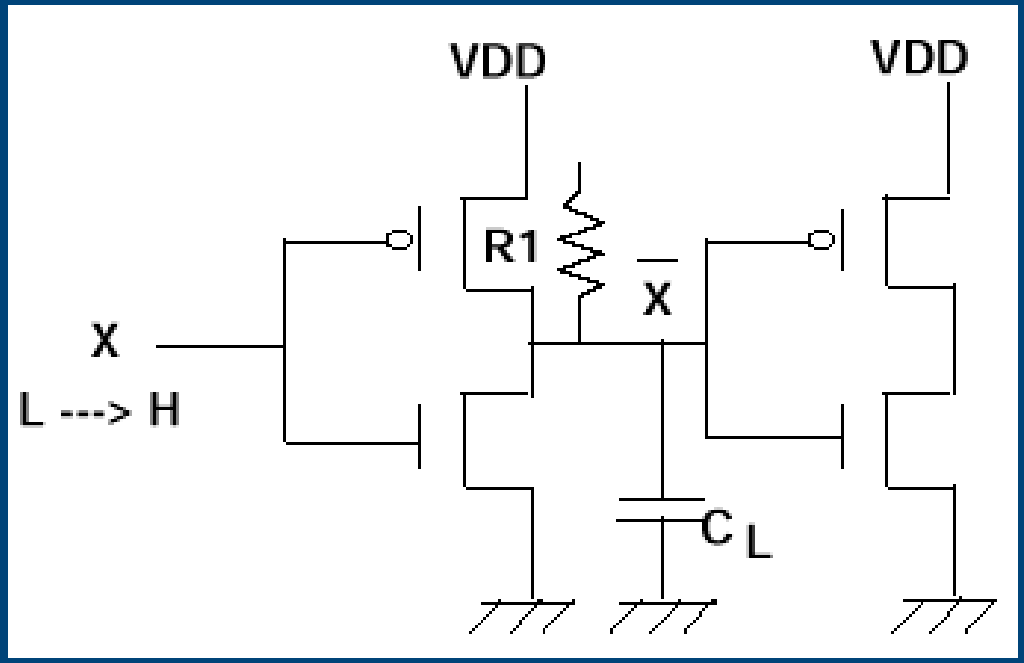
- Pattern- sensitive faults: the presence of a faulty signal depends on the signal values of the nearby points
  - Most common in DRAMs



- Adjacent cell coupling faults
  - Pattern sensitivity between a pair of cells

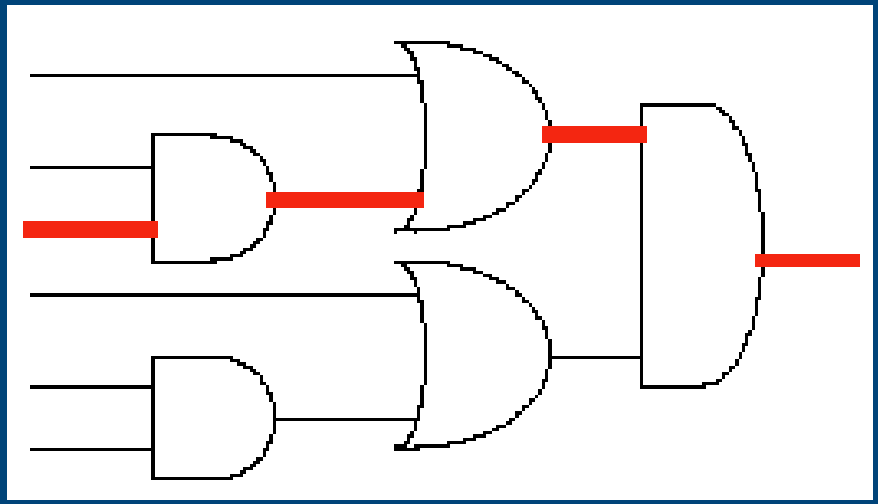
Gate- Delay- Fault

- Slow to rise, slow to fall
  - x is slow to rise when channel resistance R1 is abnormally high



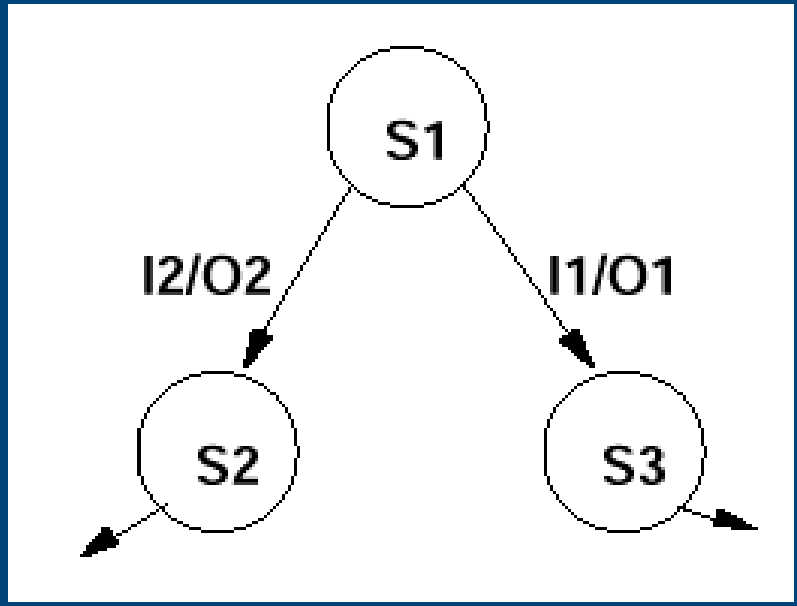
Path- Delay- Fault

- Propagation delay of the path exceeds the clock interval.
- The number of paths grows exponentially with the number of gates.



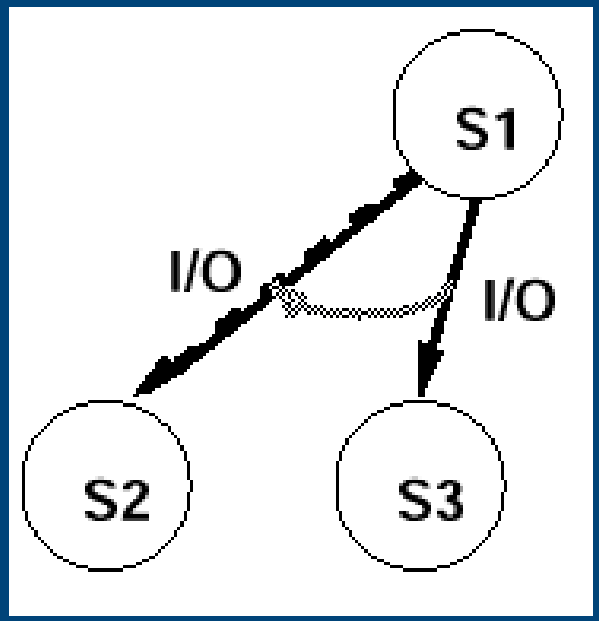
State Transition Graph

- Each state transition is associated with a 4-tuple:
  - source state, input, output, destination state



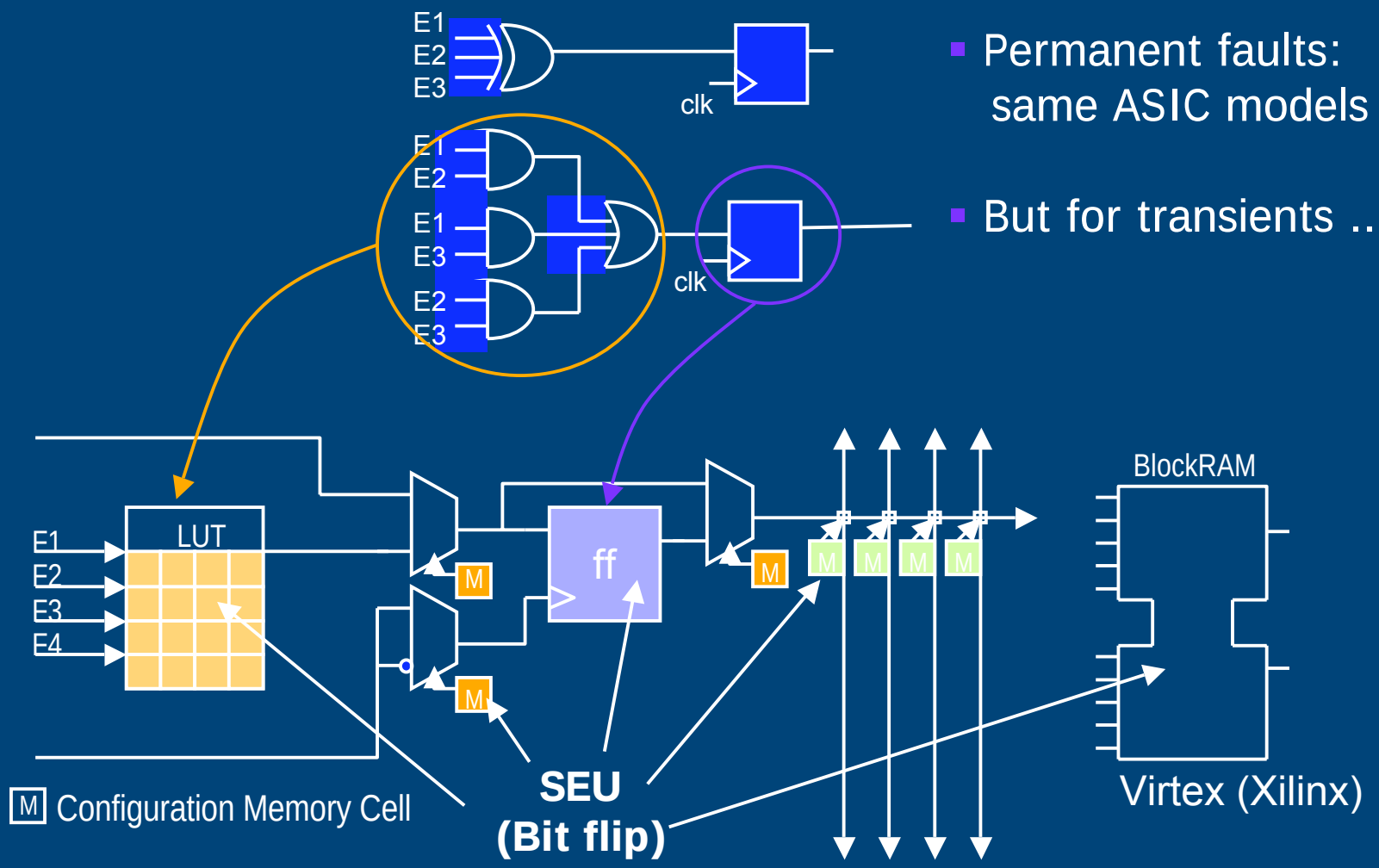
Single State Transition Fault Model

- A fault causes a single state transition to a wrong destination state.



Faults in FPGAs

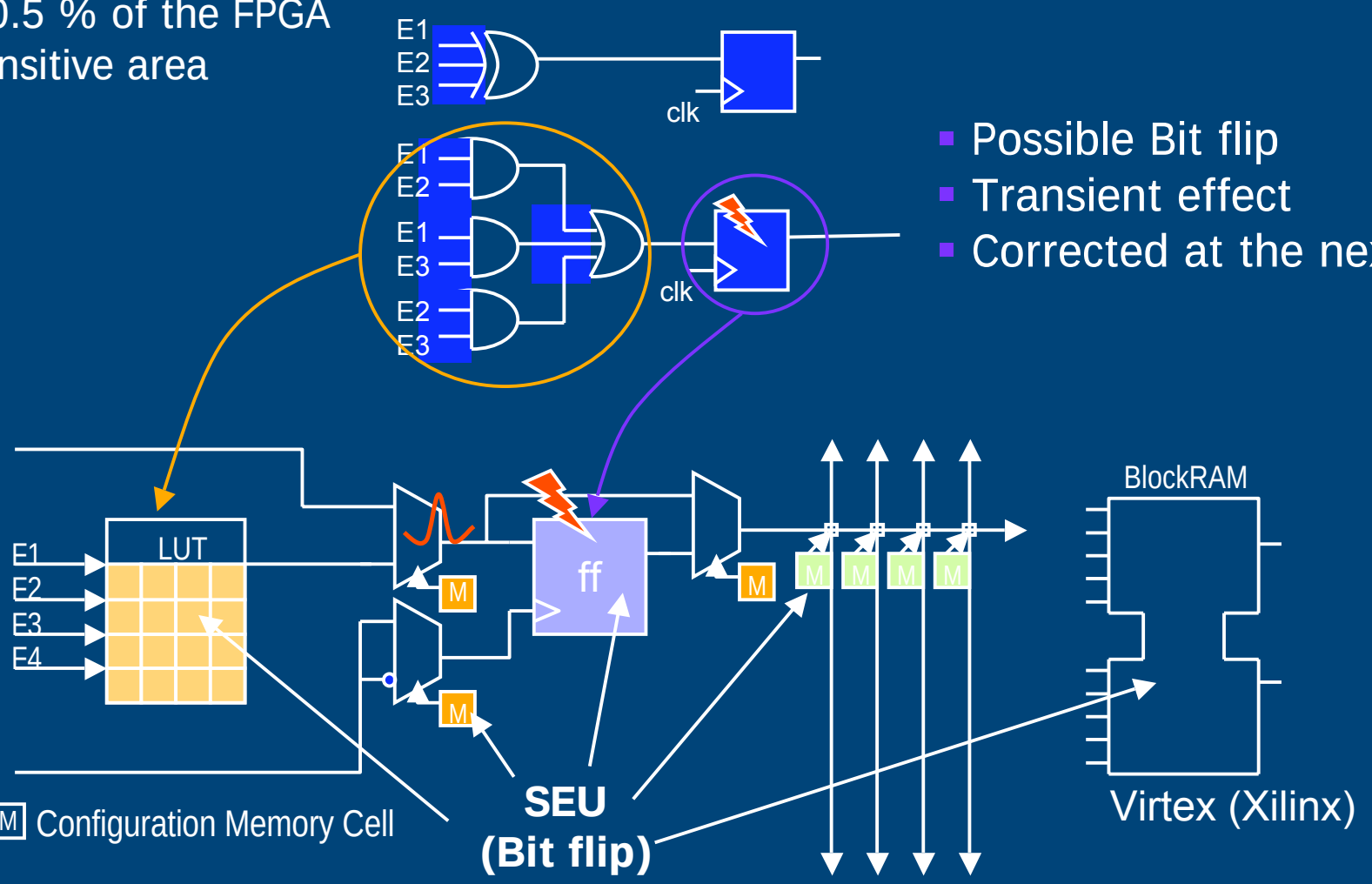
FPGA building blocks:



- Permanent faults: same ASIC models apply
- But for transients ...

Effect of Transients in SRAM-based FPGAs

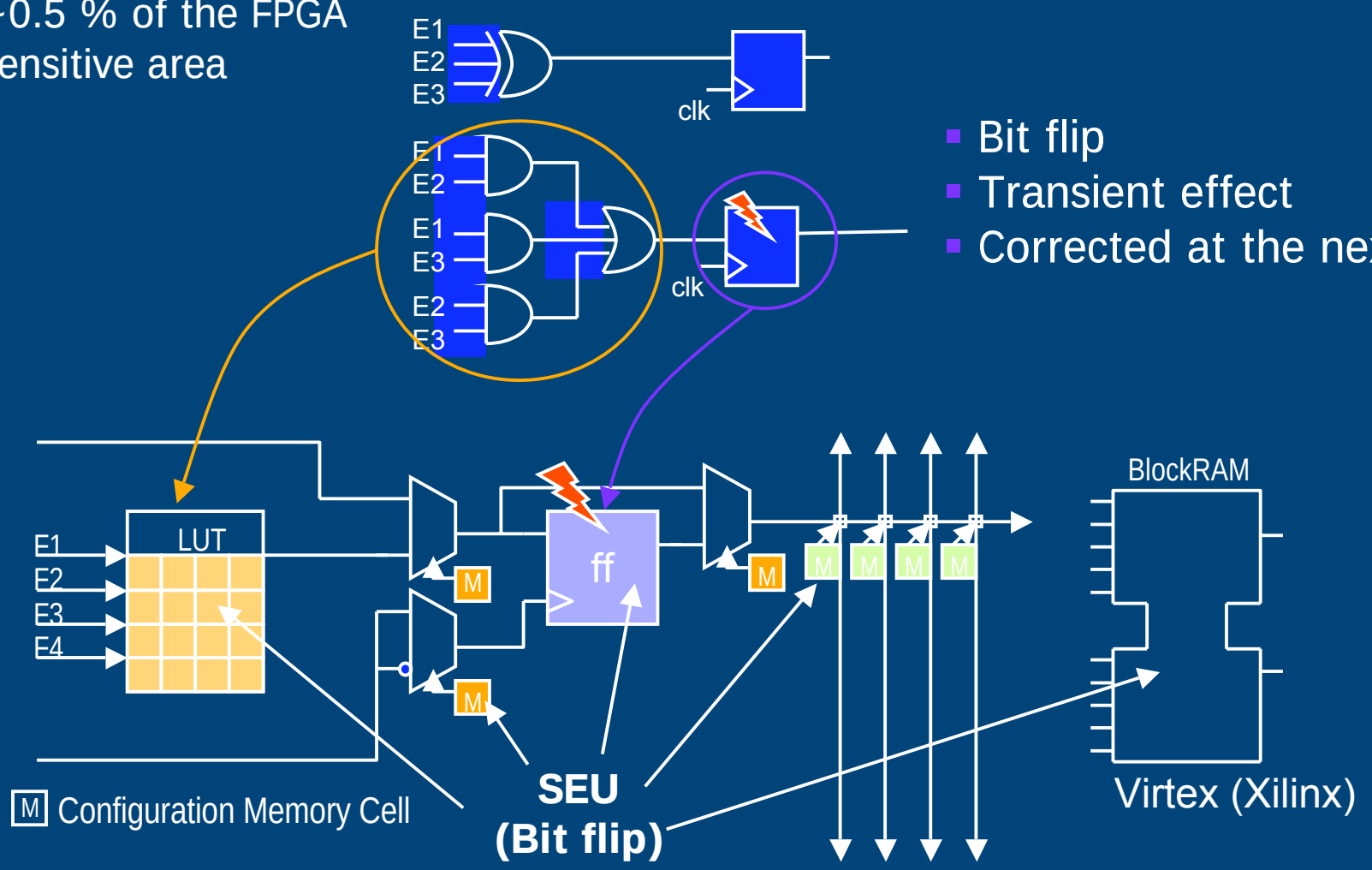
CLB Comb. Logic:
~0.5 % of the FPGA sensitive area



- Possible Bit flip
- Transient effect
- Corrected at the next load

Effect of Transients in SRAM-based FPGAs

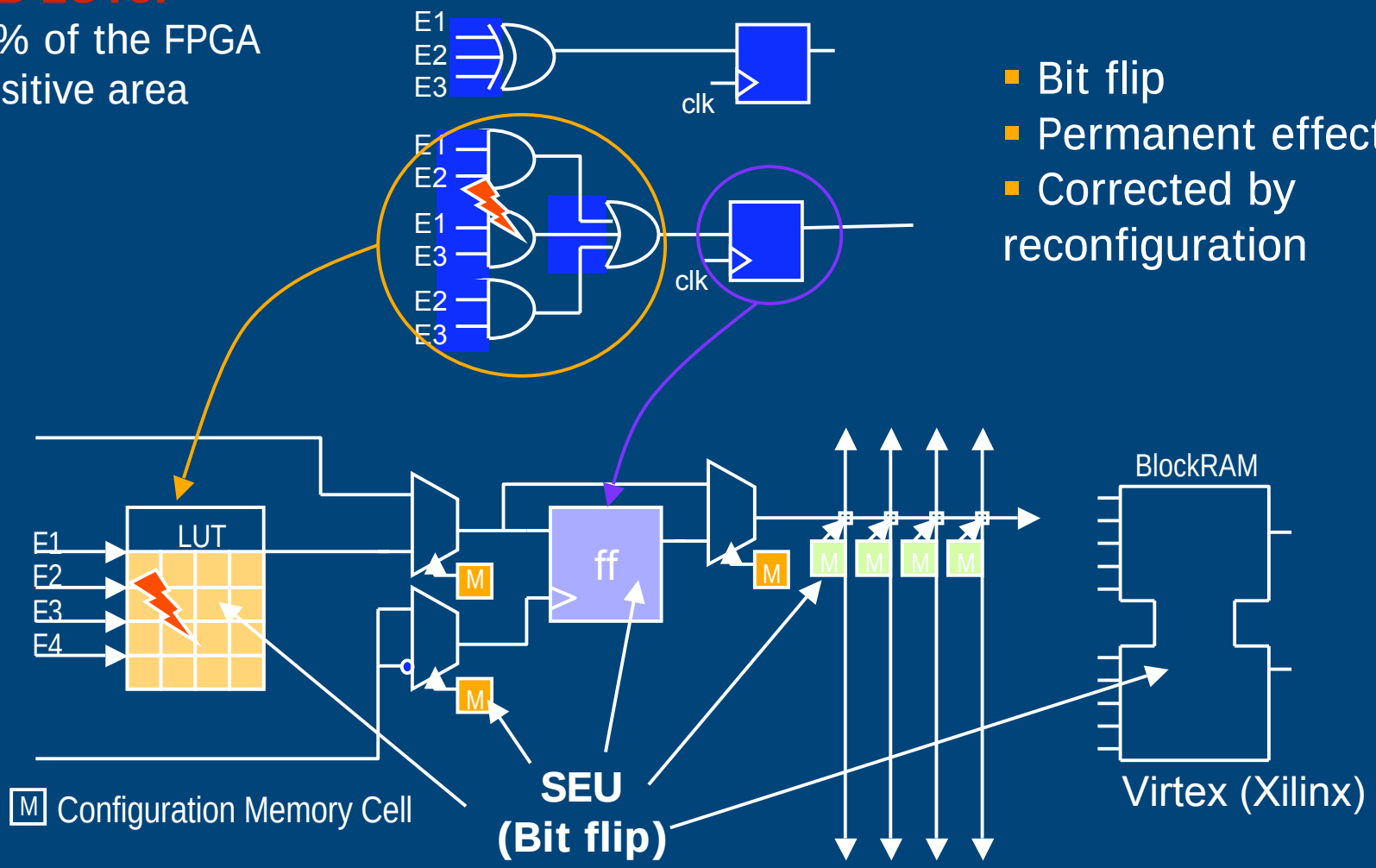
CLB Flip-flops:
~0.5 % of the FPGA sensitive area



- Bit flip
- Transient effect
- Corrected at the next load

Effect of Transients in SRAM-based FPGAs

CLB LUTs:
~8% of the FPGA sensitive area

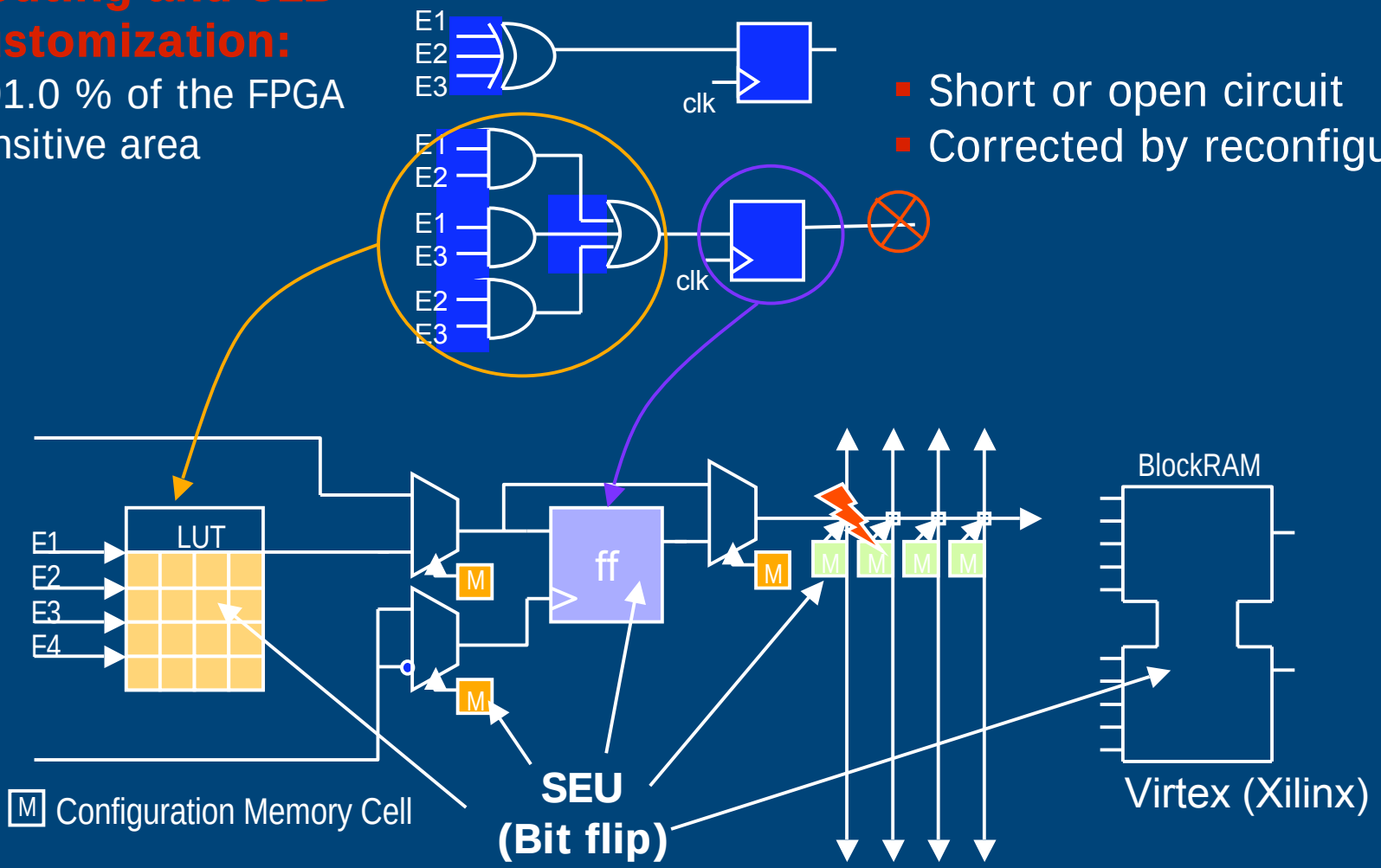


- Bit flip
- Permanent effect
- Corrected by reconfiguration

Effect of Transients in SRAM-based FPGAs

Routing and CLB customization:

~91.0 % of the FPGA sensitive area



- Short or open circuit
- Corrected by reconfiguration

Summary

- Fault models are analyzable approximations of defects and are essential for a test methodology.
- For digital logic single stuck-at fault model offers best advantage of tools and experience.
- Many other faults (bridging, stuck-open and multiple stuck-at) are largely covered by stuck-at fault tests.
- Stuck-short and delay faults are technology-dependent faults and require special tests.
- Memory and analog circuits need other specialized fault models and tests.
- Transient faults may have permanent effects in FPGAs