

MIC05: Teste de Circuitos Integrados

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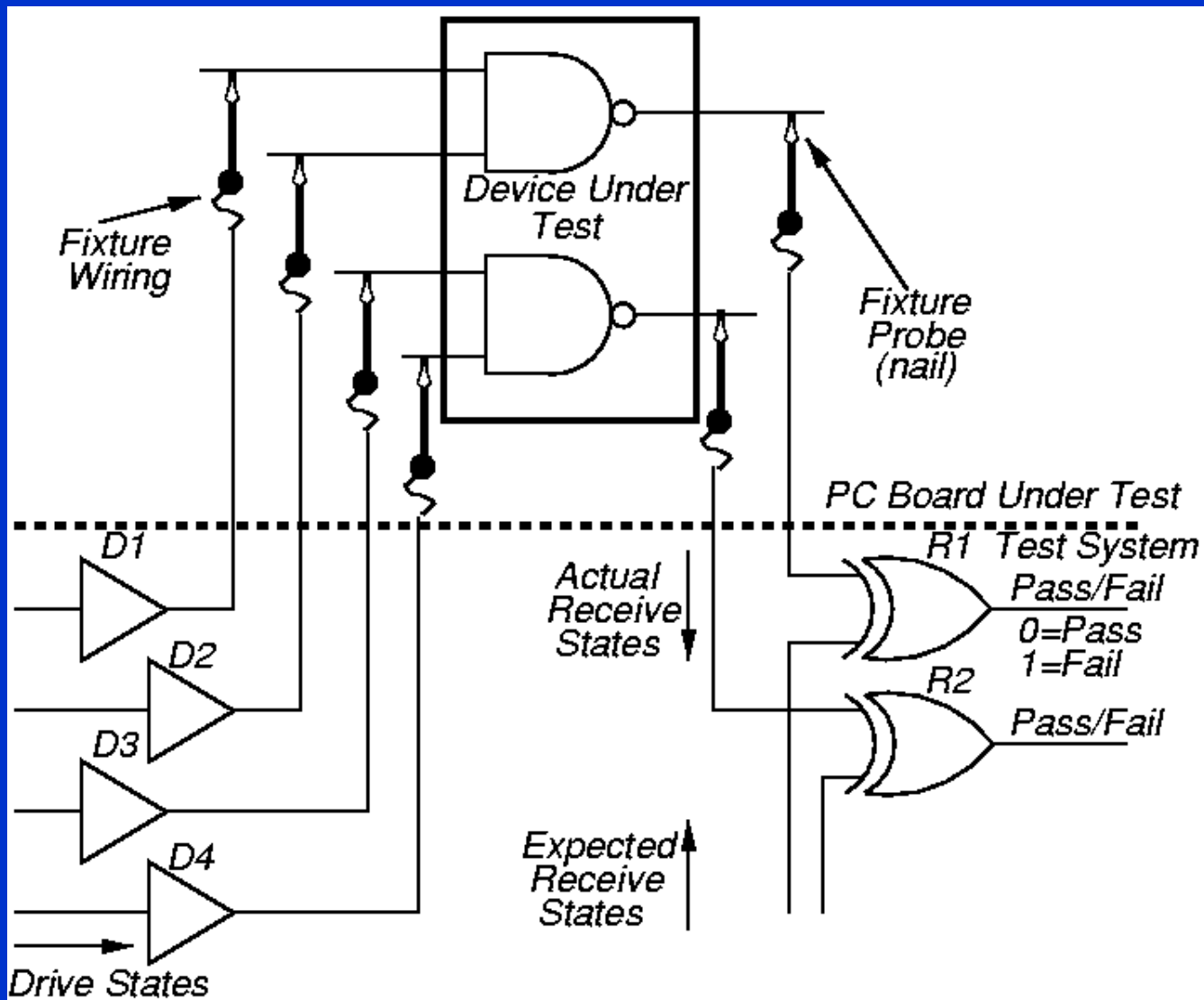
IEEE 1149.1 JTAG Boundary Scan Standard

- **Motivation**
- **Bed-of-nails tester**
- **System view of boundary scan hardware**
- **Elementary *scan cell***
- ***Test Access Port (TAP)* controller**
- ***Boundary scan* instructions**
- **Summary**

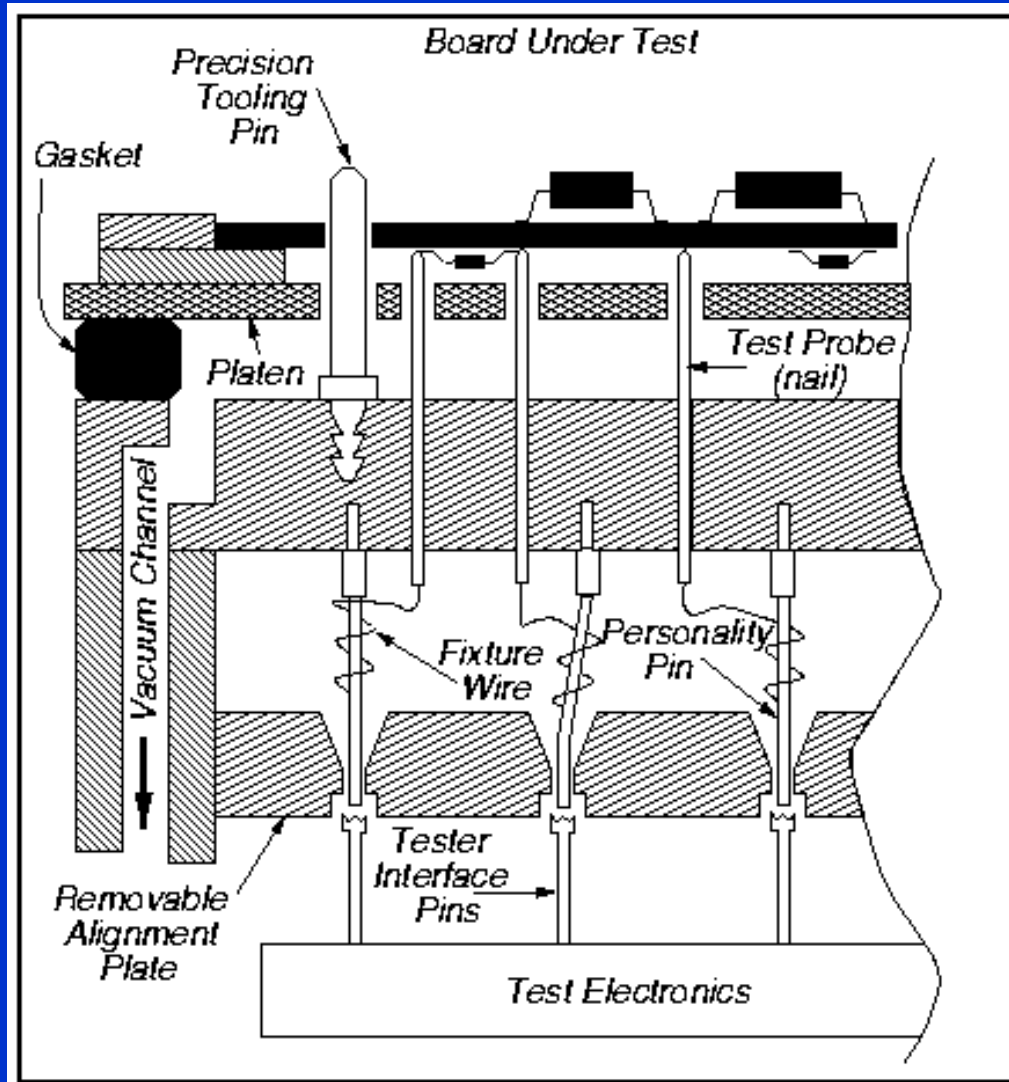
Motivation for Standard

- ***Bed-of-nails printed circuit board* tester gone**
 - **We put components on both sides of PCB & replaced DIPs with flat packs to reduce inductance**
 - **Nails would hit components**
 - **Reduced spacing between PCB wires**
 - **Nails would short the wires**
 - **Need standard System Test Port and Bus**
 - **Integrate components from different vendors**
 - **Test bus identical for various components**
 - **One chip has test hardware for other chips**

Bed-of-Nails Tester Concept



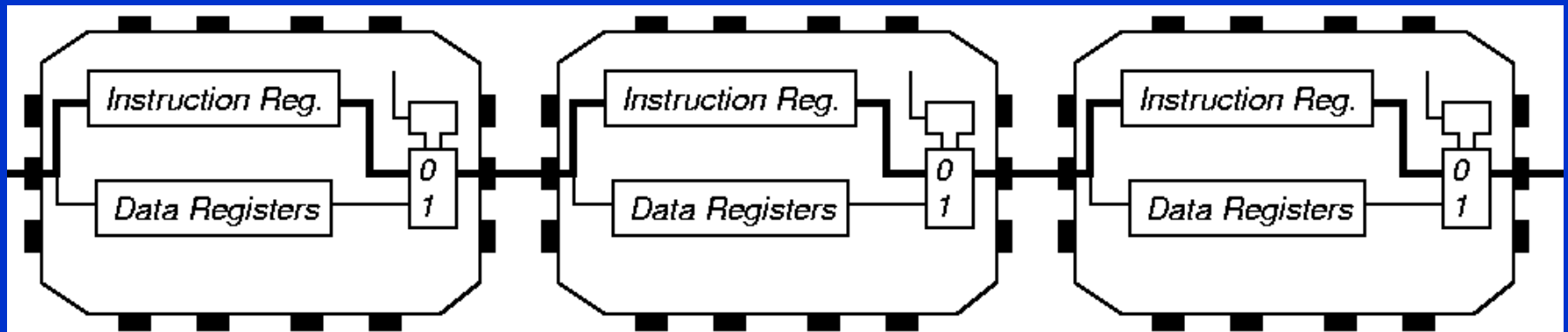
Bed-of-Nails Tester



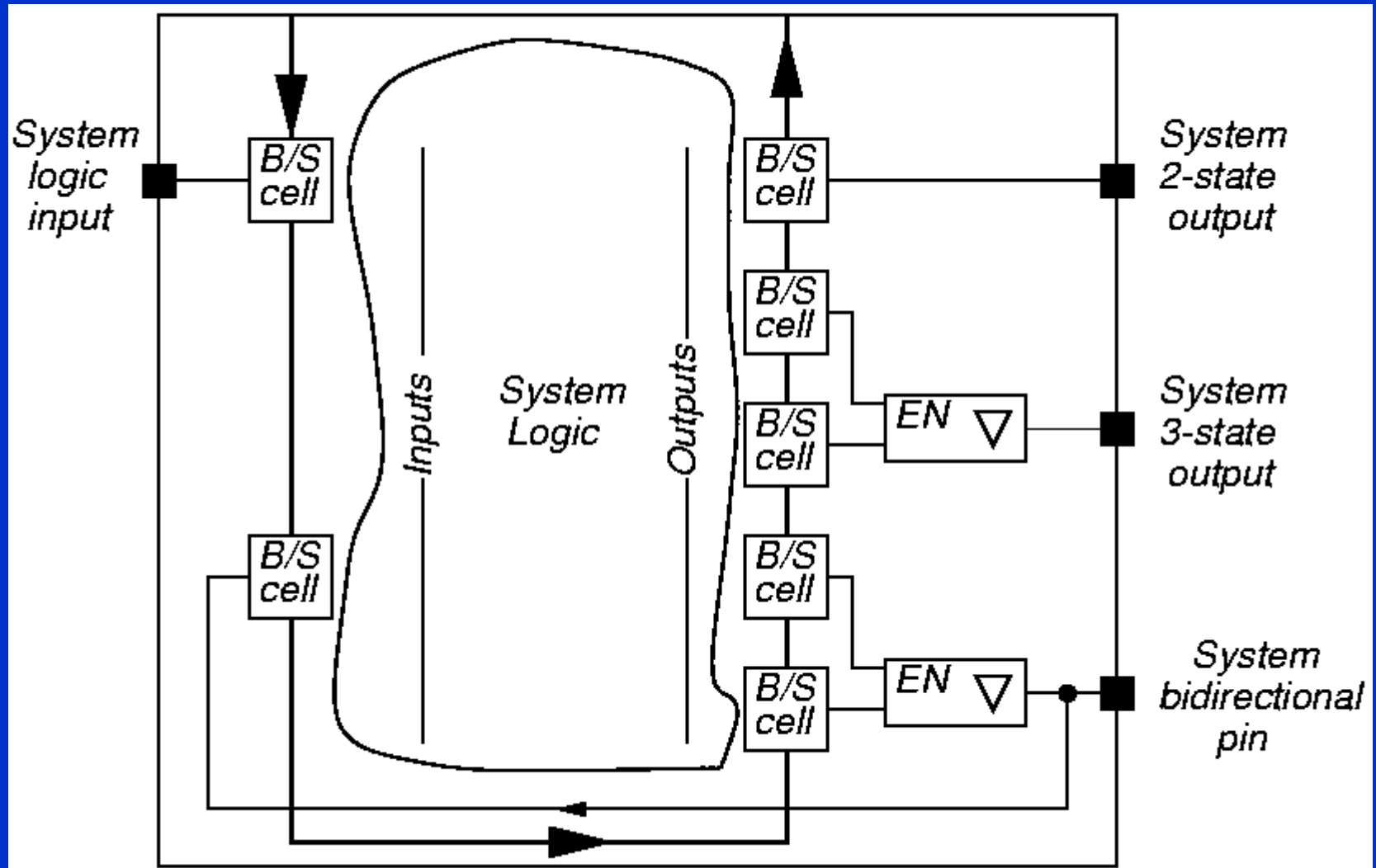
Purpose of Standard

- Lets test instructions and test data be serially fed into a *component-under-test* (CUT)
 - Allows reading out of test results
- JTAG can operate at chip, PCB, & system levels
- Allows control of tri-state signals during testing
- Lets other chips collect responses from CUT
- Lets system interconnect be tested separately from components
- Lets components be tested separately from wires

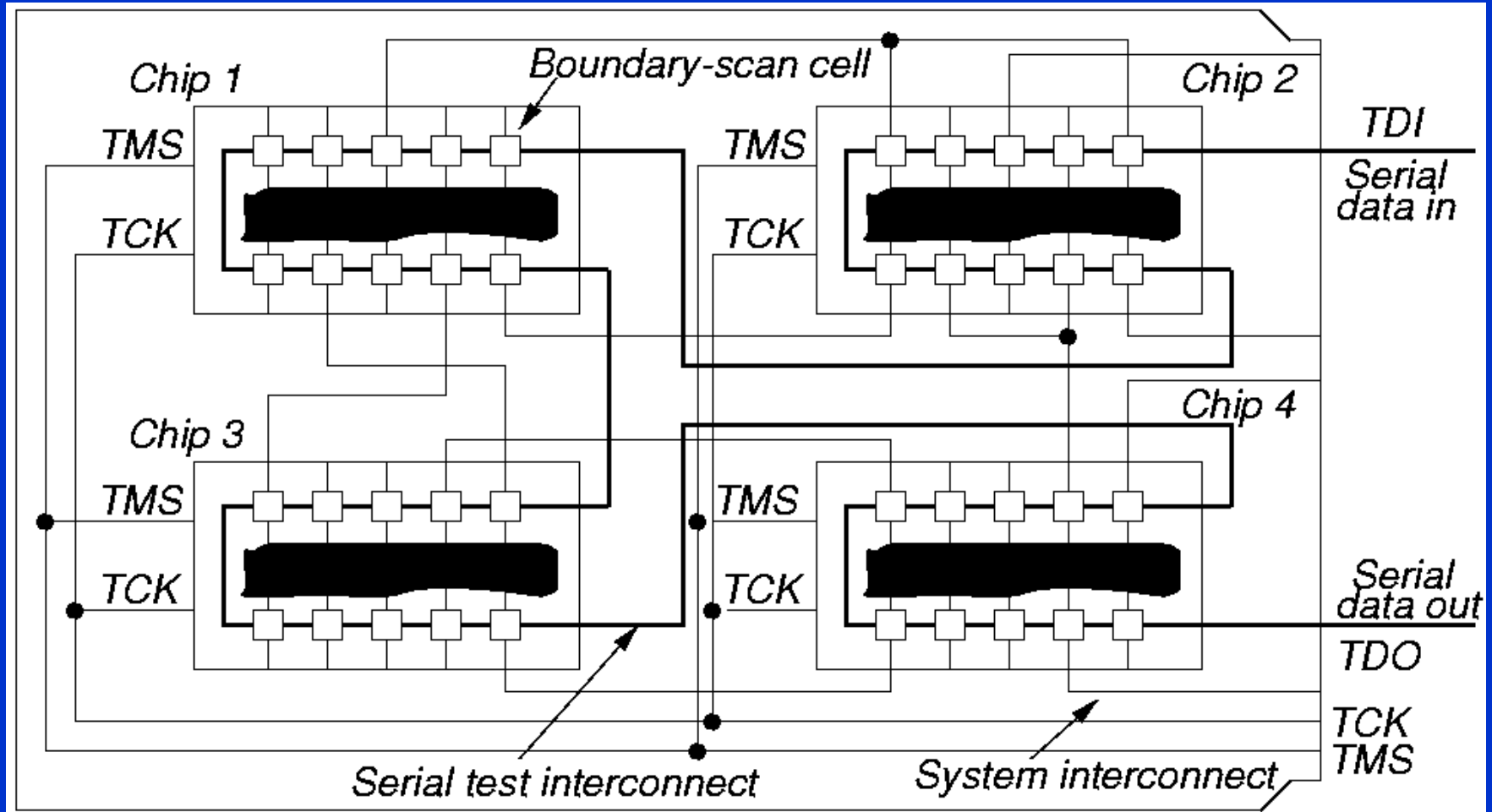
Instruction Register Loading with JTAG



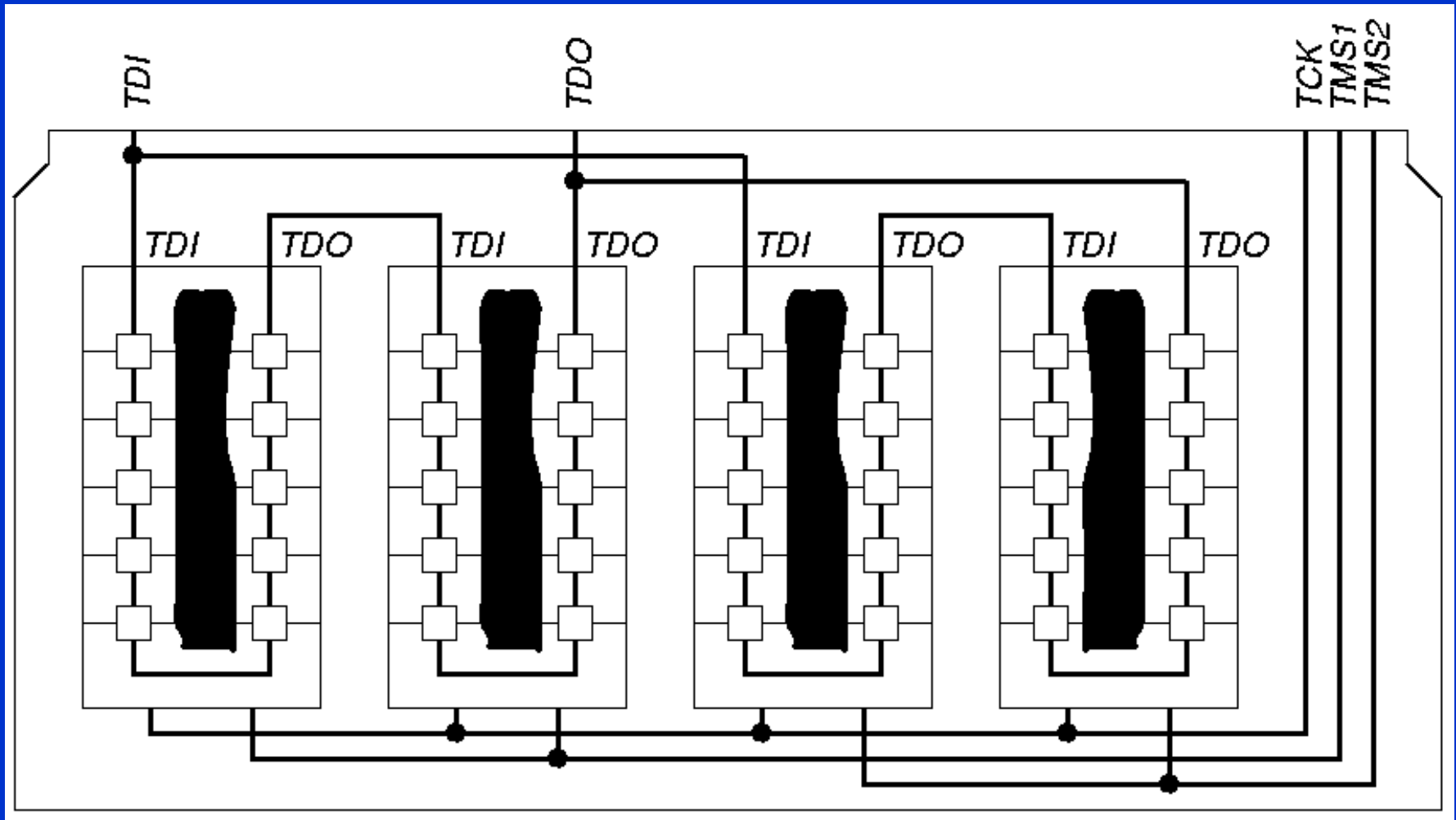
Boundary Scan Chain View



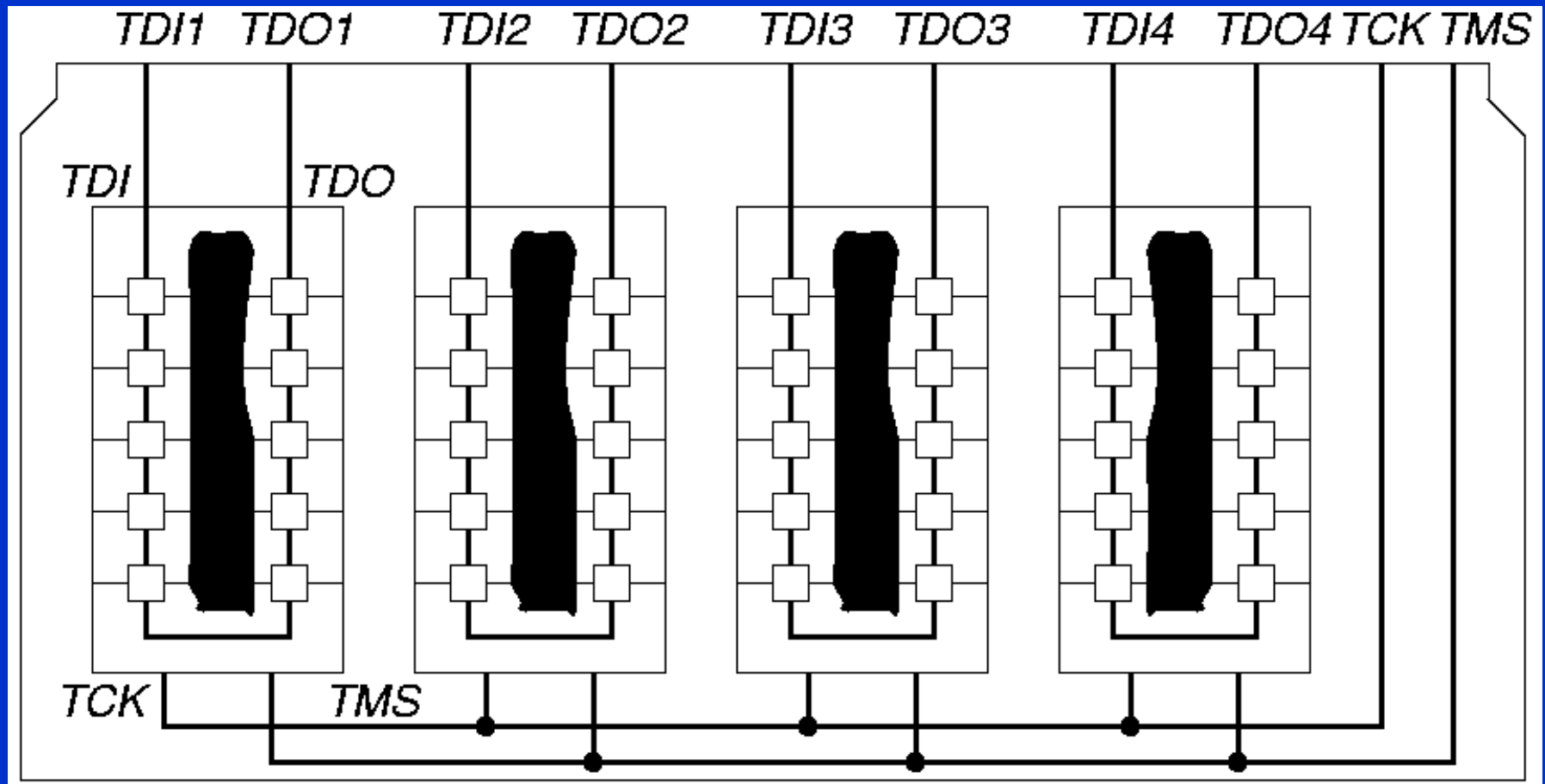
Serial Board / MCM Scan



Parallel Board / MCM Scan



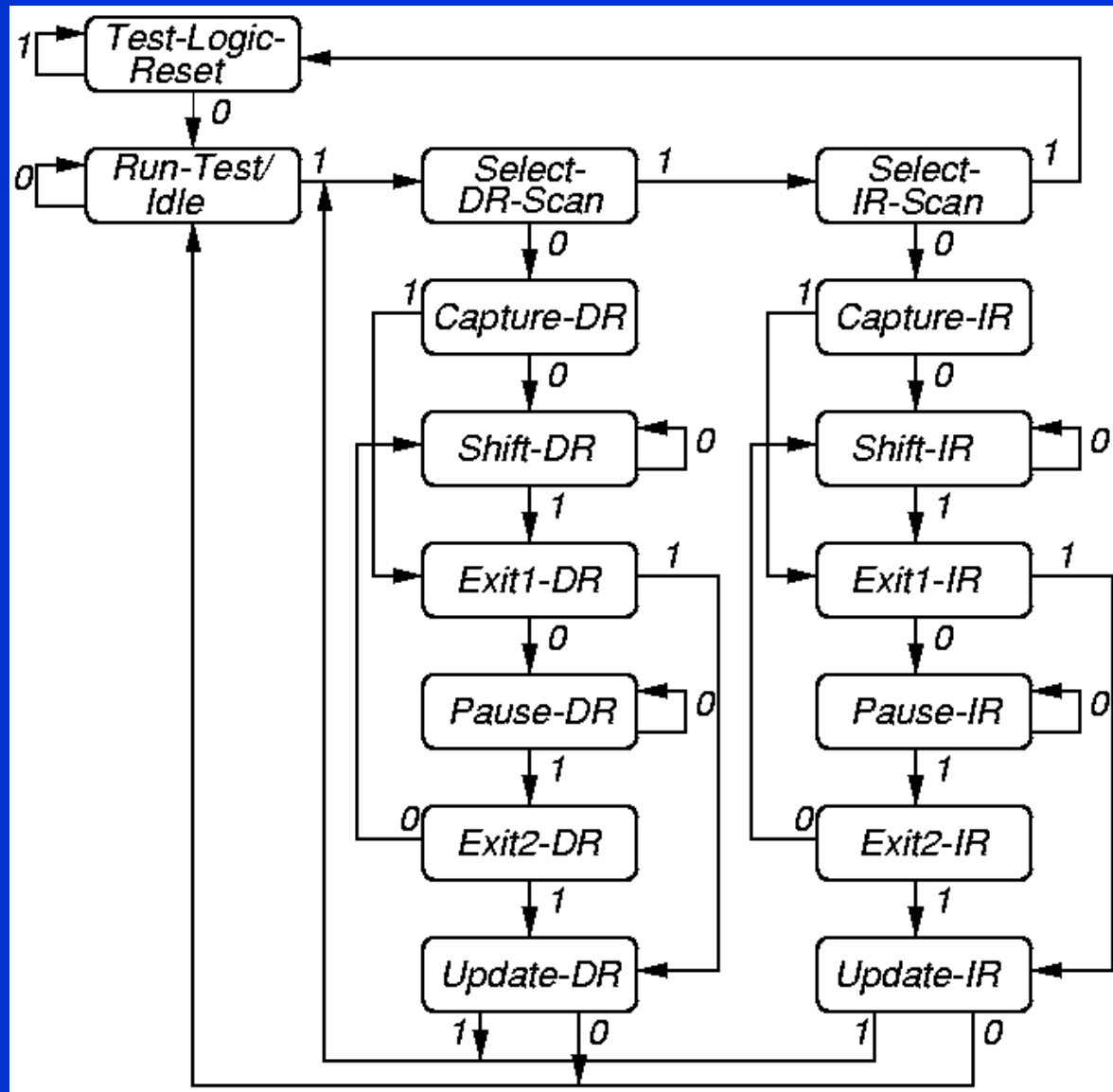
Independent Path Board / MCM Scan



Tap Controller Signals

- **Test Access Port (TAP) includes these signals:**
 - **Test Clock Input (TCK)** -- Clock for test logic
 - Can run at different rate from system clock
 - **Test Mode Select (TMS)** -- Switches system from functional to test mode
 - **Test Data Input (TDI)** -- Accepts serial test data and instructions -- used to shift in vectors or one of many test instructions
 - **Test Data Output (TDO)** -- Serially shifts out test results captured in boundary scan chain (or device ID or other internal registers)

Tap Controller State Diagram



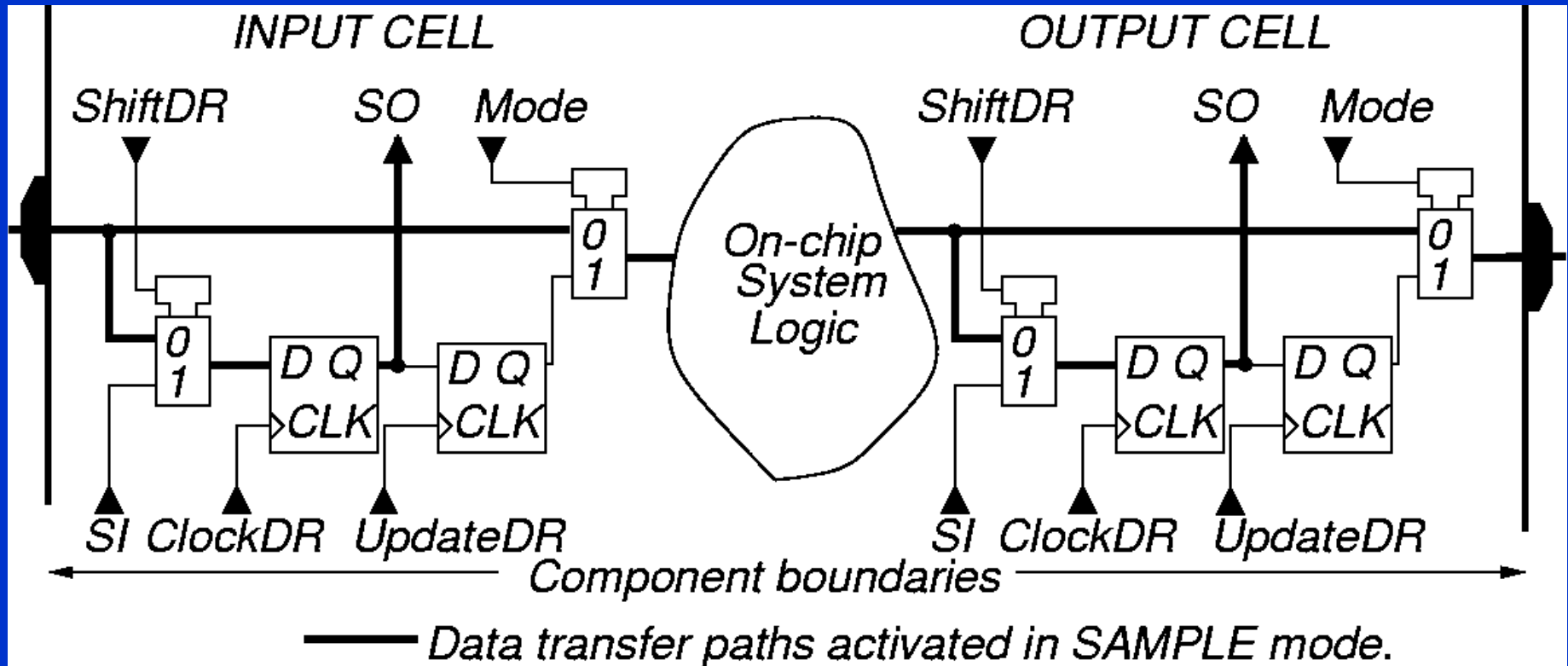
Boundary Scan Instructions

SAMPLE / PRELOAD

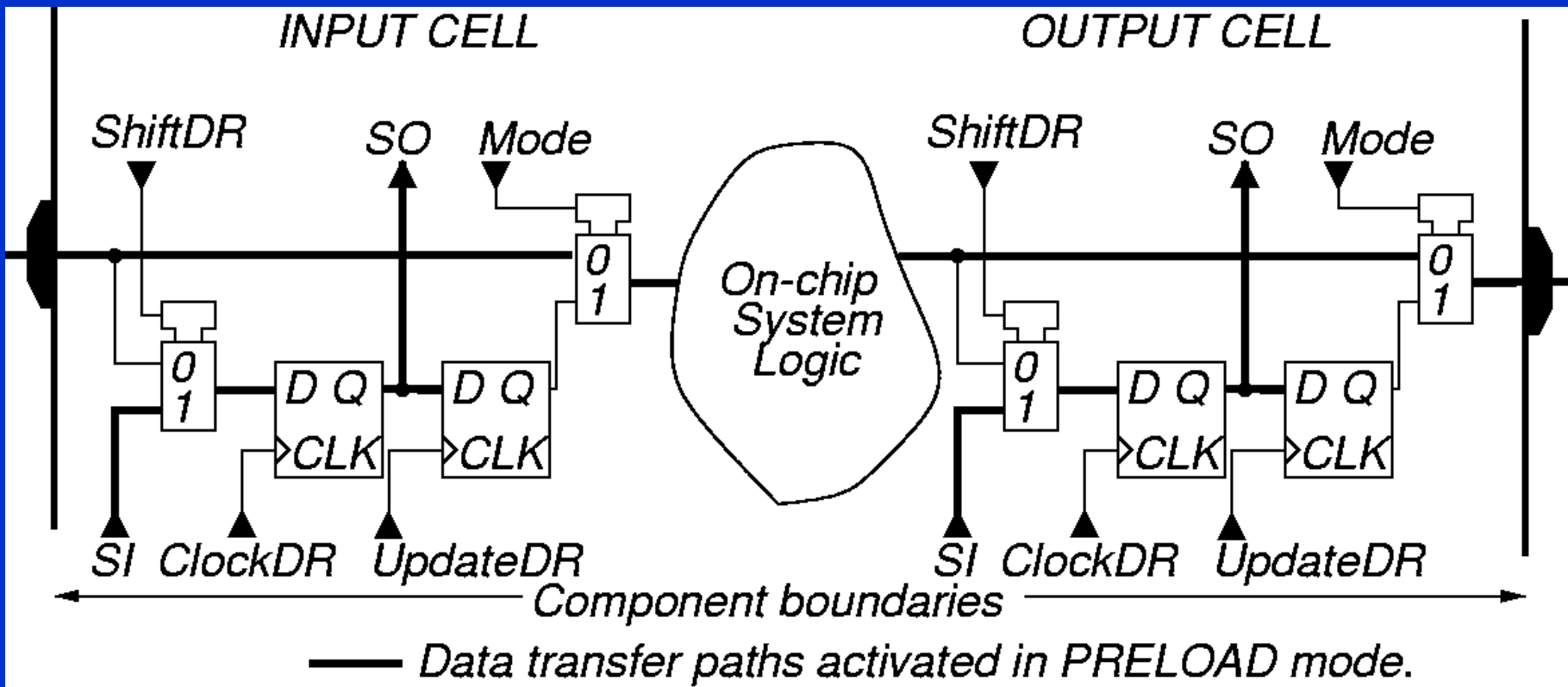
Instruction -- SAMPLE

Purpose:

- 2. Get snapshot of normal chip output signals**
- 3. Put data on bound. scan chain before next**

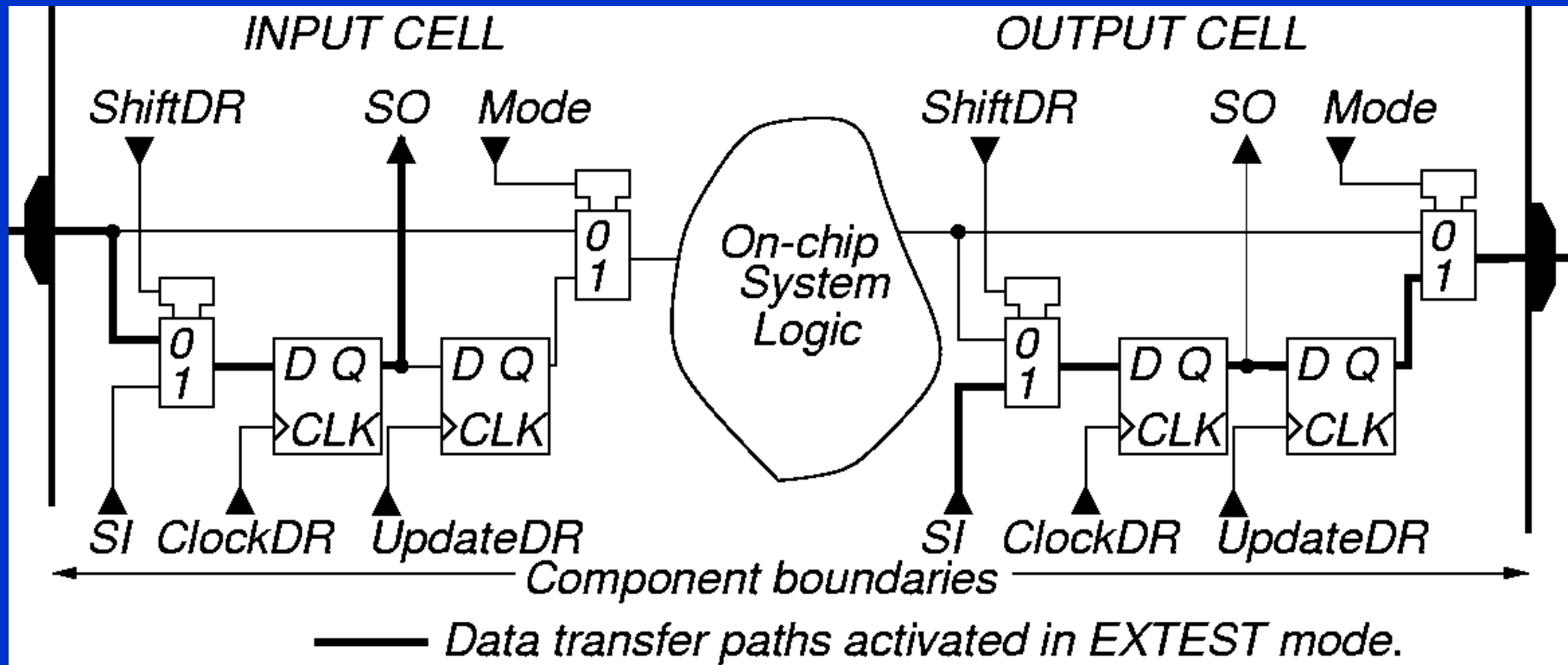


SAMPLE / PRELOAD **Instruction -- *PRELOAD***



EXTEST Instruction

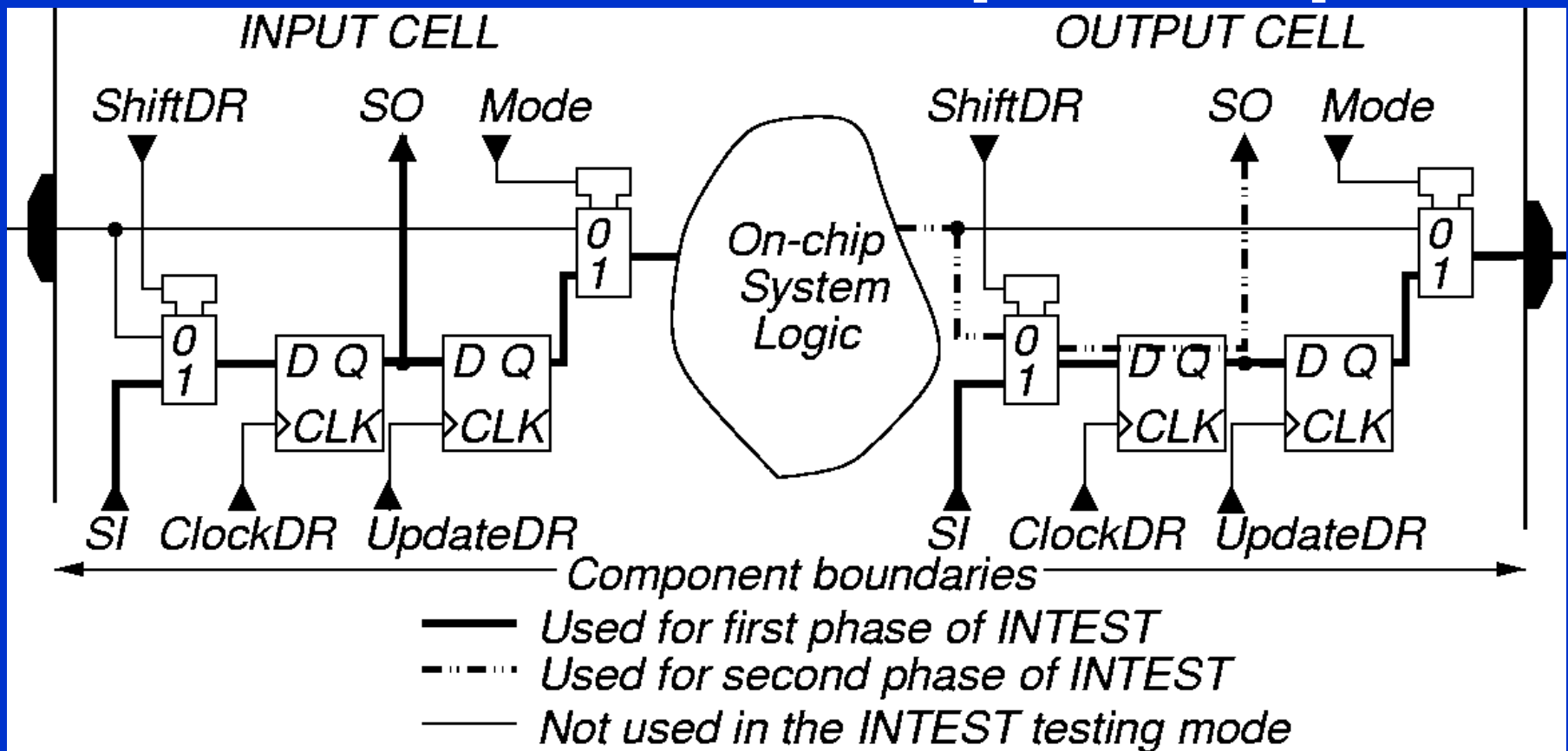
- **Purpose: Test off-chip circuits and board-level interconnections**



INTEST Instruction

Purpose:

1. Shifts external test patterns onto component
2. External tester shifts component responses



***RUNBIST* Instruction**

- **Purpose: Allows you to issue BIST command to component through JTAG hardware**
- **Optional instruction**
- **Lets test logic control state of output pins**
 - 1. Can be determined by pin boundary scan cell**
 - 2. Can be forced into high impedance state**
- **BIST result (success or failure) can be left in boundary scan cell or internal cell**
 - **Shift out through boundary scan chain**
- **May leave chip pins in an indeterminate state (reset required before normal operation resumes)**

***CLAMP* Instruction**

- **Purpose: Forces component output signals to be driven by boundary-scan register**
- **Bypasses the boundary scan chain by using the one-bit *Bypass Register***
- **Optional instruction**
- **May have to add RESET hardware to control on-chip logic so that it does not get damaged (by shorting 0's and 1's onto an internal bus, etc.)**

***IDCODE* Instruction**

- **Purpose: Connects the component device identification register serially between *TDI* and *TDO***
 - **In the *Shift-DR* TAP controller state**
- **Allows board-level test controller or external tester to read out component ID**
- **Required whenever a JEDEC identification register is included in the design**

Device ID Register -- JEDEC Code

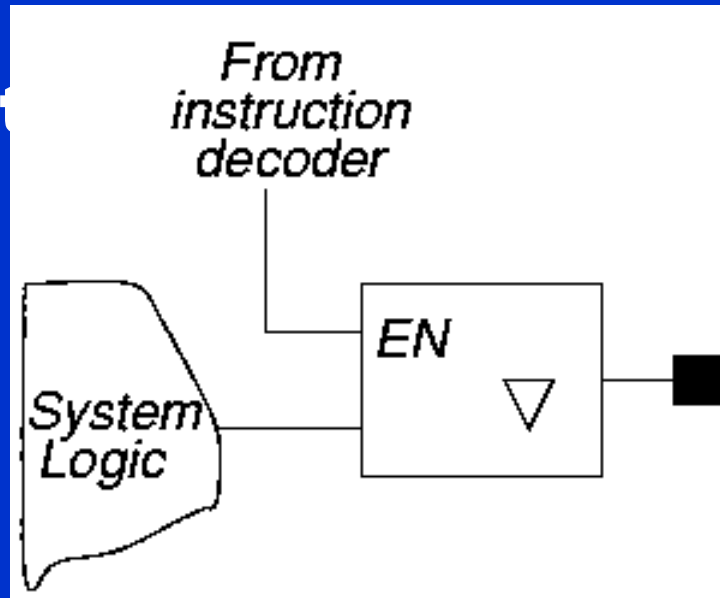
MSB							LSB
31	28	27	12	11	1		0
Version		Part Number		Manufacturer Identity		'1'	
(4 bits)		(16 bits)		(11 bits)		(1 bit)	

***USERCODE* Instruction**

- **Purpose: Intended for user-programmable components (FPGA's, EEPROMs, etc.)**
 - **Allows external tester to determine user programming of component**
- **Selects the *device identification register* as serially connected between **TDI** and **TDO****
- **User-programmable ID code loaded into *device identification register***
 - **On rising **TCK** edge**
- **Switches component test hardware to its system function**
- **Required when *Device ID register* included on user-programmable component**

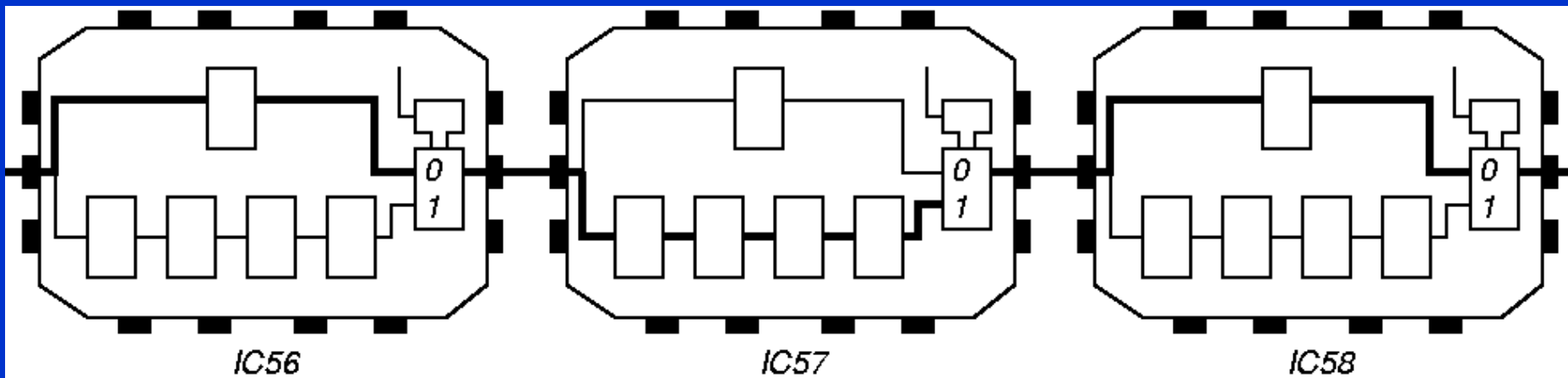
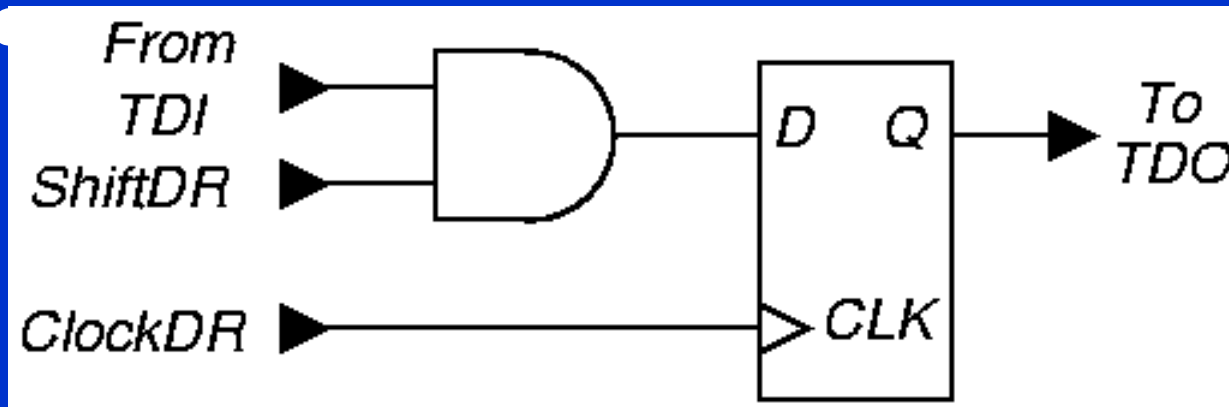
HIGHZ Instruction

- **Purpose:** Puts all component output pin signals into high-impedance state
- **Control chip logic to avoid damage in this mode**
- **May have to reset component after *HIGHZ* runs**
- **Optional inst**



***BYPASS* Instruction**

- **Purpose: Bypasses scan chain with 1-bit register**



Optional / Required Instructions

Instruction	Status
<i>BYPASS</i>	Mandatory
<i>CLAMP</i>	Optional
<i>EXTEST</i>	Mandatory
<i>HIGHZ</i>	Optional
<i>IDCODE</i>	Optional
<i>INTEST</i>	Optional
<i>RUNBIST</i>	Optional
<i>SAMPLE / PRELOAD</i>	Mandatory
<i>USERCODE</i>	Optional

Summary

- **Boundary Scan Standard has become absolutely essential --**
 - **No longer possible to test printed circuit boards with *bed-of-nails* tester**
 - **Not possible to test multi-chip modules at all without it**
 - **Supports BIST, external testing with Automatic Test Equipment, and boundary scan chain reconfiguration as BIST pattern generator and response compacter**
 - **Now getting widespread usage**