ADVANCED CMOS DEVICES AND RELIABILITY

BEN KACZER

UFRGS 2013 Tutorial
OUTLINE

CMOS FEOL trends

Why reliability

Examples of FET degradation mechanisms

TDDB

BTI
SCALING ROADMAP: VARIETY OF ARCHITECTURES ON THE HORIZON

Performance

Gate-first

Gate-last

FUSI

FinFET

Multi-gate

High-k, Metal Gate

45-32/28

22-15

32\textendash}
EXPLOSION OF MATERIAL AND DEVICE TECHNOLOGY OPTIONS

- **High k**
  - 1.0 μm
  - Pt/Si

- **Metal gates**
  - 120 nm

- **FinFET**
  - 19 μm
  - 20 μm

- **Strain**
  - 10 μm

- **Ge/III-V**
  - 25 μm

- **HP-Logic**
  - 30 μm

- **LP-Logic**
  - 40 μm

- **DRAM**
  - 50 μm

- **Flash-FG**
  - 60 μm

- **Flash-CT**
  - 70 μm

- **RRAM**
  - 80 μm

BEN KACZER, IMEC
Power supply voltage is saturating at about 1V due to non-scaling of subthreshold slope.
ELECTRIC FIELDS IN OXIDE AND IN SILICON INCREASE

Third scaling period: renewed constant voltage scaling due to non-scaling subthreshold slope has new implications on reliability!
POWER DENSITY INCREASES DUE TO NON-SCALING SUBTHRESHOLD SLOPE

Power density will soon be dominated by static power!

D. Cox, IRPS Tutorial 2004

Dynamic:

\[ P_{\text{dyn}} = \alpha \cdot V_{dd} \cdot V_{\text{swing}} \cdot C_{\text{eff}} \cdot f \]

Static:

\[ P_{\text{stat}} = V_{dd} \cdot I_{\text{leak}} \]

Almost all reliability problems are accelerated by Temperature!
NO TWO IDENTICALLY FABRICATED TRANSISTORS ARE ALIKE ANYMORE

These time-zero variations require adaptations in circuit design to account for statistical spread in device parameters

Asenov et al., IEDM 2008
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Reliability is an essential aspect of all products and technologies.
WHY RELIABILITY TESTING

As fabricated

Record performance!

E.g., a month later

Performance degraded!

Insufficient reliability: field returns, loss of profit, credibility, market share...

Devices cannot be tested for years (corresponding to field use) → accelerated testing needed!
ACCELERATED TESTING (IN FEOL) TYPICALLY DONE WITH V AND/OR T

Correct projection to operating conditions only possible if
- same mechanism at accelerated and operating conditions
- acceleration laws understood!
STOCHASTIC NATURE OF RELIABILITY MECHANISMS: A FRACTION OF DEVICES WILL FAIL!

Again, the distribution can be correctly described only if underlying mechanism understood!

As dimensions get smaller, distributions become wider (courtesy of T. Grasser)
RELIABILITY MUST BE PART OF EVERY (TECHNOLOGY) SPECIFICATION!

Example:
1 out of 10,000 chips (100ppm) allowed to fail in 10 years at operating conditions.
“CLASSICAL” APPROACH TO RELIABILITY ASSESSMENT

Reliability engineer

- accelerated testing/model
- failure mechanisms
- failure data statistics
- develop predictive reliability models

Design

→ Novel approaches needed to design reliable circuits with unreliable components: Reliability Aware Design (RAD)
RELIABILITY AND RECENT CMOS FEOL TRENDS

• New (3D) device architectures
• New “exotic” materials (high-k gate dielectrics, metal gates, high-mobility substrates)
• Downscaling of devices toward atomic dimensions (variability)
• Supply voltages are not correspondingly reduced

→ Reexamination of known “old” degradation mechanisms in new materials and architectures required
→ Revision of existing and need for novel characterization techniques
→ New reliability lifetime assessment methodologies
→ Reliability cannot be guaranteed at technology level: Reliability-Aware Design
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TIME-DEPENDENT DIELECTRIC BREAKDOWN (TDDB)

Electrical stress = Additional gate oxide leakage paths (TDDB) + FET intrinsic parameters change ("BTI")
Electrons and/or holes in the channel of a MOSFET gain high energy under influence of large electrical fields in the Si at the drain. They are injected into the oxide causing interface traps to be created and charges to be trapped in the oxide.
**POSITIVE / NEGATIVE BIAS TEMPERATURE INSTABILITY (BTI)**

Example: PFET at **Negative gate Bias** (and typically at elevated **Temperature**) pFET $V_{th}$ starts shifting (shows **Instability**) → **NBTI**

Charging of interface and oxide defects → $\Delta V_{th}$ and $\Delta \mu$

*Franco et al., IEDM 2010*
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Examples of FET degradation mechanisms
TDDB
  • Overview / Phases of BD
    • SILC
      • SBD & impact of position
      • Wear-out and HBD
BTI
Gate oxide breakdown = catastrophic failure


Gate oxide breakdown =

catastrophic failure

40 nm SiO₂
PHASES OF GATE DIELECTRIC BREAKDOWN

Electrical stress = Additional gate oxide leakage paths (TDDDB) + FET intrinsic parameters change (“BTI”)

Crupi et al., TED 1998
SINGLE TRAP CONDUCTION PATH

Additional leakage path = Trap-assisted tunneling with energy loss (*Takagi et al.*, TED 46(2), 1999). This is **Stress-Induced Leakage Current = SILC**.

- Steady-state SILC increase is proportional to neutral oxide trap density
- Trap near the middle between interfaces = highest conductivity

*Ielmini et al.*, TED 49 (11), 2002

*De Blauwe et al.*, TED 45(8), 1998
TWO COMPENSATING TRENDS IN ULTRA-THIN OXIDE SILC

Trend 1: trap generation rate drastically drops (figure)
- Less conductive paths through the oxide

Trend 2: conductivity per trap increases drastically
- Tunnel distance decreases and current rises exponentially
- Each trap contributes more to the total SILC
THE CHANGING APPEARANCE OF SILC

Thick / large device

Thick / large device:
- Capacitor top view
- SILC and individual trap components
- Many small contributions

Thin / small device

Thin / small device:
- Abrupt current increase of about 250nA
- = creation of single trap conduction path
- = ‘discrete’ SILC event
- This is NOT a breakdown

Capacitor cross section
TWO-TRAP CONDUCTION PATH

Percolation path with trap-assisted tunneling

- this is **Anomalous Stress-Induced Leakage Current** = a-SILC (non-volatile memories) (Okada *et al.*, IEDM 2001, Degraeve *et al.*, IEDM 2001)

  In thick oxide: moving bits in flash memory

- this is **Micro-Breakdown** (Cellere *et al.*, TED 49(8), 2002) or **pre-Breakdown** (Degraeve *et al.*, IEDM 2001)
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BTI
CONDUCTION PATH = SOFT BREAKDOWN = SMALL GATE CURRENT INCREASE

1st SBD observation (in 2 nm SiO₂):
  Farmer et al., APL 52, p. 1749 (1988)
• Localized current flow through lowered barrier
• Model: ‘quantum point contact’
  Suñé, IEDM 2000
• This is a soft breakdown, aka quasi-BD
  (Lee, IEDM 1994), partial BD, B-mode
  SILC (Okada, VLSI 1997).

<1 %-step detection mandatory in automatic tester
or, use smaller areas
or, use a noise-based detection (Roussel et al.,
  TDMR 1(2), 2001)
NO SIGNIFICANT EFFECT ON FET CHARACTERISTICS AT THE MOMENT OF SBD

Already in
Weir et al., IEDM, p. 73 (1997)

Kaczer et al., IRPS, p. 79 (2004)

Circuits will generally work after SBD! Gerrer et al., ESSCIRC 2009
Time-to-breakdown is Weibull distributed
Monomodal Weibull distribution is described as:

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^\beta\right] \Rightarrow \ln(-\ln(1-F)) = \beta \ln(t) - \beta \ln(\eta)$$
TDDB STATISTICAL DISTRIBUTION IS LINKED TO NUMBER OF TRAPS IN PERCOLATION PATH

Weibull slope increases with oxide thickness \( \rightarrow \) can be used to identify the breaking layer in a multilayer (high-k) stack

Not very precise or decisive for thin layers

Very indirect monitor
 Determination of the maximum applicable gate voltage

Combined effect of temperature acceleration and statistical scaling (depends on $\beta$!)

This extrapolation is only valid for soft breakdown

Voltage power-law more accurate than exponential also in high-$k$

Wu & Suñe, TED 2009
Evaluate $s \equiv \frac{I_D}{I_S + I_D}$ after BD in accumulation.

$s \equiv 0$

$s \cong 0$

$s \cong 1$

$s$ is a monotonically increasing function of $x$.

R. Degraeve, IRPS (2001)

Wu et al., IEDM, p. 187 (1998)

Pompl et al., IRPS, p. 82 (1999)

Yang et al., IEDM, p. 453 (1999)
EQUIVALENT ELECTRICAL CIRCUIT FOR FET AFTER BD

$F_S, F_D$ gate lengths, $B_S, B_D$ base lengths a function of BD position

$R_{path}$ independent of BD position

Explains varying FET behavior following BD

OTHER USES OF BD POSITION DETERMINATION

These 2 cases are equivalent in 1D

FinFETs: Crupi et al., TED 53, p. 2351 (2006)
Processing issues: Kauerauf et al., SISC (2004)
Uniformity of GOX stress in accumulation and inversion:
  Crupi et al., TDMR 3, p. 8 (2003)
Impact of BD position on BD wear-out: Pey et al., IRPS, p. 221 (2007)
Also B. Linder et al., IRPS, p. 403 (2003)
Correlation of successive BD’s and 1 and 2D:
  Alam et al., p. 151, IEDM 2002; p. 415, IEDM2005;
  TED 55, p. 3150 (2008)
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CONDUCTION PATH + THERMAL DAMAGE = HARD BREAKDOWN

Mass transport and Si regrowth in the breakdown spot
Lei Jun Tang et al., TDMR 4(1), 2004

Localized current flow through resistor (+diode)
Kaczer et al., TED 49(3) 2002
PHASES OF DEGRADATION AND WEAR OUT IN THIN OXIDES

1. SBD: Weibull ($\beta_{SBD}, \eta_{SBD}$)

2. Wearout: assume Weibull ($\beta_{wo}, \eta_{wo}$)

3. Runaway $R_S$-limited
In some cases the wear out phase is clearly observable by the increased ‘digital’ noise (Digital Breakdown)

\[ I(t) = \frac{\ln(10)}{a R_s} \log(t) + \frac{V_g}{R_s} + \ldots \equiv C \log(t_{rs}) + D(V_g) \]

- Analog breakdown rate increases with lower \( R_s \) (e.g. in Metal gates)
- Can be “arrested” by limited current supply (e.g. from previous stage)

Alam et al., IEDM 2000; Linder et al., VLSI 2001; Monsieur et al., IRPS 2003; Kaczer et al., IRPS 2004
HARDNESS OF BREAKDOWN DEPENDS ON GATE ELECTRODE

Post-BD current through BD path depends on gate material

Gate current run-away is positive feedback process controlled by electron ‘supply’ in the gate

HBD IS NOT WEIBULL DISTRIBUTED!

With limited data, hard breakdown resembles Weibull distribution

If HBD is fitted with Weibull, $\beta$ will be too high → erroneous conclusions can be drawn

TDDB data meaningful if BD detection criterion given

$V_G=2.2\text{V}$

$0.9 \text{ nm EOT SiO}_2/\text{HfO}_2$

$A=1.25\times10^{-09}\text{cm}^2$

- HBD $\beta_{\text{HBD}}=\sim1.2$
- SBD $\beta_{\text{SBD}}=\sim0.7$

Degraeve et al., IRPS 2006
Kerber et al., IRPS 2007
COMPETING FOR HBD: A TRIATHLON ...

- faster swimmer can be overtaken by even faster biker!

- In statistics described by series rule of reliability

\[
F_{\text{HBD}}[t] = 1 - \text{Exp} \left[ - \left( \frac{\eta_w}{\eta_c} \right)^{\beta_c} \int_0^1 e^{-\left( \frac{t - \tau_c}{\eta_w} \right)^{\beta_w}} \left( \frac{t - \tau_c}{\eta_w} - \left( - \ln \left[ 1 - F_{\text{tw}} \right] \right)^{\frac{1}{\beta_w}} \right)^{\beta_c} \, dF_{\text{tw}} \right]
\]

P. J. Roussel et al., Microelectron. Eng. 84, 1925 (2007)
ALL-IN-ONE RELIABILITY PREDICTION

Region 1 = breakdown-free
Region 2 = multiple soft breakdown
  ▶ Contours = relative leakage current increase DI/I₀ after 10 years
  ▶ NOTE: current increase for individual small transistor can be substantial!
Region 3 = Hard breakdown (taking multiple SBD into account)
  ▶ Contours = lifetime for 0.01% failures

SiO₂/HfO₂
EOT=0.9 nm

Sahhaf et al., IEDM 2007
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• Overview / BTI components

• Technological remedies

• NBTI recoverable component and AC stress

• BTI in deeply scaled devices

• Observing properties of individual defects

• Impact of individual defects on FET characteristics

• Constructing and projecting $\Delta V_{th}$ distributions

• Combining time-dependent and time-0 variabilities

• Defect-centric circuit simulation framework
Example: PFET $V_{th}$ at **Negative** gate **Bias** (and typically at elevated **Temperature**) starts shifting (shows **Instability**) $\rightarrow$ **NBTI**

Charging of interface and oxide defects $\rightarrow \Delta V_{th}$ and $\Delta \mu$
## BTI: CHARGED OXIDE BULK AND INTERFACE STATES

<table>
<thead>
<tr>
<th>NBTI (pFET)</th>
<th>PBTI (nFET)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Positive oxide charge</strong>&lt;br&gt;(negative $V_{th}$ shift)</td>
<td><strong>Negative oxide charge</strong>&lt;br&gt;(positive $V_{th}$ shift)</td>
</tr>
<tr>
<td><strong>Interface states</strong>&lt;br&gt;(mobility, transconductance, subthreshold-slope degradation)</td>
<td>X</td>
</tr>
<tr>
<td>Mahapatra, IEDM 2003</td>
<td>(but observed in sub 1nm EOT)</td>
</tr>
<tr>
<td>Mitani <em>et al.</em>, ECS 2005</td>
<td></td>
</tr>
<tr>
<td>Garros <em>et al.</em>, ICICDT 2010</td>
<td></td>
</tr>
<tr>
<td><strong>Generally at substrate interface</strong></td>
<td><strong>Generally trapping in high-k</strong></td>
</tr>
<tr>
<td>Zafar <em>et al.</em>, VLSI 2006</td>
<td></td>
</tr>
<tr>
<td>Mahapatra, TDMR 2007</td>
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<td>Kerber <em>et al.</em>, TED 55, 3175 (2008)</td>
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<tr>
<td>Aoulaiche <em>et al.</em>, IRPS 2009</td>
<td></td>
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</tbody>
</table>
EXAMPLE OF BTI LIFETIME EXTRAPOLATION

- **Failure Criterion:** $\Delta V_{th} = 30\text{mV}$ at $T = 125^\circ\text{C}$
- **Minimized relaxation:** $t_{\text{sense\_delay}} = 2\text{ms}$
- **Stress experiment at different voltages** ($V_{Gstress} > V_{DD}$) $\Rightarrow$ Estimate lifetime $\Rightarrow$ Power Law extrapolation at 10 Years
BTI IS A SERIOUS RELIABILITY PROBLEM

Ultra-Thin EOT high-k gate stacks with overdrive below the required 0.7V for 10 years

Courtesy of Cho and Franco, imec
“MINOR” COMPLICATION: THRESHOLD VOLTAGE SHIFT STARTS RELAXING IMMEDIATELY AFTER STRESS REMOVED

Crucial issue for all BTI measurements and interpretation!

Observed in p/nFETs, P/NBTI, DC and AC stress...

Alam, IEDM 2003; Kerber et al., TED 2008; Kaczer et al., IRPS 2008
BTI DEGRADATION RELAXES “DISPERSIVELY” OVER MANY TIME SCALES: µSECONDS OR LESS TO DAYS

→ Different measurement techniques to attack the problem

MSM = Measure-Stress-Measure
RELAXATION INCOMPLETE: PERMANENT DEGRADATION

Most common interpretation:
- Relaxation component – discharging of oxide defects
- Permanent component – generated interface states

1.4 nm SiON pFET
- $t_{\text{stress}} = 100$ s
- $T = 125$ °C

see Rangan et al., IRPS 2003
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PBTI CONTROLLED BY CHARGE TRAPPING IN HIGH-K

Significant reduction of PBTI is observed in nFETs with Lanthanum $V_{Th0}$-adjusting layer

$\Delta V_{th} (V)$

$E_{ox} (MV \ cm^{-1})$

- Group III elements compensate unpaired electrons around oxygen vacancy in HfO$_2$
- Similar effect caused by N (Xiong & Robertson, JAP 2006; Sahhaf et al., EDL 2010)
SIGE PFETS WITH BURIED CHANNEL PROMISE SUPERIOR PERFORMANCE OVER SI

To reduce NBTI:

- Increase Ge fraction
- Increase QW thickness
- Reduce Si cap thickness

Franco et al., IRPS 2010, IEDM 2010
Mitard et al., IEDM 2010
THIN Si CAP IMPROVES NBTI LIFETIME WHILE SCALING $T_{\text{inv}}$

- Enables $T_{\text{inv}}$ scaling while improving NBTI reliability
- Same trend consistently observed on SiGe, Ultra-Thin EOT SiGe, and pure Ge channels

J. Franco et al. IEDM 2010
**Thin Si cap**: channel carriers ($E_F$) ‘miss’ part of the oxide defects

- Less defects, located on the gate side, are energetically favorable for holes
- Stronger field acceleration due to ‘unaccessible’ traps becoming ‘accessible’
SiGe $\rightarrow$ LOWER $\Delta N_{OT}$

MODEL: REDUCED INTERACTION WITH OXIDE DEFECTS

**Thick Si cap:** channel carriers ($E_F$) ‘see’ all the oxide defects

- Less defects, located on the gate side, are energetically favorable for holes
- Stronger field acceleration due to ‘unaccessible’ traps becoming ‘accessible’
UNIFIED PICTURE: THE ENERGY ALIGNMENT BETWEEN CARRIER AND OXIDE DEFECTS CONTROLS BTI MECHANISMS

- nMOSFET PBTI: improved reliability shifting up the defect energy level by inserting Gd (Dy, La) in the high-k
- pMOSFET NBTI: improved reliability shifting up the channel Fermi level by using a (Si)Ge channel
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COMMON PROPERTY OF NBTI RELAXATION (RATE) AND LOW-F (“1/F”) NOISE: STATES WITH WIDELY DISTRIBUTED TIME SCALES

NBTI relaxation & rate

low-f noise (same device)

Both 1/f noise and R component higher in nitrided oxides

Kapila et al., IEDM 2008; Kaczer et al., IRPS 2009
LEARNING FROM NOISE: TWO ATTRIBUTES ESSENTIAL FOR CAPTURING BTI RELAXATION BEHAVIOR

low-f noise
(1) Many time scales → distributed RC components

\[ C = 10^0 \ldots 10^N \]

NBTI relaxation
(1) + (2) Different charging (capture) and discharging (emission) of each state

\[ C = 10^0 \ldots 10^N \]

Kaczer et al., IRPS 2008, 2009
Reisinger et al., IRPS 2010
PFET AC NBTI: (FAST) SEQUENCE OF STRESS AND RELAX PHASES

- AC BTI degradation lower than DC
- appears f-independent up to GHz

\[ T = 125 \, \text{C} \]
\[ t_{\text{stress}} = 1000 \, \text{s} \]
\[ V_S = V_D = V_B = V_{cc} = 2 \, \text{V} \]

AC NBTI:
- \( V_{select} = 2 \, \text{V} \)
- \( V_G = 0 \, \text{V} \)

DC NBTI:
- \( V_{select} = 0 \, \text{V} \)
- \( V_G = 0 \, \text{V} \)

Frequency (Hz)

Fernandez et al., IEDM 2006
Zhu et al., IRW 2002
Abadeer, IRPS 2003
Alam, IEDM 2003
Chakravarthi et al., IRPS 2004
DISTINCTIVE SHAPE OF AC NBTI $\Delta V_{TH}$ DEPENDENCE ON STRESS DUTY FACTOR

$\Delta V_{th} = R(t_{relax}) + P$ (mV)

- Shape with “plateau” due to recoverable component
- Correct model must reproduce this shape

$V_{stress} = -2.0 \text{V}$
$f_{stress} = 10 \text{ kHz}$
$t_{stress} = 6000 \text{ s}$
$t_{relax} = 10^{-3} (\bullet), 10^{-2}, \ldots, 10^4 \text{ s}$
$T = 125 \text{ oC}$
DUTY FACTOR DEPENDENCE OF THE RECOVERABLE COMPONENT REPRODUCED BY EQUIVALENT CIRCUIT

**Experiment**

\[ \Delta V_{th} = R(t_{\text{relax}}) + P \text{ (mV)} \]

Kaczer et al., IRPS 2008

- Distinctive shape of Duty Factor dependence cannot be explained by the classical Reaction-Diffusion model
- The shape is controlled by the recoverable component

\[ V_{\text{stress}} = 1 \text{ a.u.} \]
\[ t_{\text{relax}} = 10^{-3}, 10^{-2}, \ldots, 10^{4} \text{ a.u.} \]

\[ V_{\text{stress}} = -2.0 \text{V} \]
\[ f_{\text{stress}} = 10 \text{kHz} \]
\[ t_{\text{stress}} = 6000 \text{ s} \]
\[ t_{\text{relax}} = 10^{-3} (\bullet), 10^{-2}, \ldots, 10^{4} \text{ s} \]
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DEEPLY-SCALED DEVICE OPERATION IS AFFECTED BY INDIVIDUAL DEFECTS

In deeply-downscaled technologies, only a handful of random defects will be present in each device.

\[ N_{ot} = 10^{12} \text{ cm}^{-2} \rightarrow N_T \sim 10 \text{ if device area} = 10 \times 100 \text{ nm}^2 \]

Number of charged defects will be increasing with operating time \( \rightarrow \text{time-dependent variability} \) in addition to time-0 variability.
INDIVIDUAL DEFECTS RESULT IN TIME-DEPENDENT VARIABILITY

- Individual defects behave stochastically
- Individual defects have considerable relative impact on device
- These time-dependent variations require adaptations in circuit design to account for time-dependent statistical distributions of device parameters

Grasser et al., IEDM 2010
DEEPLY SCALED DEVICES: INDIVIDUAL EMISSION EVENTS VISIBLE IN NBTI RELAXATION TRACES

Large pFET

\[ \Delta V_{th} (mV) \]

\[
\begin{array}{c|c|c|c|c|c}
\tau_1 & \tau_2 & \tau_{n-2} & \tau_{n-1} & \tau_n \\
\hline
Kaczer et al., IRPS 2009
\end{array}
\]

70 × 90 nm² pFET

\[ \Delta V_{th} (mV) \]

relaxation time

[Asenov]
IN GENERAL, EACH DEFECT CHARACTERIZED BY

- capture time $\tau_c$
- emission time $\tau_e$
- impact on device ($\Delta I_d$ or $\Delta V_{th}$, ...)
- occupancy (0 or 1) at given time
  (covers BTI, RTN, ... easily extensible to other mechanisms)

EACH DEVICE CHARACTERIZED BY

- number of defects $N_T$ with above properties

Example: defects in 3 different devices

\[
\begin{align*}
\tau_c(V, T) & \quad | \quad \tau_e(V, T) \\
\tau_c(V, T) & \quad | \quad \tau_e(V, T) \\
\tau_c(V, T) & \quad | \quad \tau_e(V, T)
\end{align*}
\]

(size of bubble represents impact)

Kaczer et al., IRPS 2011
EXTENDED MEASURE-STRESS-MEASURE (eMSM): EFFICIENT WAY OF OBSERVING MOST DEFECTS

Example: 3 deeply-scaled devices

\[
\tau_e(V_L, T) \quad \tau_e(V_H, T) \quad \tau_e(V_L, T)
\]

\[
\tau_c(V_H, T) \quad \tau_c(V_H, T) \quad \tau_c(V_H, T)
\]

\[
\text{degradation (\~\text{total } \Delta V_{th})} \quad \sim \log \text{stress time} \quad \sim \log \text{relaxation time}
\]
Random Telegraph Noise (steady-state)

NBTI relaxation transient (perturbation/non-steady-state)

$\Delta V_{th}$ (mV)

$V_{th}$ (mV)

$t_{stress} = 0$ s

$t_{stress} = 1900$ s

B. Kaczer et al., IRPS 2009 & 2010
RTN, BTI STRESS AND BTI RECOVERY UNDERSTOOD WITHIN THE SAME “UNIFIED” PICTURE

Assume 5 defects with different time constants present in a single device

T. Grasser et al., IEDM 2010

Noise under cyclo-stationary conditions: G. I. Wirth et al., IEDM 2009
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EXPERIMENTAL SETUP

-0.1V

$L \times W = 70 \times 90 \text{ nm}^2$

DC or AC stress

$V_{\text{G}}$ (V)

$V_{\text{STRESS}}$

$t_{\text{STRESS}}$

$t_{\text{relax}}$

• Initial $I_s - V_G$ used to convert $\Delta I_s$ to $\Delta V_{th}$

M. Toledano et al., IRPS 2011

B. Kaczer et al., IRPS 2005 & 2008
Example: repeated emission from a single defect

\[ \Delta V_{TH} \sim 22 \text{mV} \]

\[ V_{RELAX} = -0.63 \text{V} \]
\[ V_{STRESS} = -2.20 \text{V} \]
\[ t_{STRESS} = 20.13 \text{s} \]

\[ \langle \tau_{emission} \rangle = 11.1 \text{ s} \]

Toledano et al., IRPS 2011
CONSTRUCTING THE DEFECT SPECTRUM

aka “Time Dependent Defect Spectroscopy” (TDDS) map

Grasser et al., IRPS 2010
As steps reappear in multiple traces, clusters begin to form.
CONSTRUCTING THE DEFECT SPECTRUM 3

As more steps are added, clusters begin to form, identifying each trap by its “fingerprint”
MULTIPLE DEFECTS CAN BE CHARACTERIZED SIMULTANEOUSLY

- Every defect is characterized by step height $\Delta V_{th}$ and emission time
- Cluster intensity indicates defect occupancy

Toledano et al., INFOS 2011
EMISSION AND CAPTURE TIMES EXTRACTED, OBSERVED TO BE VOLTAGE DEPENDENT

Increasing $V_{\text{STRESS}}$, $\tau_{cH}$ decreases (easier to charge)
$\tau_{eH}$ increases (more difficult to emit)

Important for circuit simulations with varying voltages
SINGLE TRAP OCCUPANCY AFTER “AC” WORKLOAD CAN BE DESCRIBED

Waveform: a sequence of constant $V’s$

$$P_C = \frac{\tau_e(V)}{\tau_e(V) + \tau_c(V)} \left\{ 1 - \exp \left[ - \left( \frac{1}{\tau_e(V)} + \frac{1}{\tau_c(V)} \right) t \right] \right\}$$

Note: lines not fits to data, calculated purely from DC $\tau$ values!

Toledano-Luque et al., IRPS 2011
CMOS FEOL trends
Why reliability
Examples of FET degradation mechanisms
TDDB

**BTI**

- Overview / BTI components
- Technological remedies
- NBTI recoverable component and AC stress
- BTI in deeply scaled devices
- Observing properties of individual defects
- Impact of individual defects on FET characteristics
- Constructing and projecting $\Delta V_{th}$ distributions
- Combining time-dependent and time-0 variabilities
- Defect-centric circuit simulation framework
STATISTICS OF $\Delta V_{TH}$'S DUE TO SINGLE TRAPPED CHARGES EXTRACTED: EXP DISTRIBUTED

$B. \text{Kaczer et al., IRPS 2010, EDL 2010}$

$f_1(\Delta V_{th}, \eta) = \frac{\exp \left(-\frac{\Delta V_{th}}{\eta} \right)}{\eta}$

$\eta = 4.75 \text{ mV}$

$t_{stress} = 1900 \text{ s}$

$\eta (V) = \text{expectation value} = \text{average shift per elementary charge}$
CAUSE: RANDOM DOPANT FLUCTUATIONS IN THE CHANNEL

Channel current non-uniform: flows via percolation paths

One “lucky” TRAP can cause an important decrease of drain current ($\Rightarrow V_{TH}$)!!

Note: lower substrate doping $\Rightarrow$ smaller effect of TRAP

http://www.ibiblio.org/e-notes/Perc/contour.htm

e.g. Ghetti et al., TED 2009
SCALING OF $\eta$

Average shift per $q$:

$$\eta \approx \frac{t_{inv}^\alpha \sqrt{N_A}}{L W}$$

Scales reciprocally with gate area

$A = (2H_{fin} + W)L$ (nm$^2$)

Scales with $t_{inv}$ and $N_A$ (via $V_B$)

J. Franco et al., IRPS 2012 & 2013
“ULTIMATE” RELIABILITY EXPERIMENT: A FET $I_D$-$V_G$ WITH AND W/OUT A SINGLE CHARGED TRAP

Note apparent transconductance increase after trapping event

Franco et al., IRPS 2012, EDL 2012
PATTERN OBSERVED IN BEHAVIOR BASED ON THE DISTANCE FROM CRITICAL SPOT

Bukhari et al., IIRW 2010, Franco et al., IRPS 2012
OUTLINE

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Instead of averages, lifetime distributions projected

Past (large devices)

Present (small devices)

“Classical” reliability

Time-Dependent Variability
CONSTRUCTING TOTAL DEVICE-TO-DEVICE $\Delta V_{TH}$ DISTRIBUTION

1) Exponential distribution of $\Delta V_{th}$ steps due to a single defect

\[ f(\Delta V_{th}) = \frac{e^{-\frac{\Delta V_{th}}{\eta}}}{\eta} \]

\[ t_{stress} = 1900 \text{ s} \]

$\eta = 4.75 \text{ mV}$

2) Poisson distribution of the average number of defects $N_T$

(note: $N_T = W L N_{ot}$)
BTI STATISTICS FULLY DESCRIBED BY IMPACT PER DEFECT $\eta$ AND NUMBER OF ACTIVE DEFECTS $N_T$

$$H_{\eta,N_T}(\Delta V_{th}, \eta) = \sum_{n=0}^{\infty} \frac{e^{-N_T} N_T^n}{n!} \left[ 1 - \frac{n}{n!} \Gamma(n, \Delta V_{th} / \eta) \right]$$

$\eta = \langle \text{single defect impact} \rangle$

$N_T(t) = \langle \# \text{ of active defects per device} \rangle$

Known statistics $\rightarrow$ all moments can be derived
**CONVERTING BETWEEN MINDSETS**

**Time-dependent variability**

**Technology**
- Avrg. number of defects $N_T$
- Average impact per defect $\eta$

\[
N_T(t) = 2\frac{\langle \Delta V_{th}(t) \rangle^2}{\sigma_{\Delta V_{th}}^2}
\]

\[
\eta = \frac{\sigma_{\Delta V_{th}}^2}{2\langle \Delta V_{th}(t) \rangle}
\]

**Design**
- Average shift $\langle \Delta V_{th} \rangle$
- Variability $\sigma_{\Delta V_{th}}$

\[
\langle \Delta V_{th}(t) \rangle = \eta N_T(t)
\]

\[
\sigma_{\Delta V_{th}}^2(t) = 2\eta^2 N_T(t)
\]

- Time-dependent variability increases with degradation
- Time (degradation kinetics) can be taken out of the equation
- Note factor of “2” rigorously derived
\( N_T \) OR \( \langle \Delta V_{TH} \rangle \) EXTRACTED AS A FUNCTION OF TIME AND VOLTAGE

\( N_T \) at 10 years

Toledano et al., VLSI 2011
A FRACTION OF DEEPLY-SCALED DEVICES EXCEEDS FAILURE CRITERIA AT LOWER OVERDRIVES

\[ \Delta V_{TH} = 30\text{mV at 10 years} \]

- \( A = 35 \times 90 \text{nm}^2 \)
- \( 5 \times A \)
- \( 10 \times A \)
- \( 1000 \times A \)

median

M. Toledano et al., VLSI 2011
OUTLINE

CMOS FEOL trends

Why reliability

Examples of FET degradation mechanisms

TDDB

BTI

• Overview / BTI components
• Technological remedies
• NBTT recoverable component and AC stress
• Defect properties
  • Observing properties of individual defects
  • Impact of individual defects on FET characteristics
  • Constructing and projecting $\Delta V_{th}$ distributions
• Combining time-dependent and time-0 variabilities
• Defect-centric circuit simulation framework
TIME-DEPENDENT VAR ADDS TO TIME-0 VARIABILITY

\[ V_{TH}(t) = V_{TH0} + \Delta V_{TH}(t) \]

\[ \text{Stress} \int_{0}^{\infty} (V_{TH} - V) H_{\eta,\Delta V_{TH}/\eta}(V) dV \]

Total \( V_{th} \) distribution

Initial \( V_{TH0} \) variability

Time-dependent \( \Delta V_{TH} \) variability

\[ \sigma_{V_{TH0}}^2 \propto \frac{t_{ox} \sqrt{N_A}}{WL} \]  

\[ \sigma_{\Delta V_{TH}}^2(t) = 2\eta \langle \Delta V_{TH}(t) \rangle \]

Kuhn et al., TED 2011

\[ L_x W = 35 \times 90 \text{ nm}^2 \]
INITIAL & TIME-DEPENDENT VARIABILITY ARE CORRELATED

• Independently of technology, $\sigma_{\Delta V_{TH}}$ and $\sigma_{V_{TH0}}$ are correlated

\[ \sigma_{\Delta V_{TH}}^2 \propto \frac{t_{ox} \sqrt{N_A}}{WL} \]

\[ \sigma_{\Delta V_{TH}}(t) = 2\eta \langle \Delta V_{TH}(t) \rangle \]

where

\[ \eta \propto \frac{t_{ox} \sqrt{N_A}}{WL} \]

Same sources of channel variability (RDF, MGG, LER, etc.) responsible

• Time-dependent variability can be predicted from time-0 var

→ allows benchmarking existing and future technologies

Toledano et al., VLSI 2013
IMPACT OF TIME DEPENDENT VARIABILITY INCREASES WITH OPERATION

Empirical relation (pFET): $\sigma_{V_{TH0}}^2 \approx 200 \text{ mV} \times \eta$

Derived from $H$-statistics: $\sigma_{\Delta V_{TH}}^2 (t) = 2 \eta \langle \Delta V_{TH} (t) \rangle$

Observed correlation (pFET): $\sigma_{\Delta V_{TH}}^2 (t) \equiv \frac{\langle \Delta V_{TH} (t) \rangle}{100 \text{ mV}} \sigma_{V_{TH0}}^2$

Franco et al., IRPS 2013

Observed correlation (pFET): $\sigma_{\Delta V_{TH}} (t)$ with $\eta = 3.4 \text{ mV}$
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Example: 3 deeply-scaled devices

Failure spec circuit dependent! → **Reliability-Aware Design**
FETs IN STANDARD CIRCUIT NETLIST INSTANTIATED WITH INDIVIDUAL TRAPS
THE CIRCUIT IS SOLVED WITH INDIVIDUAL DEFECT BIAS-TIME (I.E., WORKLOAD) DEPENDENCES
SIMULATION FRAMEWORK BASED ON EXISTING INDUSTRY-STANDARD TOOLS

INPUT
- Trap & sim parameters (config file)
- Circuit (standard netlist + model card)
- Control script (perl)
- FET model (BSIM4/Verilog-A)
- Trap kinetics

OUTPUT
- Circuits (enhanced netlists)
- Circuit performance metrics

HSPICE or SPECTRE + Verilog-A

test an INV: transient analysis

simulator lang=spectre

include "L90_SPHVT10_V102.lib.scs" section=tt

ahdl_include "bsim4_spectre.va"

include "logicgates.sub"

.. 

SetTemp alter param=temp value=temperature

// Circuit Installation
X1and3 (vddCell g vddCell out vddBulk) AND3

// Power Supplies
VvddBulk (vddBulk 0) vsource type=dc dc=vddBulk
VvssBulk (vssBulk 0) vsource type=dc dc=vssBulk

VvQ ( g 0 ) vsource dc=vlo type=pulse
val0=vlo val1=vhi period=1n delay=0.4n rise=0.01n fall=0.01n width=0.49n

VvddCell ( vddCell 0 ) vsource type=dc dc=vddCell
VvssCell ( vssCell 0 ) vsource type=dc dc=vssCell

..
#Start the file
spice_file = and3.scs

USE store_inputs

Monte = 1
internal_monte=1
language = spectre

#transistor parameters

vth0_mean_pmos = -0.25
vth0_sd_pmos = 0.05
vth0_mean_nmos = 0.25
vth0_sd_nmos = 0.05

#Traps density#

pmos_trap_density_sio2 = 9e10
nmos_trap_density_sio2 = 5e10
nmos_trap_density_hk = 2e10

#standard transistor definition

wp=90nm
lp=70nm
wn=90nm
ln=70nm

#input history

start_time=0

..
SIMULATION FRAMEWORK BASED ON EXISTING INDUSTRY-STANDARD TOOLS

Kaczer et al., IRPS 2011

Circuit (standard netlist + model card)

FET model (BSIM4/Verilog-A)

Control script (perl)

Trap & sim parameters (config file)

HSPICE or SPECTRE + Verilog-A

INPUT

Circuits (enhanced netlists)

Circuit performance metrics

.. 

Nmnmos3_X1nand_X1and3 (_X1nand_X1and3_midnode vddCell 0 0) bsim4_va type=1 l=80nm w=100nm*1*2
vth0=0.224068372498511 Ntraps=8 VH=0.8 VL=0 len=8
DeltaVth=[ 0.00021502392265272
0.00129168432396303 0.0047480549849773
0.00115964999542421 0.0018326350216282
0.00177542424038912 0.00122528625484488
0.00193559032206868 ] tcH=[ 0.0034617748767338
2.9514020629307e-11 2.35108924858284e-07
7.5008568766976e-10 1.34632779405625e-06
1.0944844080164e-12 4.6405220957496e-11
1.532523524155e-06 ] tcL=[ 100000000 100000000
100000000 100000000 100000000 100000000 100000000 100000000 ] teH=[ 0.304046922519998
2.77299758745423e-06 1.0359818715254
0.00901532692412415 0.000905011102154941
2.8672832368865e-06 0.000135952087963774
0.018531074298117 ] teL=[ 0.00185336582376316
4.43992015382931e-08 0.0144582180307964
0.000171466248546535 4.396634106273e-07
2.76627004569314e-08 4.38821936112408e-07
0.000238047697343963 ] ic_trap=[ 0 0 0 0 0 0 0 ] device_seed=1301500415

OUTPUT

ircuit performance metrics

Kaczer et al., IRPS 2011
SIMULATION FRAMEWORK BASED ON EXISTING INDUSTRY-STANDARD TOOLS

**INPUT**
- Trap & sim parameters
- Control script (perl)

**Circuit**
- (standard netlist + model card)
- FET model (BSIM4/Verilog-A)

**OUTPUT**
- Circuit performance metrics
- Trap kinetics

\[
P_{p,v} = \frac{\tau_{p,v}}{\tau_{e,v} + \tau_{c,v}} \left\{ 1 - \exp \left[ -\left( \frac{1}{\tau_{e,v}} + \frac{1}{\tau_{c,v}} \right) \Delta t \right] \right\}
\]

---

```verbatim
/*
File's brief description:
This is the include file to simulate the defect trapping and detrapping of NBTI model & Calculate the total occupancy of defects.
*/

/*************************************************************************/
Modified by Swaraj for NBTI
***************************************************************************/

Vth=Vth+IC_DeltaVthNbti;
//Modified Vth due to inicial NBTI defect......Swaraj
if(analysis("tran")) begin
    //$strobe(" " \nNew TimeStep");
    SimTime_new=$abstime;
    if(SimTime_new >= SimTime_old)begin
        TimeStep=SimTime_new-
        SimTime_old;
        //$strobe("Simulation Time Step=%e", TimeStep);
        SimTime_old=SimTime_new;
    end
    ...
```

---

Kaczer et al., IRPS 2011
SIMULATION FRAMEWORK BASED ON EXISTING INDUSTRY-STANDARD TOOLS

Circuit (standard netlist + model card)
- FET model (BSIM4/Verilog-A)
- Control script (perl)
- Trap & sim parameters (config file)

INPUT OUTPUT
- Circuits (enhanced netlists)
- Circuit performance metrics

 normalized delay

 normalized power

$ts = 10^{-8} \text{s}$

$ts = 10^8 \text{s}$
SIMULATION FRAMEWORK ALLOWS TO FOLLOW BOTH FAST AND SLOW DEFECTS

Kaczer et al., IRPS 2011
32-BIT SRAM BIT SLICE WORKLOAD DEPENDENCE ANALYZED WITHIN THE SIMULATION FRAMEWORK

D. Rodopoulos et al., ICICDT 2011

Other applications of framework:

V. V. A. Camargo et al., IEEE T. VLSI Systems, 2013
Khan, Hamdioui et al., DDECS 2012, DFT 2012
H. Kukner et al., EuroMicro 2012
CIRCUIT SIMULATION FRAMEWORK “V2”

Transistor dimensions

CET map

Workload

\[ \int \int \]

\( N_T \)

\( \Delta V_{th} \) distribution

\( \eta \approx 4 \text{ mV} \)

\( N_T = 1, 2, \ldots, 20 \)

\( N_T = 6 \)

\( N_T = 9 \)

\( N_T = 14 \)

P. Weckx et al., IRPS 2013
\( \Delta V_{TH} \) DISTRIBUTION INSERTED INTO EACH FET: EXAMPLE SRAM CELL

- CDF\(_3\)
- CDF\(_4\)
- CDF\(_5\)
- CDF\(_6\)
- CDF\(_1\)
- CDF\(_2\)

- The CDFs can be combined with time-zero variability
SNM DISTRIBUTIONS CAN BE PROJECTED AS A FUNCTION OF OPERATING TIME

P. Weckx et al., IRPS 2013
IMPACT OF VARIOUS WORKLOAD SCENARIOS CAN BE SIMULATED

Results can be combined with expected SRAM usage distributions

P. Weckx et al., IRPS 2013

Bansal et al., IRPS 2012
SUMMARY

• Reviewed the basics of
  • TDDB (SILC, Soft BD, progressive wear-out, Hard BD...)
  • and N and PBTI (Interface vs. bulk, Recoverable and Permanent components, DC and AC stress...)

• Time-dependent (in addition to time-zero) variability will occur in future nm-sized technologies:
  • the “defect-centric” perspective provides basis for understanding and mitigating reliability issues at appropriate level
THERE ARE ONLY TWO KINDS OF PEOPLE

1) Those who cannot extrapolate …