A VLSI Architecture for Reference Frame Compression on High Definition Video Coding Systems

Guilherme Povala, Lívia Amaral, Dieison Silveira, Júlio Mattos, Marcelo Porto, Luciano Agostini
Introduction
Introduction

- Block diagram of a typical video coding system
Memory issues in a video coding system
- Energy consuming
- Bottleneck of many digital systems
Memory Issues in Video Coding

- Known Solutions for memory issues
  - **Data reuse**
    - Reduces reading operations
    - Requires a cache
  - **Reference frame compression**
    - Compresses reference frames before they are stored in the external memory (DRAM)
    - Reduces reading and writing operations
    - It can be lossy or lossless quality
Memory Issues in Video Coding

- **Lossless reference frame compression:**
  - Reduces reading and writing operations
  - Keeps video quality unaltered
  - Requires a lossless compression algorithm
  - It can be used by the current video encoders, like H.264/AVC and HEVC
The main goals of the designed RFCAVLC were:

- Lossless to avoid quality degradation
- Achieve good compression rates
- Decode one sample per cycle
- Provide a throughput enough to process high resolution videos in real time
RFCAVLC8t

- RFCAVLC8t (Reference Frame Context Adaptive Variable-Length Compressor with 8 tables);
- It uses 4x4 blocks during the coding process;
- It reaches a compression rate of more than 31% on average;
- Compresses the frame before it is stored in the external memory;
- Decompresses the frame when it is required by ME;
- Uses eight static Huffman tables.
Video coding system
Video coding system + RFCAVLC8t

**Diagram:**
- **External Memory**
- **Decoder**
- **Encoder**
- **RFCAVLC**
- **ME/MC**
- **Deblocking Filter**
- **Residual Frame**
- **Reconstructed Frame**
- **Residual Coding**
- **Compressed Residue**
- **Entropy Coding**
- **Bitstream**
RFCAVLC Architecture

- Architecture of the RFCAVLC Encoder

```
4x4 Samples Block

128 -> Average Calculator

32 -> External Memory

8 -> Sample Controller

39 -> Table Selector

39 -> Tables
```

SIM ‘13 – South Symposium on Microelectronics
RFCAVLC Architecture

- Architecture of the RFCAVLC Decoder

External Memory

Control Unit

Parser

Translator

Assembler

4x4 Samples Block

Tables
The architecture was described in VHDL and synthesized to the EP4S40G2F40I2 Altera Stratix 4 FPGA device.

<table>
<thead>
<tr>
<th>Results</th>
<th>Encoder</th>
<th>Decoder</th>
<th>RFCAVLC</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALUTs</td>
<td>1.563</td>
<td>5.056</td>
<td>6.516</td>
</tr>
<tr>
<td>Registers</td>
<td>169</td>
<td>852</td>
<td>1.147</td>
</tr>
<tr>
<td>Frequency</td>
<td>295.62 MHz</td>
<td>198.89 MHz</td>
<td>198.30 MHz</td>
</tr>
<tr>
<td>Throughput</td>
<td>45 fps (WQSXGA)</td>
<td>30 fps (WQSXGA)</td>
<td>30 fps (WQSXGA)</td>
</tr>
</tbody>
</table>

It is able to encode one sample per cycle.

Throughput: 30 frames per second in WQSXGA (3200x2048) resolution.
Conclusions

- This work presented the RFCAVLC8t, a solution for memory bandwidth reduction in video coding systems through lossless reference frames compression.
- This design presented a very low hardware cost and reached a high throughput, processing more than 198 millions of samples per second.
- The best architecture performance among the related works.
- This solution is compliant with state-of-the-art coding standards, such as the H.264/AVC and the emerging HEVC.
Future Works

- Implementing a memory solution that uses both RFCAVLC and Data Reuse to improve bandwidth reduction
- Obtaining and analyzing power and energy results
A VLSI Architecture for Reference Frame Compression on High Definition Video Coding Systems

Thank you!

Guilherme Povala