A Fully-Integrated CMOS Class-AB Power Amplifier

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Sumario

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Introduction

A Power Amplifier (PA) is a circuit designed for delivering high power signal to a load, while keeping the efficiency as high as possible. Trends in the design of these circuits include its full integration in CMOS technologies and addressing the trade-offs between supply voltage, output power, power efficiency and linearity.
Proposed Topology

Fig. 1 Topology of Proposed PA
Design Methodology

Load pull

Fig. 2 Load Pull Contours example for 2.4GHz
Design Methodology

Stability

\[ K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \]

\[ \beta_{1f} = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \]

\[ \Delta = S_{11}S_{22} - S_{21}S_{12} \]
Efficiency

\[ PAE = \frac{P_{out} - P_{in}}{P_{DC}} \]

\[ n = \frac{P_{out}}{P_{DC}} \]

\[ n_{AVG} = \frac{P_{out, AVG}}{P_{DC, AVG}} \]
Simulation Results

Fig. 3 Spectrum of Power Output

- Power at 2.4 GHz = 17.57 mW
- Power at 4.6 GHz = 71.17 uW
- Power at 7.2 GHz = 12.46 uW

Fig. 4 Curve of S-parameters analysis for (S_{11})

- BW = 112 MHz
- S11 at 2.4 GHz = -20.38 dB
Simulation Results

Fig. 5 Stability factor $K$

Fig. 6 Alternative stability factor ($\beta_{1f}$)
Simulation Results

Fig. 7 Curve of 1 dB Compression Point

1st Order freq = 2.4 GHz
Input Referred 1dB Compression = -11.8340 dBm
## Simulation Results

### Table 1- MonteCarlo Analysis

<table>
<thead>
<tr>
<th></th>
<th>$\sigma$</th>
<th>$\mu$</th>
<th>$N$</th>
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</thead>
<tbody>
<tr>
<td>Output Power</td>
<td>1.74 mW</td>
<td>17.35 mW</td>
<td>442</td>
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<tr>
<td>Power Consumption</td>
<td>1.65 mW</td>
<td>41.92 mW</td>
<td>442</td>
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<tr>
<td>$K$</td>
<td>0.032</td>
<td>1.70</td>
<td>442</td>
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<tr>
<td>$\beta_{1f}$</td>
<td>0.004</td>
<td>0.85</td>
<td>442</td>
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<tr>
<td>$S_{11}$</td>
<td>1.034 dB</td>
<td>-20.278 dB</td>
<td>442</td>
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<tr>
<td>Efficiency</td>
<td>2.67 %</td>
<td>41.4 %</td>
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</table>
### Simulation Results

#### Table 2- Corners Analysis

<table>
<thead>
<tr>
<th>Corners</th>
<th>Output Power (mW)</th>
<th>DC Consumption (mW)</th>
<th>K</th>
<th>$\beta_{1f}$</th>
<th>$S_{11}$ (dB)</th>
<th>n (%)</th>
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<tr>
<td>Nominal</td>
<td>17.57</td>
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<td>1.7</td>
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<td>ff</td>
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<td>36.57</td>
<td>1.779</td>
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<td>-18.42</td>
<td>32.89</td>
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</table>
Fig. 8 Power Amplifier Layout
Conclusion

A fully-integrated 2.4 GHz power amplifier implemented in standard CMOS 0.18-µm technology was presented. By using a driver and power stage as well as on-chip input and output matching networks, the presented PA achieves high gain and high output power. It can submit an output power of 12.45 dBm with 41% of drain efficiency, in the power stage, for a input power of -11.42 dBm. The corners and montecarlo analysis showed good accuracy with the typical simulations.
Thanks

Questions?