ASCEND: A STANDARD CELL LIBRARY FOR SEMI-CUSTOM ASYNCHRONOUS DESIGN

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Introduction

- Evolution of technologies used to fabricate ICs
  - SoCs, VLSI circuits
  - Limitations of the synchronous paradigm

- Asynchronous circuits
  - Possible solution
  - ITRS
  - Not recent paradigm
  - Limited research, limited quality
Asynchronous Circuits

- No clock signal to control sequencing of events
- Synchronization, communication and operation employ handshaking
  - Registers clocked only when and where needed!!

![Diagram of asynchronous circuits with registers and control signals](image)
Asynchronous Circuits

- **The C-element**
  - Fundamental in async.
  - Event synchronization

\[ Q = (A \times B) + (A \times Q) + (B \times Q) \]

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<tr>
<th>A</th>
<th>B</th>
<th>( Q_i )</th>
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Asynchronous Circuits

- Delay-Insensitive Minterm Synthesis (DIMS)
  - Semi-custom Design
  - C-Elements and OR gates

- MUTEXs
  - Mutual Exclusion Elements
  - Electric race

\[
Aa = \overline{Rb} \lor Ra \\
Ab = \overline{Ra} \lor Rb
\]
Null Convention Logic (NCL)
- Theseus Logic, Inc.
- Low power, high speed, high density, fault tolerance
- Semi-custom Design

NCL Gates
- Threshold Function with positive weights + hysteresis
  - m-of-n for logical 1s
  - n-of-n for logical 0s
- 2-of-3

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The ASCEnD Flow and Library

- ASCEnD Flow \(\rightarrow\) Used for generating over 500 C-Elements (SoCC’11)
The ASCEnD Flow and Library

- **ASCEnD-ST65**
  - STMicroelectronics 65nm CMOS
  - C-Elements
  - Metastability Filters X1, X2, X3 and X4
  - 14 NCL Primitives (X1, X2, X3 and X4)
Conclusions and Future Work

- Vertical Integration of ASCEnD Flow with CMOS Technologies
- Parameterizable Design Flow
- Future
  - ASCEnD-IBM130
    - Integrated with ARM/ARTISAN Libraries
    - Compatible with MOSIS
  - Development of new tools
THANK YOU!

QUESTIONS?