A Tool to Evaluate Stuck-Open Faults in CMOS Logic Gates

Alexandra L. Zimpeck, Cristina Meinhardt e Paulo F. Butzen
Summary

- Introduction
- Motivation
- Stuck-Open Faults
- Stuck-Open Faults in Nanometer Technologies
- Tool Development
- Conclusions and Future Works
Introduction

• The technology scaling causes several undesired effects:
  – Leakage;
  – Variability;
  – Reliability–Aging;
  – Increase the number of possible faults.

Stuck-On  Stuck-Open

Transients  Stuck-At  Bridging
Introduction

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  - Leakage;
  - Variability;
  - Reliability–Aging;
  - Increase the number of possible faults.

Stuck-On

Stuck-Open

Stuck-At

Bridging

Transients
Stuck-Open Faults

NOR2 Logic Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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Stuck-Open Faults

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The output signal floats in a high impedance state.
Stuck-Open Faults

• For example, considering the pair of vectors below:

  - AB = 00: Previous State

    Expected Result: 1 
    Obtained Result: 1

  - AB = 01: Next State

    Expected Result: 0 
    Obtained Result: 1

Voltage of the previous state
The structure used for analysis of logic gates in presence of faults.

The NOR2 block diagram shows the expected result with test application of technology of 45nm.
Stuck-Open Faults in Nanometer Technologies

The structure used for analysis of logic gates in presence of faults.

Obtained result with SOF in technologies of 45nm.
Stuck-Open Faults in Nanometer Technologies

The structure used for analysis of logic gates in presence of faults.

Obtained result with SOF in technologies of 16nm and 45nm.

High leakage currents influence greatly behavior of SOFs!
Holding Time

$45\text{nm} = 200\text{ns}$

$16\text{nm} = 30\text{ns}$

$1.00$ $0.80$ $0.60$ $0.40$ $0.20$

$0.0$ $0.1$ $0.2$ $0.3$ $0.4$ $0.5$ $0.6$ $0.7$ $0.8$ $0.9$ $1.0$

Time (us)

Holding time ($VDD - |Vtp|$)$^1$

Holding Time x Technology

High Frequency

16nm: 1 fault
45nm: 1 fault

1.20
1.00
0.80
0.60
0.40
0.20

0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0
Time us

OUT45
OUT16

0.80
0.60
0.40
0.20
Holding Time x Technology

Medium Frequency

16nm: 0 fault
45nm: 1 fault
Holding Time x Technology

Low Frequency

16nm: 0 fault
45nm: 0 fault
Motivation

- The use of tools that assist the project of integrated circuits are relevant due to the high design complexity.
  - Even more important in nanometer technologies due to emergent challenges

- This work presents a tool that analyzes the circuit behavior in the presence of SOFs and the interaction with leakage currents, also allows to evaluate the holding time parameter.
The Tool – Fault Simulator

- **User Interface**
- **Input Parameters**
- Fields generated by the program
The Tool – Fault Simulator

- **User Interface**
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Tool Development

User Interface

Input Data

Read of Circuit

Data Validate

Input Data

Generate Test Vectors

Test Vectors

Fault Simulation

Obtained Result

Response Analyzes

Obtained Result

Comparison

Expected Result

Expected Result

Circuit Description

Input Data

Circuit Description

Test Vectors
Tool Development

Consists in knowing the circuit in which the fault will be simulated.
Tool Development

User Interface

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Data Validate

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Comparison

Expected Result

Verifies the data supplied by the user. Automatically generated the correct truth table.
Tool Development

Generation of vectors:

- \( \leq 3 \) inputs: all combinations.
- > 3 inputs: random.

User Interface

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Generate Test Vectors

Fault Simulation

Input Data

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Obtained Result

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Circuit Description

Obtained Result

Expected Result

Input Data

Test Vectors
Simulates the circuit in the presence of a stuck-open fault in the transistor chosen for the user.
Tool Development

User Interface

Read of Circuit

Data Validate

Generate Test Vectors

Fault Simulation

Input Data

Test Vectors

Obtained Result

Response Analyzes

Expected Result

Obtained Result

Comparison

Expected Result

Makes the comparison between these two results and from this module calculates the percentage of faults during test application.
Conclusions and Future Works

• With the aid of this tool, it is possible to determine the coverage fault of some circuits;

• This tool can be also used to assist the impact evaluation of fault tolerance techniques applied to logic gates.

• Next step in the development of this tool is compute the holding time and include analyses of other kinds of faults.
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Muito Obrigada!

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