What is a 3D IC?

- An Integrated Circuit composed of 2 or more layers of active electronics...
  - ...stacked on top of each other or mounted side by side (2.5D ICs)
- 2.5D ICs are considered by many as 3D ICs – same technologies
- Key enabler: TSV – Through Silicon Via

Related Names:
- 3D SIC – Stacked IC
- SiP, SoP – System in/ on Package, from System on Chip (SoC)
- PiP, PoP – Package in/ on Package
- SCS - Stacked Chip SoC
- Chip stack MCMs (Multi-Chip Modules)
- This is not Intel’s 22nm tri-gate FinFET 3D transistors

Motivation: 1

- Scaling: shrinking, packing more electronics in the same space, making them faster, less power, more reliable, with more value
- Moore's Law
- Economics
- 10BS foundries
- Need to aggregate value, keep improving...
- More than Moore
- Diversification to add value

Motivation: 2

- Internal (die) – needs more scaling:
  - CI’s evolved tremendously as flat surfaces
  - Many metal layers enabled integration
  - Today reaching all limits: xtor size, wire delays (GHz), power, yield...
  - The “only” way is to escape vertically
- External (package/PCB) – scaling demands:
  - Dramatic scaling makes dies very far from the PCB
  - Ex: 28nm metal1 pitch compared to a 0.4mmPCB: > 10000 x
  - It translates to huge delay, power, signal integrity problems
  - Performance limitation (memory latency/bandwidth)
- Package/Integration must evolve into foundry-like size/processing
Promises of 3D

- Scaling – more components/performances in the same area/cost
- System-on-Package – from PCBs to smaller footprints (mobiles)
- Heterogeneous integration – easier, analog/digital, different processes
- Shorter global/average wirelength – homogeneous
- Better timing, bandwidth
- Low power (10-100 times)
- Increased yield/integrity (less on PCB)
- Reduced cost with better yield (partitioning)
- Security
- Ex from Samsung: 35% smaller, 50% less power, 800% improvement in bandwidth to DRAM

Challenges

- Yield – many additional steps are needed
- Heat removal – focus of many research works
- TSV overhead – size, placement, legalization, parasitics, stress
- Test – depending on the partitioning
- Design Complexity – including CAD complexity
- Lack of standards (new tech) – being addressed
- Integration and supply chain (delays)
- Lack of clearly defined ownership (ecosystem/business model)
- Nevertheless, a revolution happening right now...

Current Technology: Fabrication

1. TSV Fabrication
   - Deep silicon etching
   - Via oxide deposition
   - C4 via reflow deposition
   - Cu plating
   - CMP

2. Wafer Thinning and Bonding
   - Carrier wafer
   - Temporary carrier bonding
   - Back-side thinning
   - Expose Cu vias
   - Permanent bonding
   - Temporary carrier de-bonding

Current Technology: Data Points

- BGA - 0.4 a 0.8mm
- C4 bump - 40-250um
- Microbump - 5-45um
- TSV - 5-100um
- Transistor – 12 to 28m (source: Amkor, Yole Development)

Current Technology: Examples

- Tezzaron
- Amkor
- TSMC
- Intel
- JEDEC Solid State Technology Association, formerly known as the Joint Electron Devices Engineering Council (JEDEC) - Standards
  - http://www.jedec.org/category/technology-focus-area/3d-ics/d
### Products/Designs
- Intel Pentium 4 in two tiers - 2004
- Intel 80-core Teraflop – improved mm communication – 2007
- Many other research designs. Ex: The 3D-MAPS Many-Core Processor – 2 tiers F2F – GeorgiaTech (2012: http://www.gatech.edu/research/centers/3d-maps)
- Many SoPs being used on Mobile devices
- Apple A5 is PackageOnPackage
- Apple A6 should use TSMC 3D-IC
- Xilinx Virtex-7 T Family – 6.8B transistor, TSMC 3D-IC, side by side

### Market Trends
- **Main drivers:**
  - Imaging/Optoelectronics - 26%
  - Logic 3D SIP/SoC - 30%
  - 3D Wide IO Mem - 15% (important: speed/low power)
  - 3D Stacked DRAM - 15%
- **Other (~9% or less):**
  - 3D stacked NAND Flash
  - MEMS/Sensor
  - LED
  - RF, Power, Analog, Mixed-Signal
- **Expected Market:**
  - 2014 - 2M wafers - 2500 M USD$
  - 2017 - 9M wafers
    (source: Yole Development)

### CAD Tools
- Cadence 3D-IC Solution:
- Synopsis:
  http://www.synopsys.com/Solutions/EndSolutions/3d-ic-solutions/Pages/default.aspx
- Mentor Graphics:
  http://www.mentor.com/solutions/3d-ic-design/
- Most of these are “aware” of 3D technology, understand it, its libraries, and provide analysis tools
- There is a lot to do for automation, however

### Concluding
- 3D ICs and chip stacking is at its momentum
- You will see a lot of new designs/products using it
- It can keep Moore’s law expectations for the next years
- This is not only for the most advanced billion-dollar process
- Chip stacking is a “replacement” for PCBs, a bridge to advanced scaling
- There is a lot to do...
- There is a lot to learn...
- There is a lot of research on...
- As a breakthrough, it provides opportunities for new people and new companies to jump to the state of the art