

A Reconfigurable Digital Decimation Filter Design for a Cascade 2-2 Sigma-Delta Analog-to-Digital Converter

Cristian Müller, Paulo César C. de Aguirre, Cesar A. Prior and João B. S. Martins
{cristian.muller, paulocomassetto}@mail.ufsm.br
{prior, batista}@inf.ufsm.br

Grupo de Microeletrônica – Gmicro
Universidade Federal de Santa Maria – UFSM

Abstract

This paper presents a reconfigurable digital design of filtering and decimation for a cascade 2-2 sigma-delta ($\Sigma\Delta$) analog-to-digital converter (ADC). The $\Sigma\Delta$ ADC reconfigures its MASH (Multi-Stage-Noise-Shaping) topology and building blocks in order to adapt the bandwidth requirements to diverse standard specifications. This reconfigurable design is composed by a logic cancellation of the total first stage quantization error, a 5th order CIC decimation filter followed by a Finite Impulse Response (FIR) compensator to correct the pass-band attenuation due to the CIC filter and a half-band FIR to reduce the transition band response. The complete high-level design was simulated in Matlab/Simulink environment and the hardware implementation of this design was coded with VHDL using optimization techniques for computational resources reduction aiming to reduce area and power consumption for future standard cell implementation. At this time, the complete design was validated and prototyped in a Stratix II FPGA device.

1. Introduction

The mobile telecommunications are in ascendant growth with progressive development of wireless communication systems. It is being reflected in new communications Standards with larger transmission bandwidths. The most common standards are the Global System for Mobile Communications (GSM), Wide-Band Code-Division Multiple Access (CDMA) and Wireless Local Area Networks (WLAN).

Also, mobile systems are expected to work with multi-mode Standards supplying the user's needs. Analog-to-Digital Converters (ADCs) are present in the most communications systems and they shall combine a good compromise between power consumption and bandwidth requirements. The Sigma-Delta ($\Sigma\Delta$) ADC is the most promising candidate to achieve high resolutions in different bandwidths requirements. The advantage of $\Sigma\Delta$ ADCs is that they provide high resolution with relative low precision components using oversampling and noise-shaping.

The bandwidth increase in a $\Sigma\Delta$ ADC, considering a constant circuit operating frequency, can be achieved by the $\Sigma\Delta$ modulator order increment. In order to design a Dual-Mode $\Sigma\Delta$ ADC composed by a cascade 2-2 $\Sigma\Delta$ modulator, shown in Fig.1, it was designed a complete reconfigurable Decimation Filter. As the modulator order programmability in this approach is achieved by the control of the cascade or MASH (Multi-Stage-Noise-Shaping) architecture [1], [2] a reconfigurable digital logic cancellation circuit is needed [3].

This paper presents a digital part of a Dual-Mode $\Sigma\Delta$ ADC and it is composed by a logic cancellation of the total first stage quantization error, a 5th order CIC decimation filter followed by a Finite Impulse Response (FIR) compensator employed to correct the pass-band attenuation due to the CIC filter and a half-band FIR to reduces the transition band response. This digital circuit combined with an analog cascade 2-2 $\Sigma\Delta$ modulator complete a Dual-Mode $\Sigma\Delta$ ADC.

The paper is organized as follows. Section 2 focuses on the filter specification, the appropriate choice of the digital filter architecture and the circuit high-level models in a Matlab/Simulink environment. Section 3 describes the optimization techniques employed to design the digital filter. Section 4 provides the results of the circuit implementation in a Stratix II FPGA. Finally, conclusions are given in Section 5.

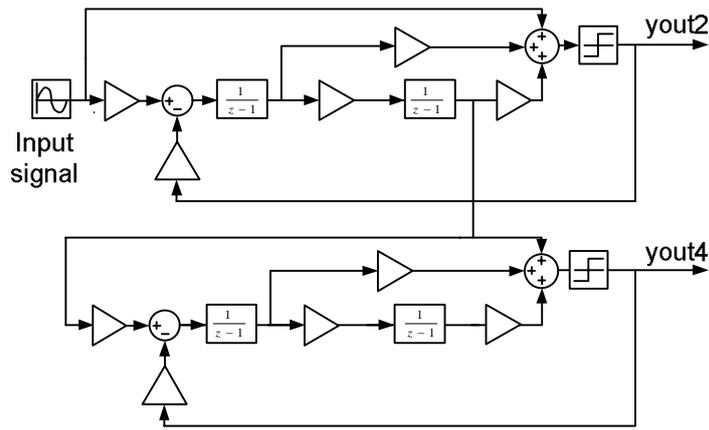


Fig. 1 – Typical Cascade 2-2 Sigma-Delta Modulator.

2. Dual-Mode $\Sigma\Delta$ ADC Specification and High Level Simulation

The specifications of the Dual-Mode $\Sigma\Delta$ ADC are: 5 MHz operating frequency, 10 kHz bandwidth and 50 kHz bandwidth operating with a 2nd and a 4th order modulator, respectively. The power spectral density of the ideal modulator output with 2nd and 4th order configuration is shown in Fig. 2. This MASH modulator is similar to the one presented in [4].

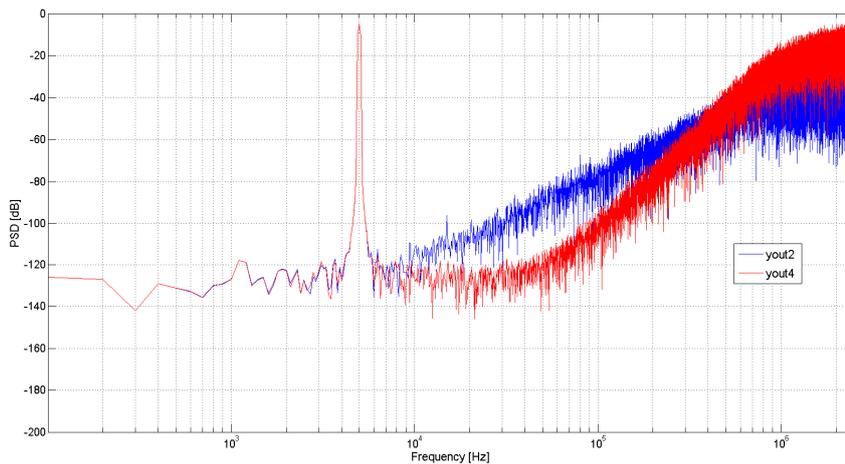


Fig. 2 – Behavioral output power spectrum density (PSD) for a -3 dB input amplitude.

To supply the needs of this Dual-Mode ADC the digital filter specifications are: 0.01 dB pass-band ripple, 80 dB stop-band minimum attenuation and 3-4 times oversampling output. Aiming to minimize the logic resource and power consumption of the digital filter a multi-stage topology [5] was used.

The digital filter first stage is composed by a 5th order Cascaded Integrator-Comb (CIC) in accordance with [6] and [7]. This CIC filter is followed by a compensator Finite Impulse Response (FIR) to correct the pass-band attenuation due to the CIC filter and a half-band FIR filter to reduce the transition band. In Fig. 3 is shown the Dual-Mode ADC diagram block.

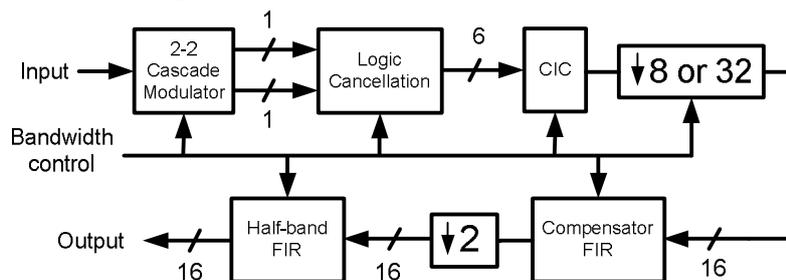


Fig. 3 – Dual-Mode ADC diagram block.

Initially, the high-level filter model was created and simulated with the Filter Design and Analysis tool and the complete ADC simulation was performed in Matlab. As the modulator operates with two different bands, two filter models were created with features that allow the subsequent integration into a single digital filter that could be configured to operate in either band. Both bandwidth filter models were created with 30 valid coefficients (summing the Compensator and half-band FIR stages), 80 dB stop-band attenuation and 100 dB aliasing signal attenuation. The decimation rates and transition bands for the 10 kHz and 50 kHz bandwidth filter models are 64 and 11 kHz, and 16 and 60 kHz, respectively. The filter response for both bandwidths is shown in Fig. 4.

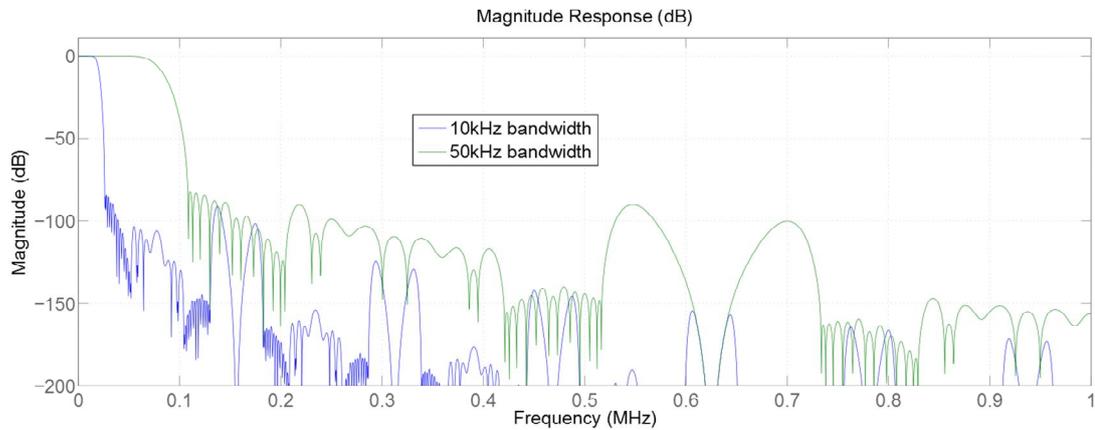


Fig. 4 - Attenuation caused by 10 kHz and 50 kHz bandwidth filters.

3. Logic Design and Simulation

This filter was designed employing techniques of logical structures reuse and serial multiplications, especially minimizing the multipliers in FIR stages aiming to increase logical resources optimization and reduce the circuit power consumption. The reuse of logical structures is based on the fact that the Dual-Mode $\Sigma\Delta$ ADC works with only one bandwidth requirement at same time, allowing that the same logical structures (adders, multipliers and registers) operate in both modes.

The serial multiplication, as shown in Fig. 5, can occur because the data output frequency is less than that circuit operating frequency due to the oversampling. Therefore, it is possible to perform several multiplications at each multiplier in FIR stages.

Through these two techniques the number of multipliers was minimized to only 2. This digital design was coded in VHDL, simulated with ModelSim tool and validated with the same stimuli data used in the high-level models.

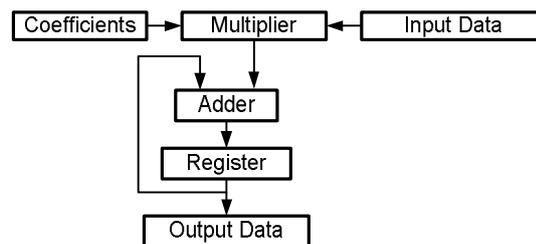


Fig. 5 – Schematic of a serial multiplier.

4. FPGA Implementation

The designed digital system was synthesized in an Altera Stratix II EP2S60F672C3N FPGA, using Quartus II. Tab. 1 shows the maximum operating frequency and the synthesis results for the implemented design in the specified device. To validate the FPGA prototyping, additional structures were implemented in the same FPGA to provide input stimuli and capture the output data from the digital design. These input stimuli are the same used in the high-level simulation.

Tab. 1 – Synthesis Results		
Stratix II EP2S60F672C3N		
Frequency	#ALUTs	#DLRs
67,76 MHz	868	1082

The output power spectral density data from the FPGA design implementation is shown in Fig. 6. The designed reconfigurable digital filter eliminates the high frequency noise, reaching a Signal-to-Noise and Distortion Ratio (SNDR) of 85 dB, approximately, for both bandwidth.

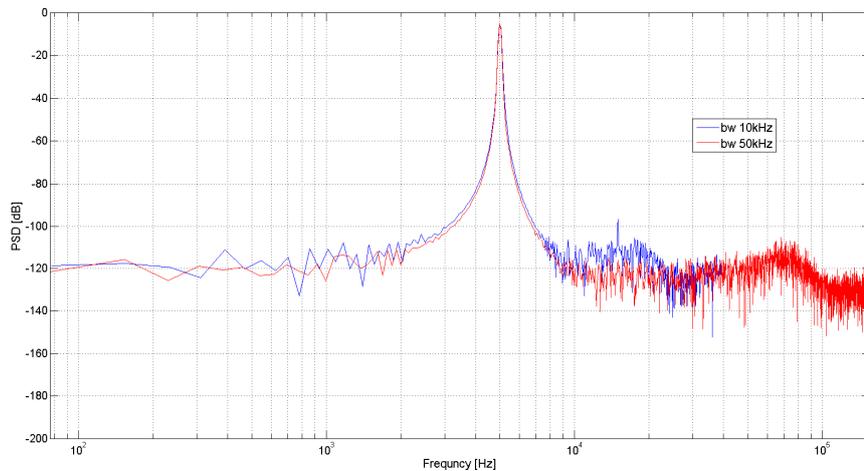


Fig. 6 –ADC output power-spectrum for a -3dB input amplitude.

5. Conclusions

This paper presented the design, validation and FPGA synthesis results of a reconfigurable digital logic cancellation and filtering architecture for a Dual-Mode $\Sigma\Delta$ ADC composed by 2-2 cascade $\Sigma\Delta$ modulator. Through techniques of logical structures reuse and serial multiplications the number of multipliers was minimized to only 2. The FPGA design implementation achieved a SNDR of 85 dB, approximately, for both bandwidth requirements.

The future works include the extension of this digital reconfigurable filter that will cover the triple-mode operation showed in [4] and its design with standard cells for IC prototyping.

6. References

- [1] B. R. Jose, J. Mathew, P. Mythili, and D. K. Pradhan, "A Multi-Mode Sigma-Delta ADC for GSM/WCDMA/WLAN Applications", *J Sign Process Syst* (2011) 62:117–130, DOI 10.1007/s11265-008-0326-z.
- [2] A. Xotta, A. Gerosa, and A. Neviani, "A Multi-Mode $\Sigma\Delta$ Analog-to-Digital Converter for GSM, UMTS and WLAN," *IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, May 2005, vol.3, pp. 2551-2554.
- [3] P. C. C. Aguirre, F. C. Lucchese, L. Teixeira, C. Müller, and C. A. Prior, "Digital Logic Cancellation Block for a Cascade Feed-Forward Sigma-Delta Analog-to-Digital Converter" *26th South Symposium on Microelectronics*, 2011. v. 1. p. 149-152.
- [4] R. Tambara, C. A. Prior, P. C. C. Aguirre, and J. B. S. Martins, "High-Order Low-Distortion Switched-Current Cascade 2-2-2 Sigma-Delta Modulator," *IEEE Latin American Symposium on Circuits and Systems*, 2012, Playa del Carmen, México. *LASCAS 2012 Proceedings*, 2012.
- [5] Ricardo Losada: *Digital Filters with MATLAB*, May 2008. [Online]. Available: www.mathworks.com/matlabcentral/fileexchange/19880.
- [6] E. Hogenauer, "An economical class of digital filters for decimation and interpolation," *Acoustics, Speech and Signal Processing*, *IEEE Transactions on*, vol.29, no.2, pp. 155- 162, Apr 1981.
- [7] S. Parameswaran, N. Krishnapura, "A 100 μ W Decimator for a 16 bit 24 kHz bandwidth Audio $\Delta\Sigma$ Modulator," *Circuits and Systems (ISCAS)*, *Proceedings of 2010 IEEE International Symposium on*, vol., no., pp.2410-2413.