INF01 118

Técnicas Digitais para Computação

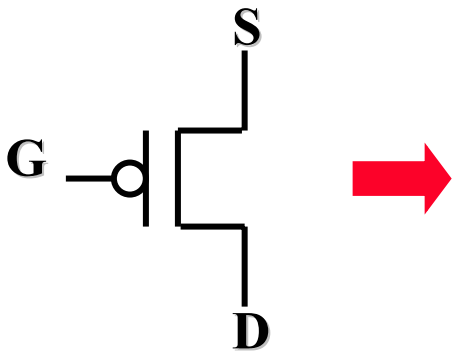
UFRGS

Pass Transistors (transistor de passagem)
Transmission Gates (portas de transmissão)
Lógica Tri-state

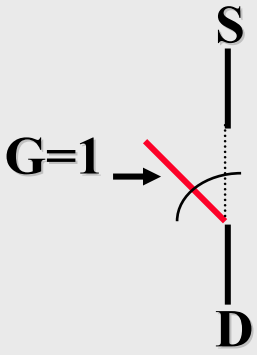
Aula 5

Transistores PMOS e NMOS

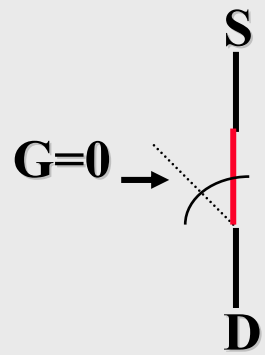
PMOS:



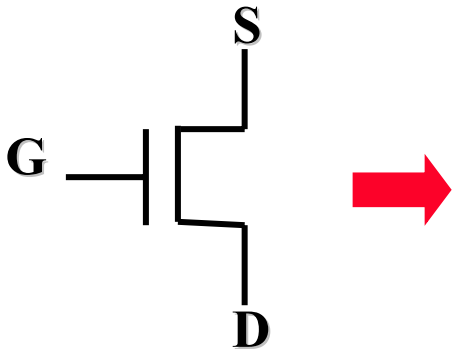
Se G = 5V (‘1’)
Chave aberta (off)



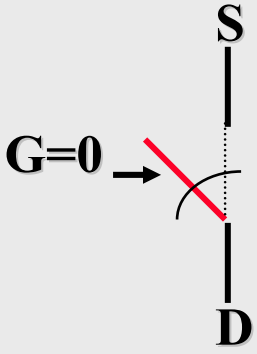
Se G = 0V (‘0’)
Chave fechada (on)



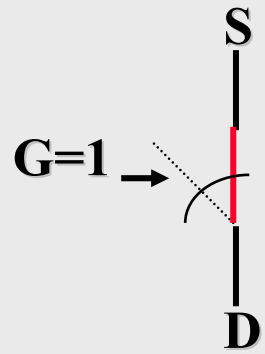
NMOS:



Se G = 0V (‘0’)
Chave aberta (off)

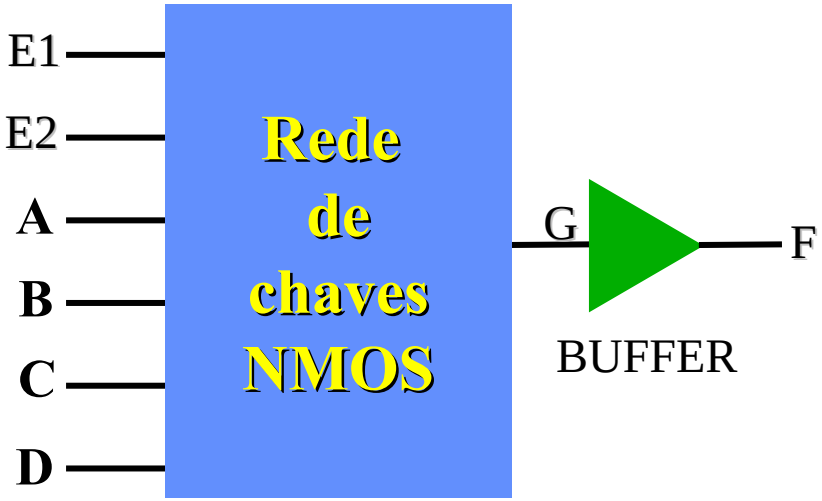


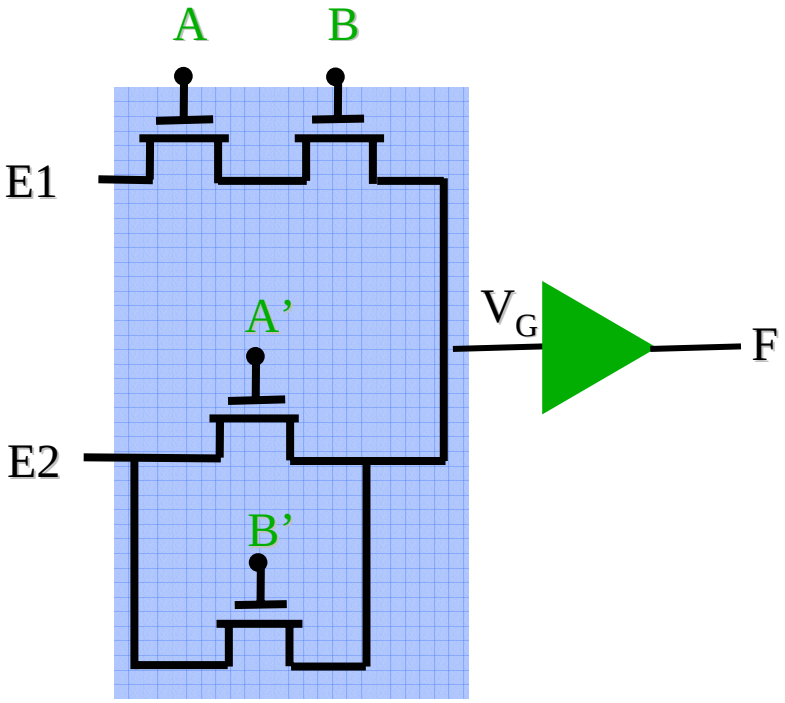
Se G = 5V (‘1’)
Chave fechada (on)



Portas Lógicas

Lógica com chaves NMOS





Transistores N

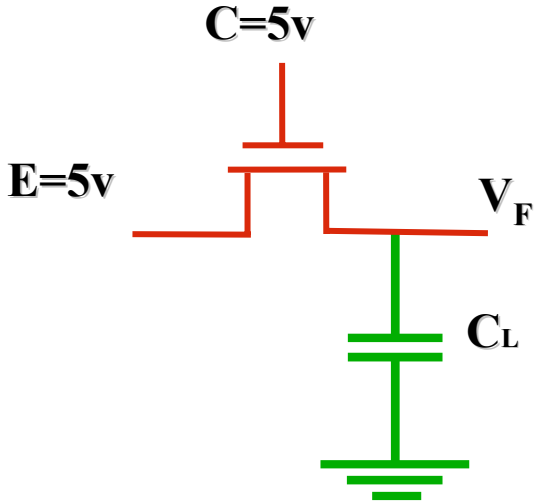
Sem consumo estático na rede de chaves.

V_G alto varia em função da lógica.

O buffer regenera o sinal lógico.

Portas Lógicas

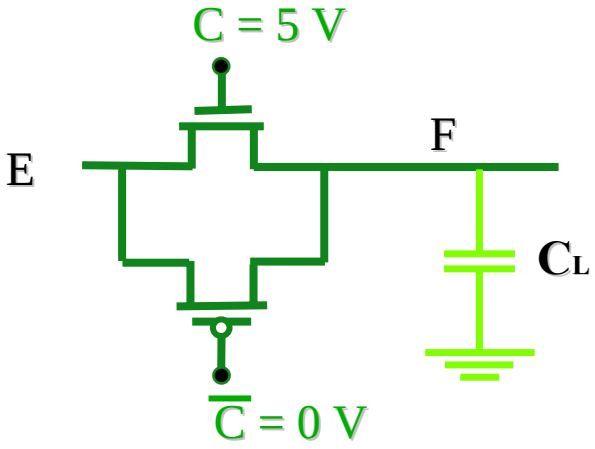
Chaves NMOS



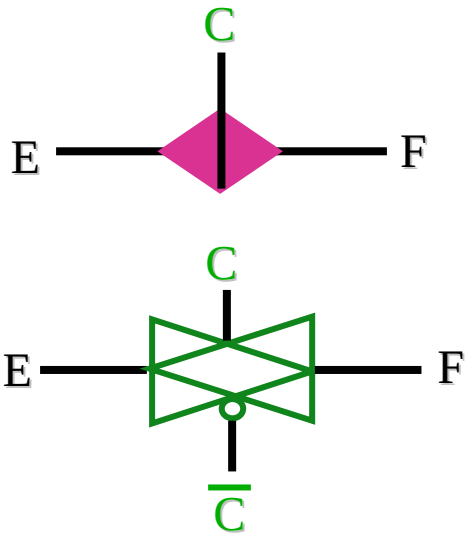
- V_F está abaixo de V_C para NMOS "ON"
- V_F não consegue atingir **5V**, mas **5V** $-V_{Tn}$
- O transistor NMOS passa um '0' forte (GND) e um '1' fraco ($V_C - V_{Tn}$)

Portas Lógicas

Chaves CMOS ou Porta de Transmissão (Transmission gate)



Símbolos:



OBS: o transistor PMOS passa um '0' fraco e um '1' forte

o transistor NMOS passa um '0' forte e um '1' fraco

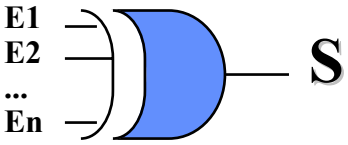
R_{eq} de uma chave CMOS: cerca de 10 KΩ

Desvantagem: A chave é controlada por C e $\overline{C}$

Portas Lógicas

Porta XOR (porta 'OU Exclusivo')

Símbolo:



Equação Booleana: $S = E1 \oplus E2$

$S = E1 \oplus E2 \oplus ... \oplus En$

Tabela Verdade:

E1	E2	S
0	0	0
0	1	1
1	0	1
1	1	0

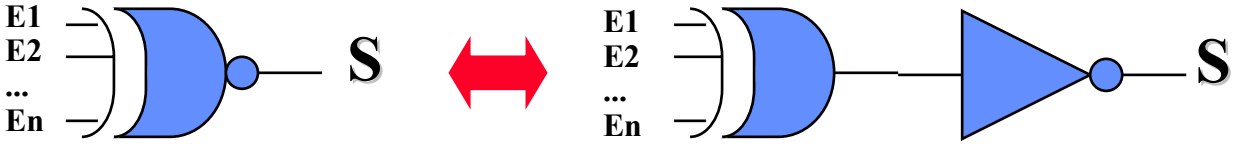
E1	E2	...	En	S
0	0		0	0
0	1		1	0
1	0		0	1
1	1	...	1	1

Dica: A SAÍDA É 1 SOMENTE QUANDO HOUVER UM NÚMERO ÍMPAR DE ENTRADAS COM VALOR 1.

Portas Lógicas

XNOR (porta 'Não OU Exclusivo')

Símbolo:



Equação Booleana: $S = \overline{E1 \oplus E2}$

$S = \overline{E1 \oplus E2 \oplus \ldots \oplus En}$

Tabela Verdade:

E1	E2	S
0	0	1
0	1	0
1	0	0
1	1	1

E1	E2	...	En	S
0	0		0	1
0	1		1	1
1	0		0	0
1	1	...	1	0

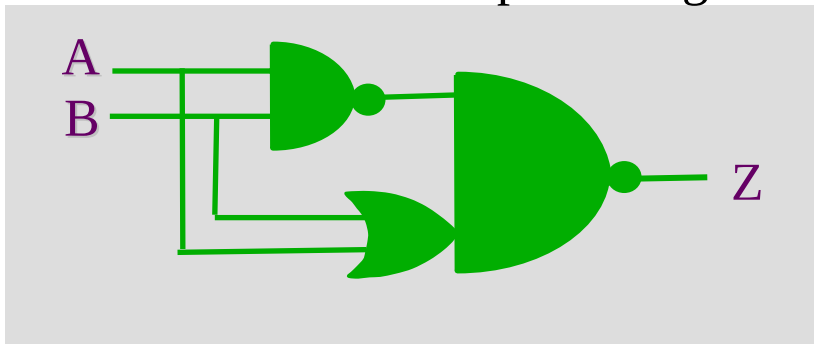
Dica: A SAÍDA É 1 SOMENTE QUANDO HOUVER UM NÚMERO PAR DE ENTRADAS COM VALOR 1. CONTRÁRIO DA PORTA XNOR.

Portas Lógicas

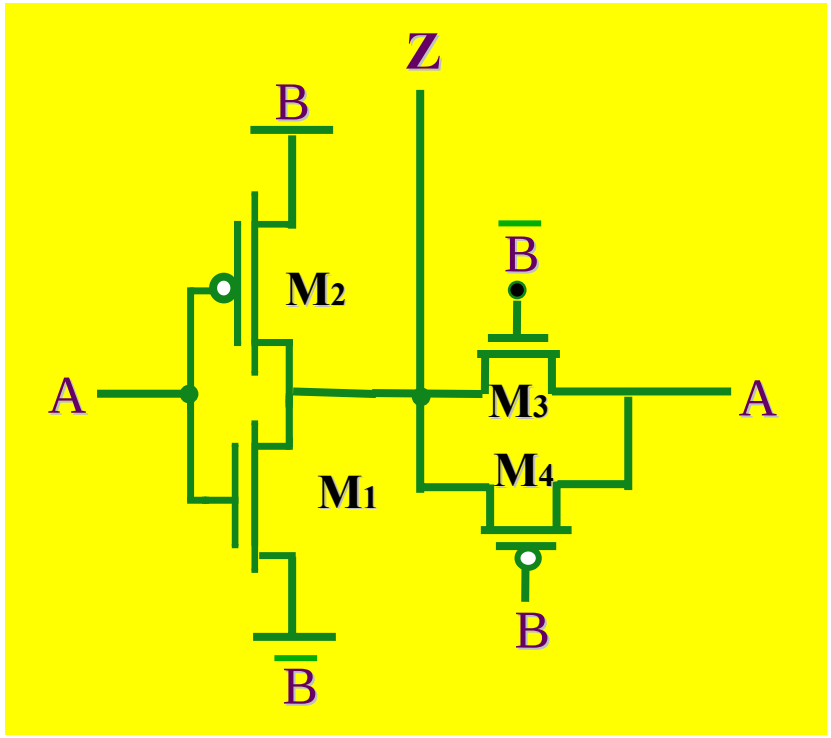
Lógica com chaves CMOS

XNOR e XOR

XNOR realizado com portas lógicas

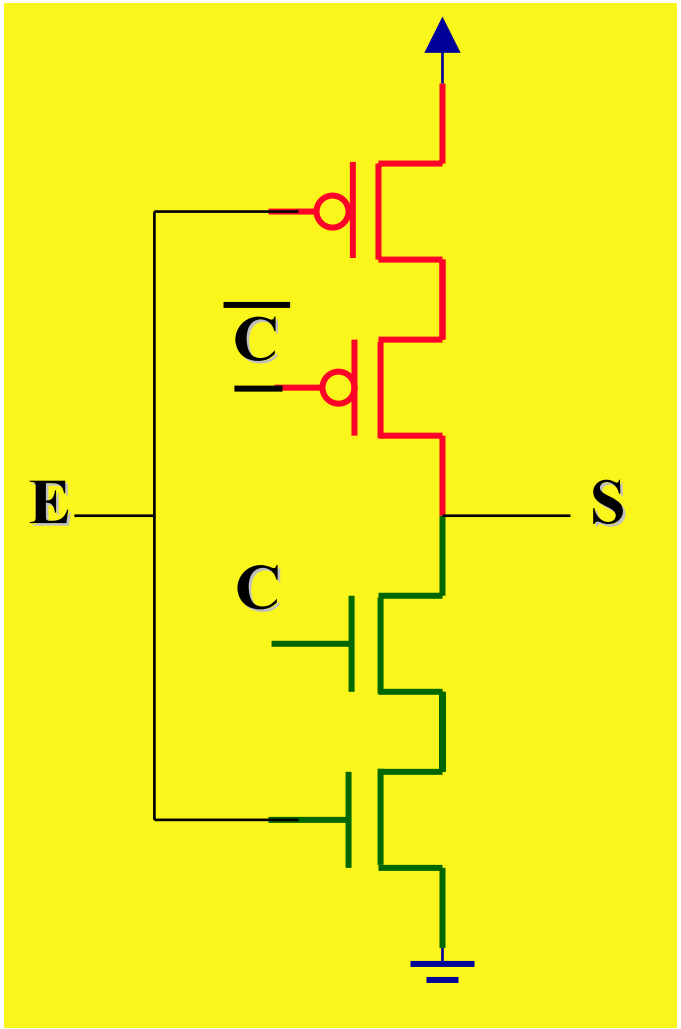


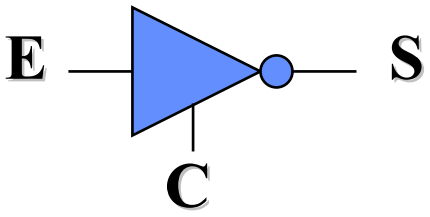
XOR realizado com transistores de passagem



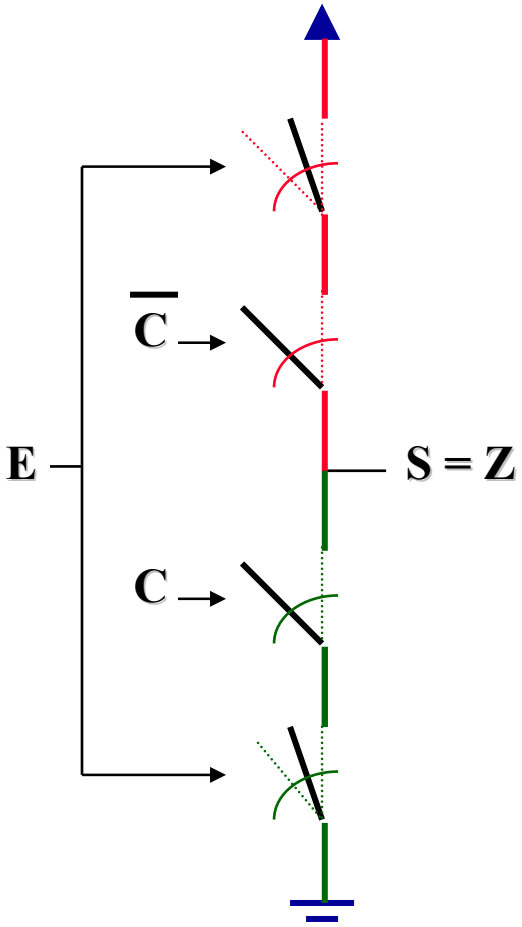
Alta Impedância (Z)

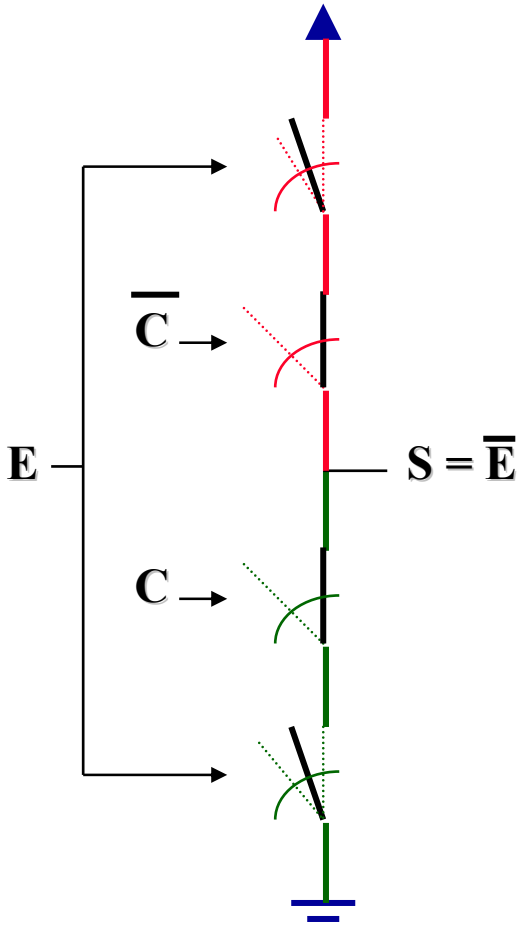
Inversor Tri-State (INVTR)



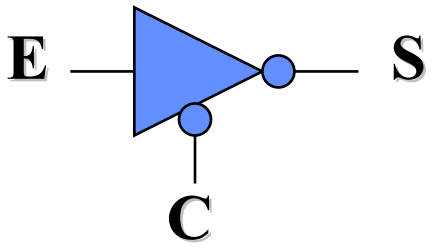


E	C	$\overline{C}$	S
0	0	1	Z
1	0	1	Z
0	1	0	1
1	1	0	0





Outra opção... (*controle negado*)

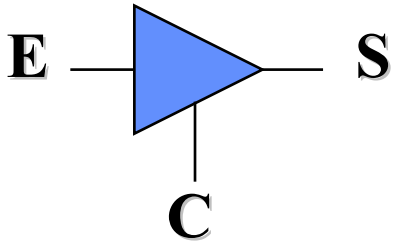


E	C	S
0	0	1
1	0	0
0	1	Z
1	1	Z

OU

C	S
0	$\overline{E}$
1	Z

Buffer Tri-State (BUFTR)

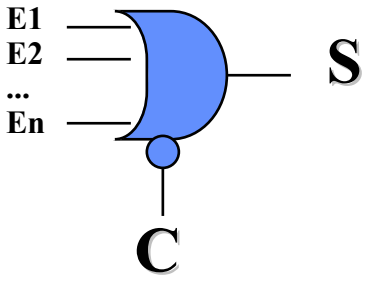


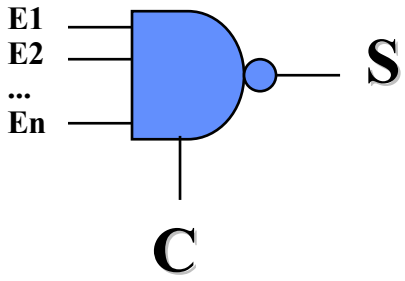
E	C	S
0	0	0
1	0	1
0	1	Z
1	1	Z

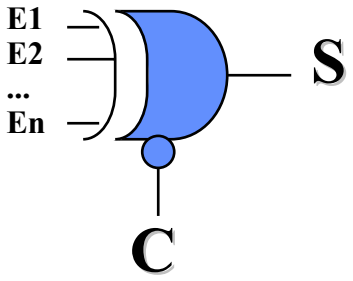
OU

C	S
0	Z
1	E

*** PODE-SE PENSAR EM QUALQUER PORTA LÓGICA COM SAÍDA TRI-STATE OU ALTA-IMPEDÂNCIA (Z) !!!**

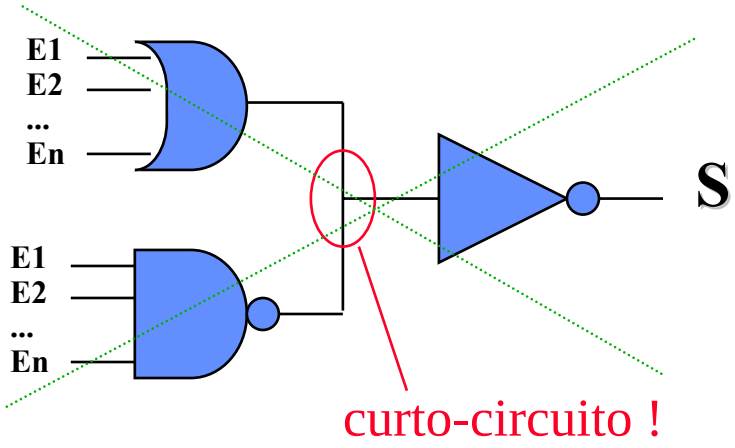




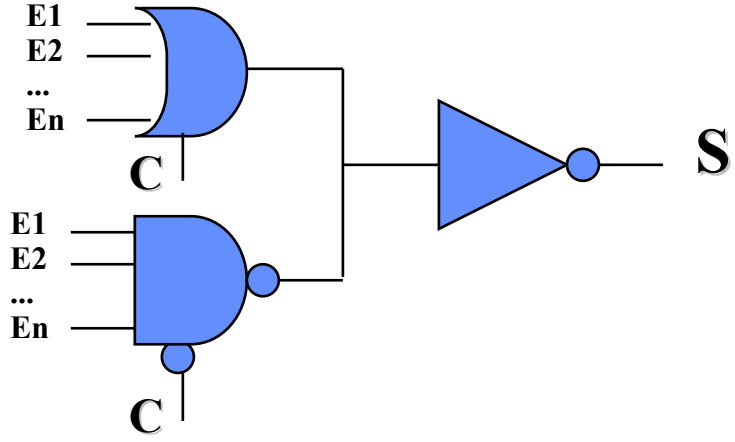


Uso de Porta Tri-State ...

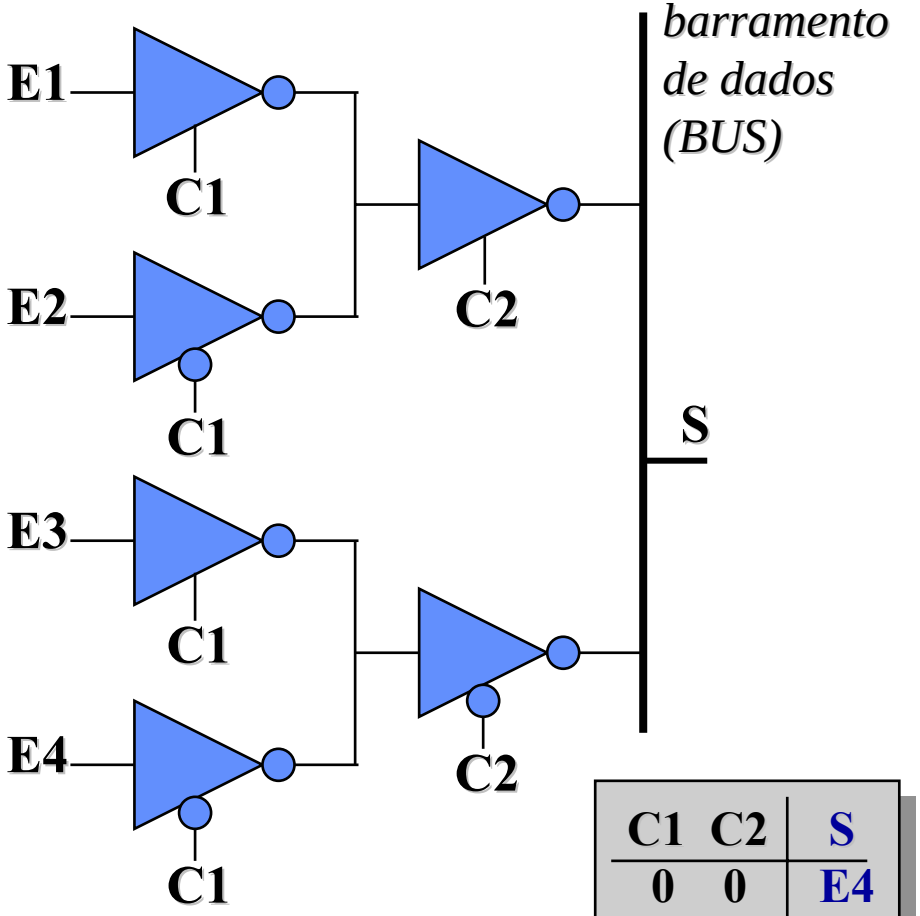
* NÃO É PERMITIDO EM CMOS :



* CORRETO :



* BARRAMENTO DE SINAIS :



C1	C2	S
0	0	E4
1	0	E3
0	1	E2
1	1	E1