INF01 118

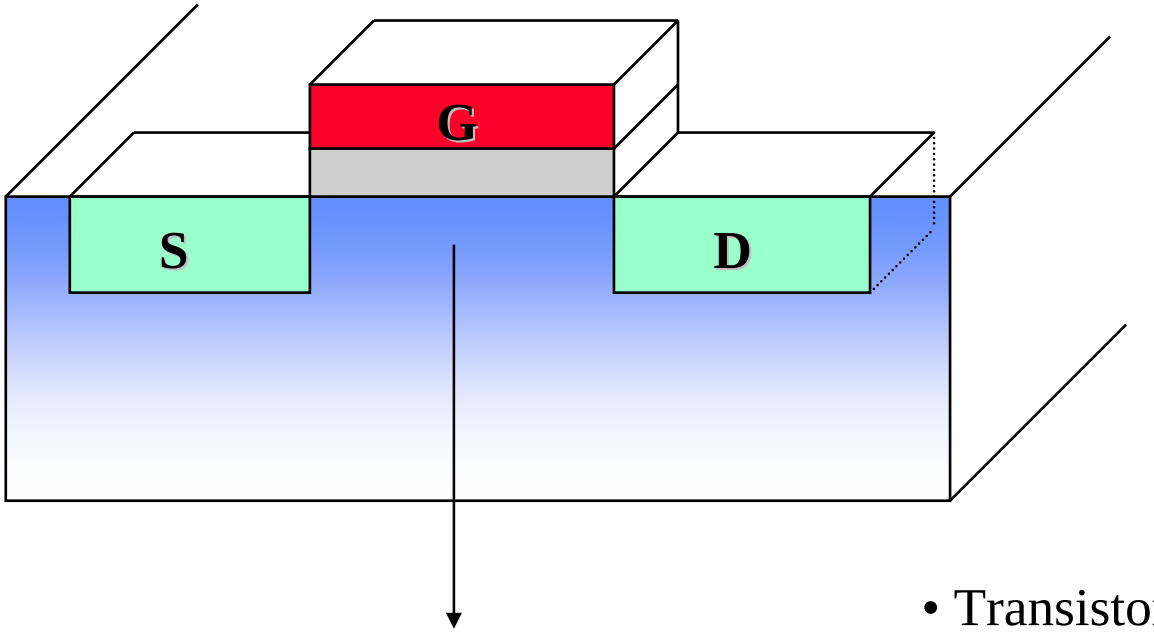
Técnicas Digitais para Computação

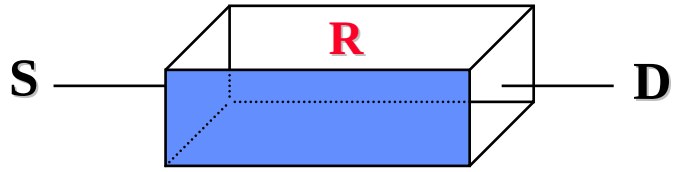
Dimensionamento de Transistores
Parasitas RC em Portas CMOS

UFRGS

Aula 6

Resistência de Canal do Transistor





canal do transistor

- Transistor não é ‘chave ideal’.
- Canal do transistor $\Rightarrow$ resistência
- Transistor conduzindo:

  resistência pequena ($R \Rightarrow 0$)
- Transistor ‘cortado’:

  resistência muito alta ($R \Rightarrow \infty$)

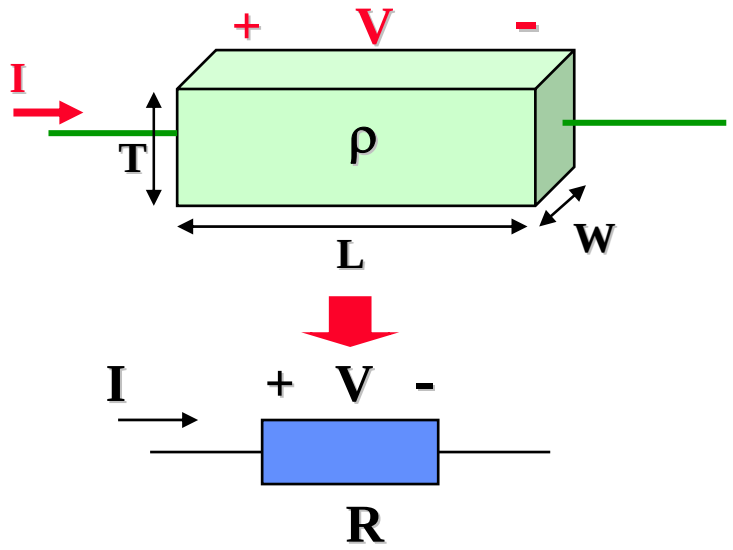
Dimensionamento de Transistor MOS

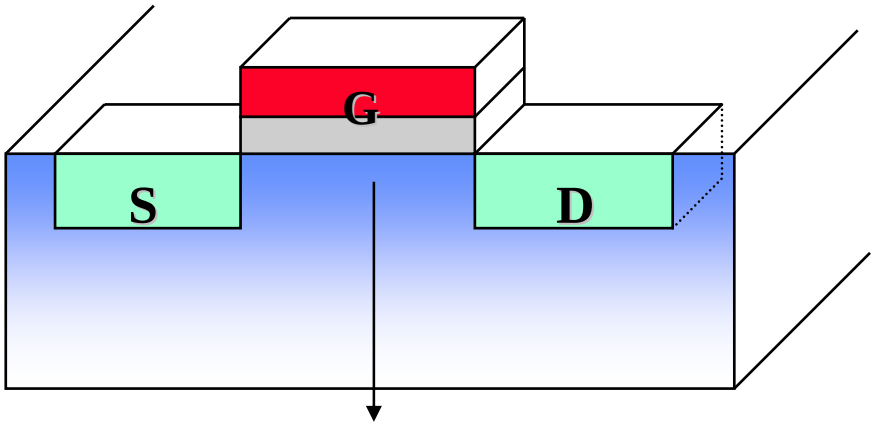
Resistência

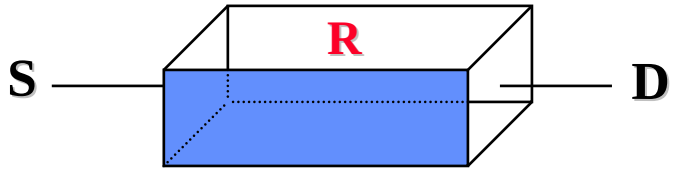
$$R = \rho \cdot \frac{L}{W \cdot T}$$

Lei de Ohm:

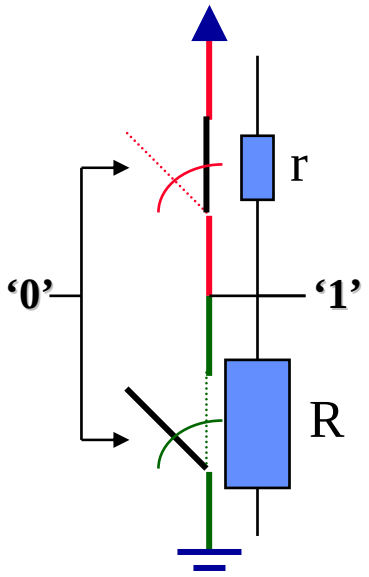
$$I = V / R$$



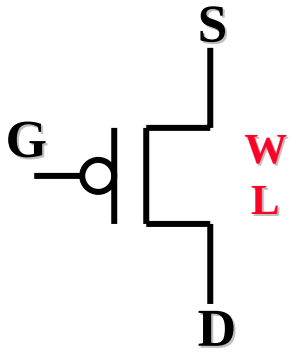




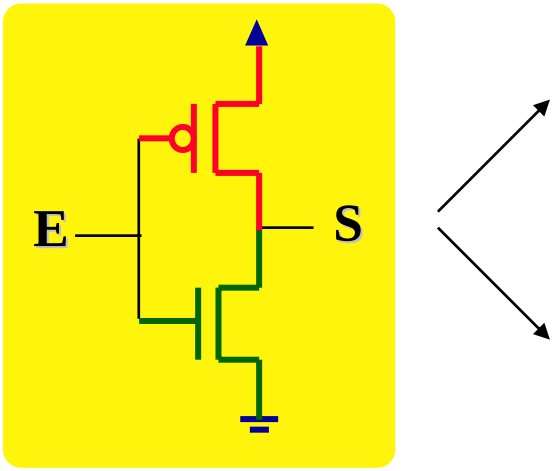
canal do transistor

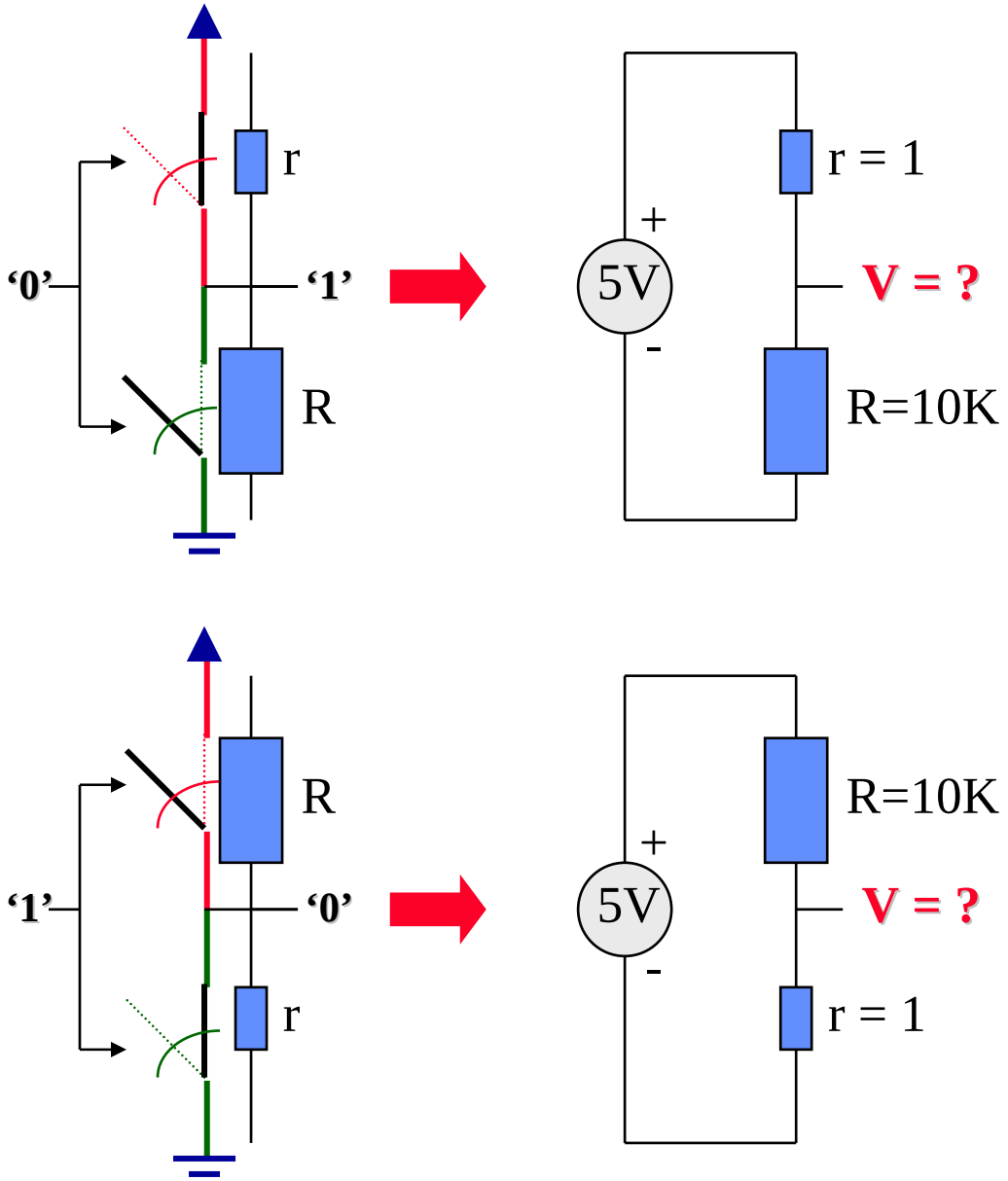


$$\begin{cases} W\uparrow : r\downarrow, C\uparrow \\ L\uparrow : r\uparrow, C\uparrow \end{cases}$$

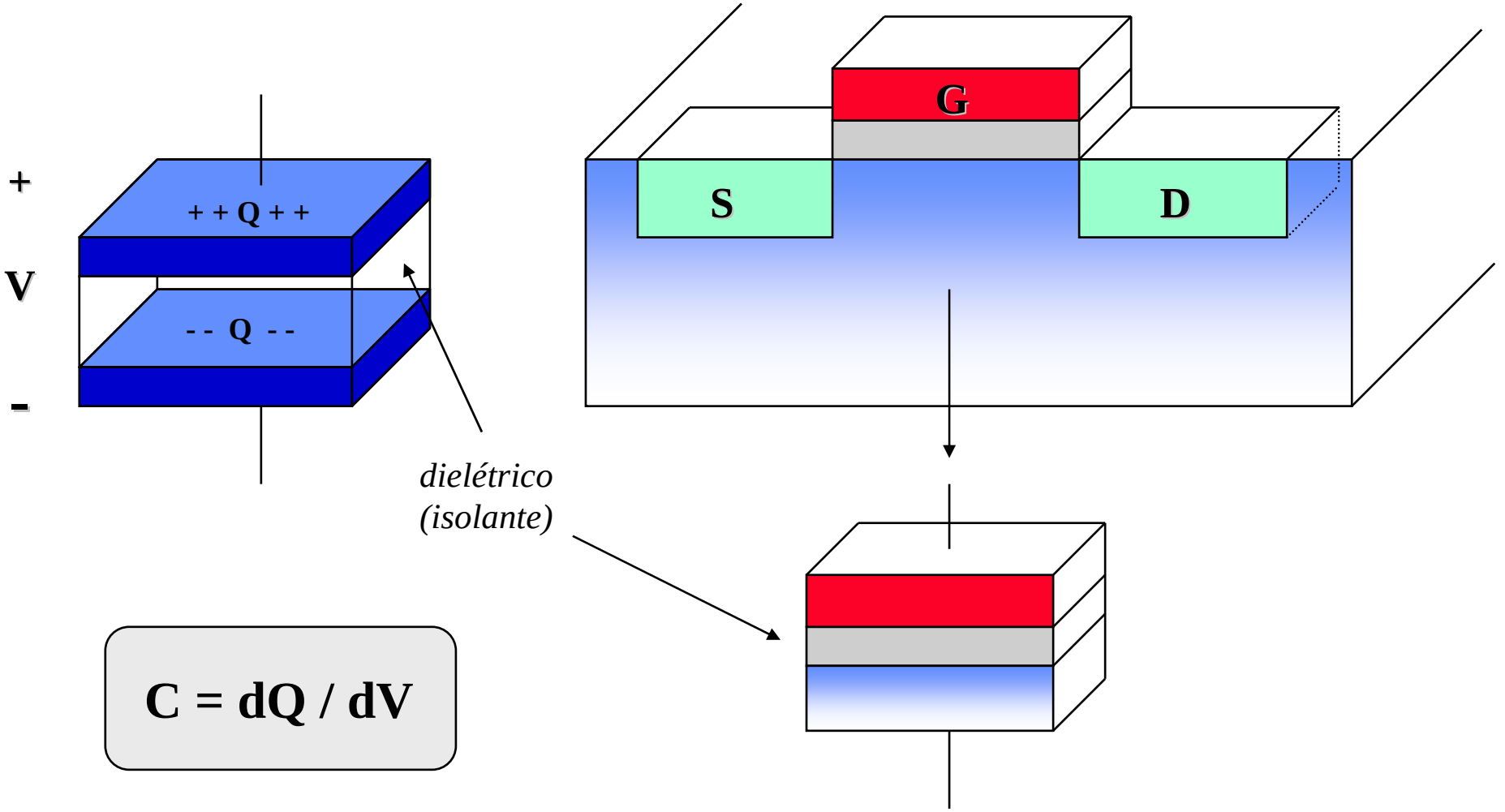


Inversor CMOS : (resistência parasita)



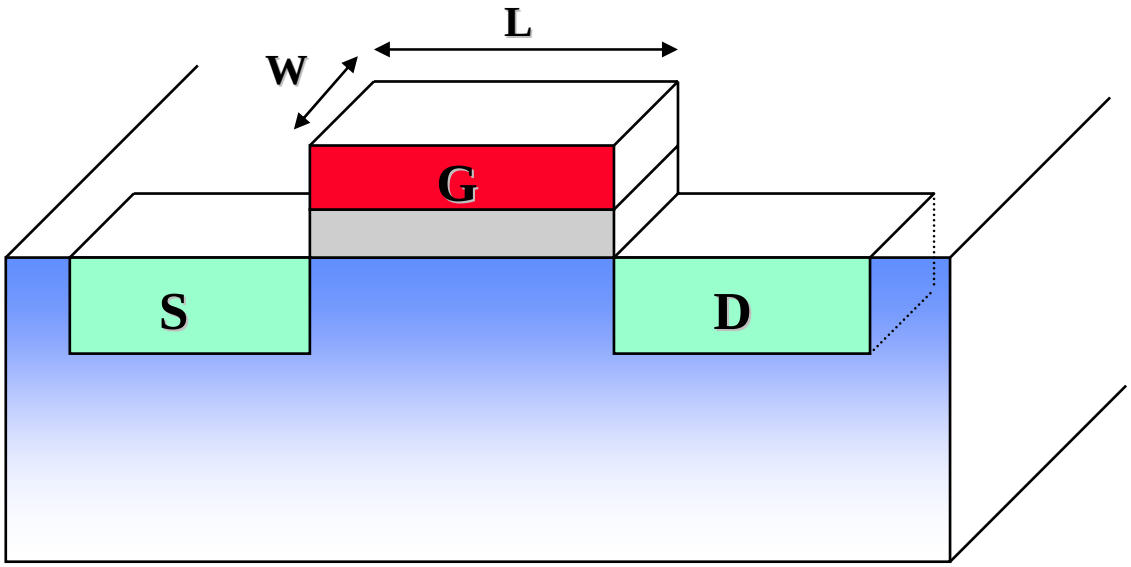


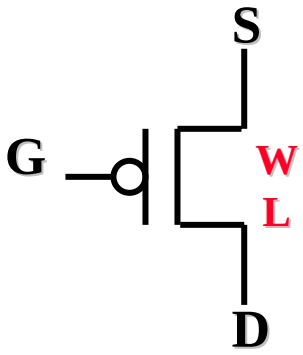
Capacitância (C)



$$C = dQ / dV$$

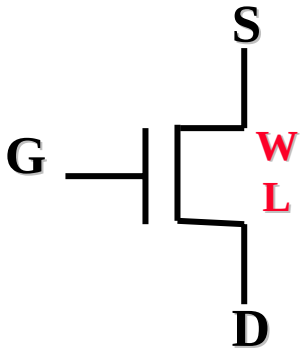
Dimensionamento do Transistor MOS



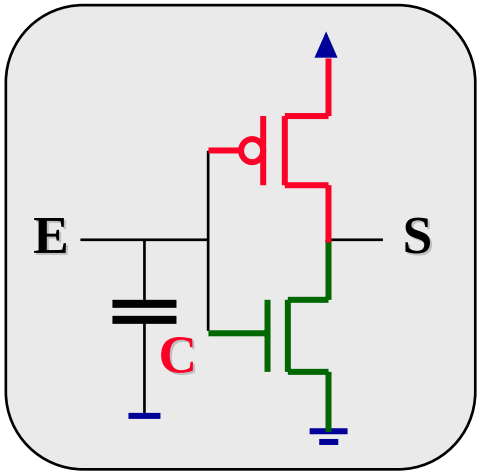


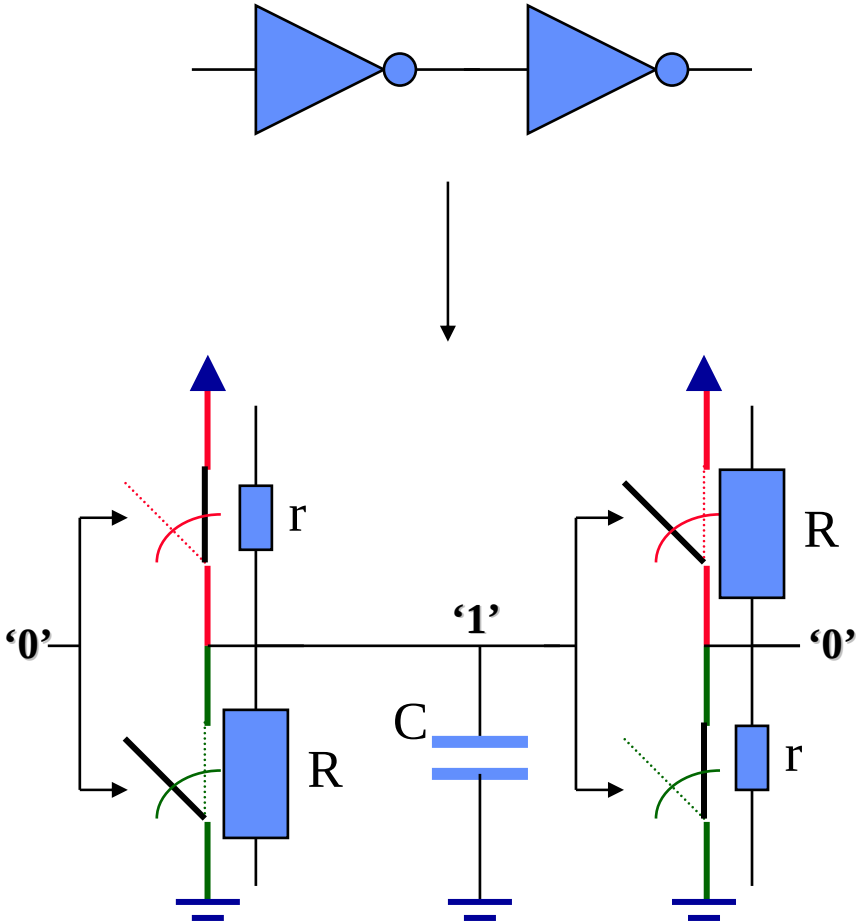
Análise de ‘r’ (‘*on*’) e C:

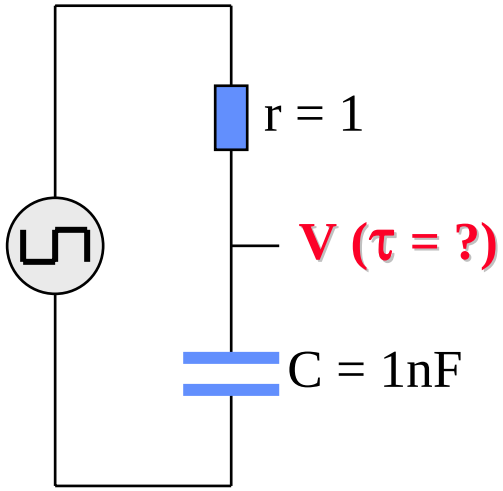
- W ↑ : r ↓ e C ↑
- L ↑ : r ↑ e C ↑



Inversor CMOS : (capacitância parasita)

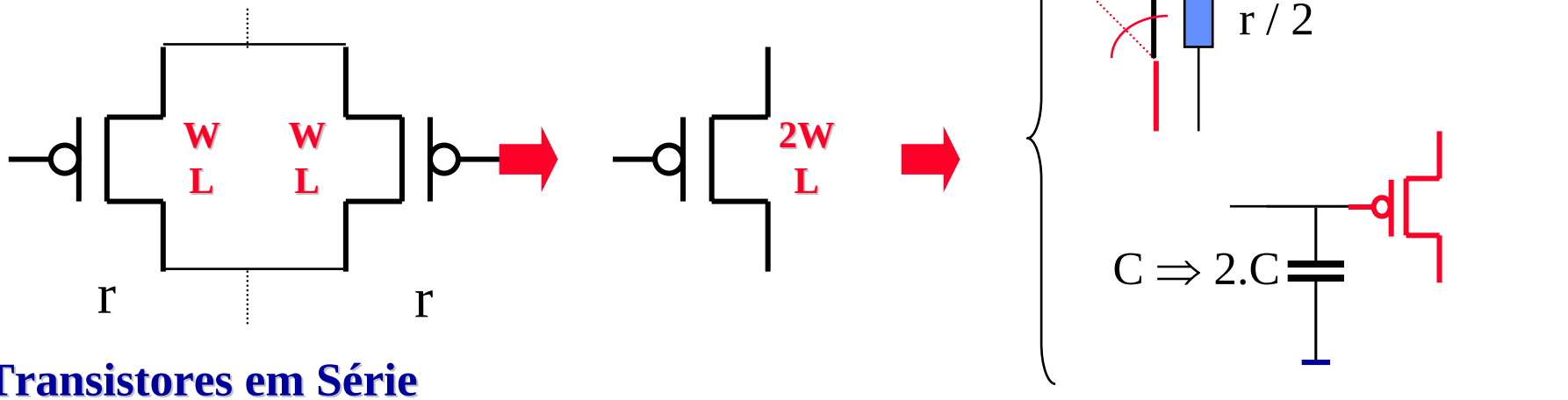




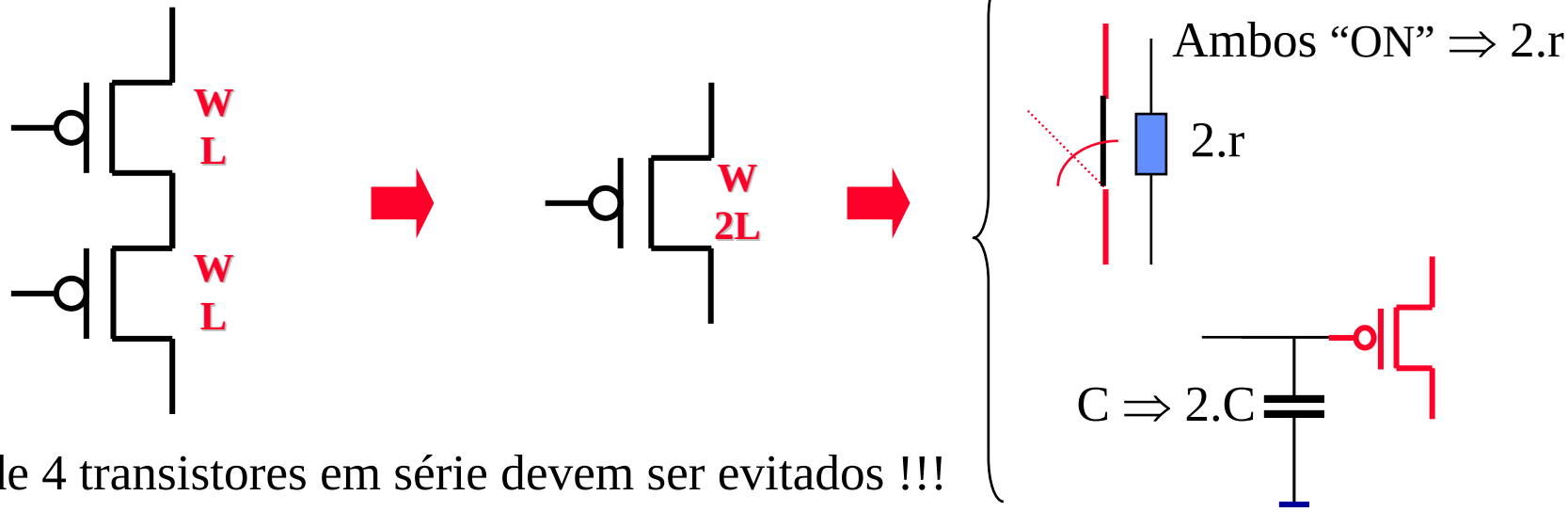


Associação de Transistores

Transistores em Paralelo



Transistores em Série

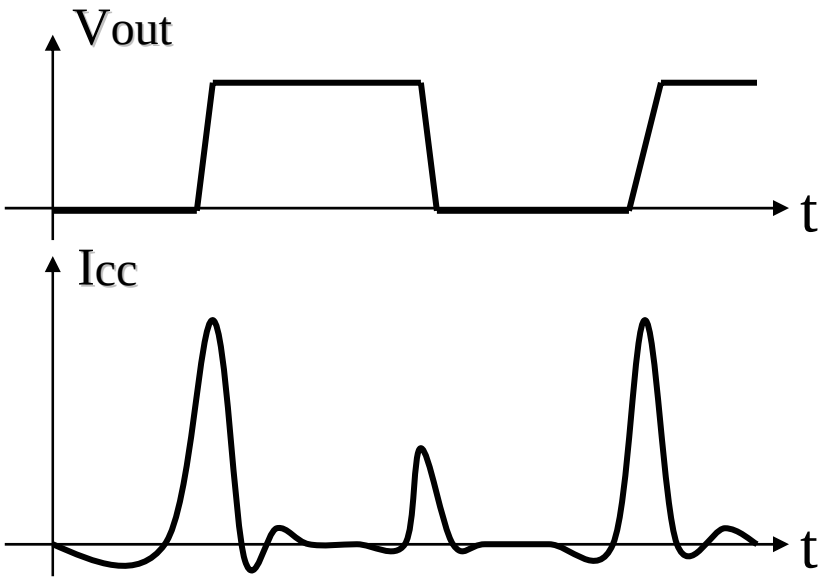


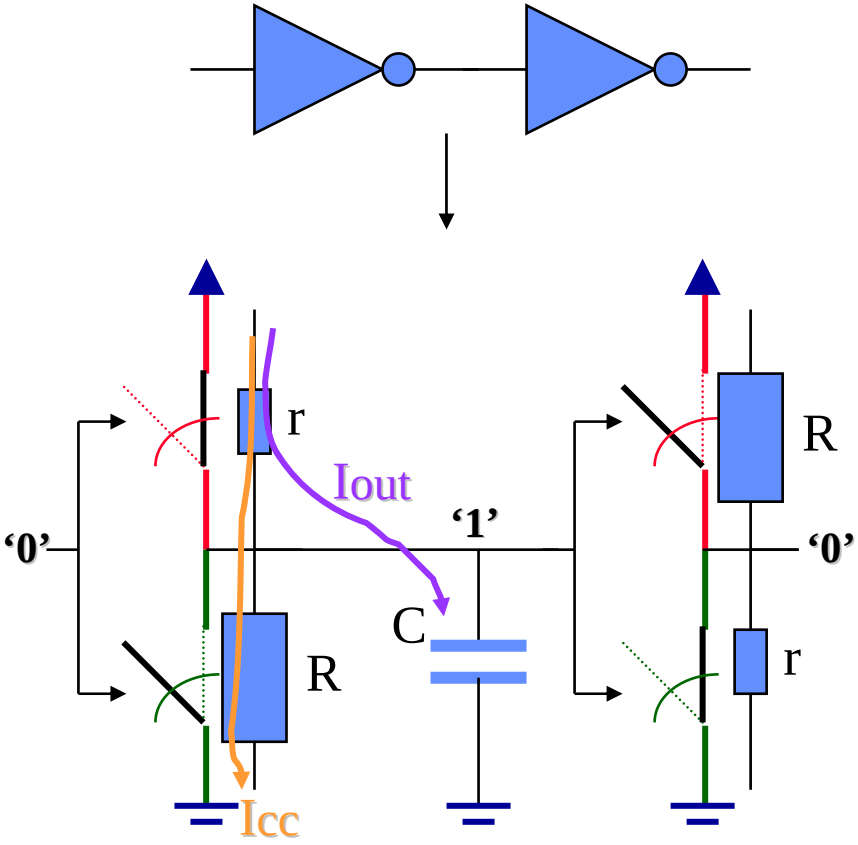
* Mais de 4 transistores em série devem ser evitados !!!

Consumo (Dissipação de Potência)

- Corrente de Carga: Iout
- Corrente de Curto-Circuito: Icc

- consumo estático ≈ 0
- consumo dinâmico (transição) = Iout + Icc
- consumo total = estático + dinâmico





* A variação de W e L afeta o tempo de transição dos sinais e o consumo da porta lógica.