Estudo dos Efeitos da Radiação em Circuitos Integrados e Desenvolvimento de Técnicas de Tolerância a Falhas de Efeito Transiente

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Aula 10
Técnicas de tolerância a falhas em FPGAs programados por Antifuse e Flash

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SEE Mitigation Techniques

• By Design
  – Need matrix modifications (FPGA fabricant)

• By high-level (VHDL, logic, software, others)
  – Implemented by the user
  – May need design flow assistance
Protecting SEU by DESIGN

- **Control Logic**
  - Logic redundancy design
- **Clock Network**
  - Eliminate small leaves in the clock tree
- **User flip-flop**
  - Hard-wired triple redundant latch for master and slave
- **Embedded SRAM**
  - EDAC macro in FPGA design software (ACTgen)
  - Hamming code detect two error bits, correct one error bit
- **Glancing-angle-strike double upset simulated by SPICE and SpaceRad to determine the bit separation**
- **Charge-sharing double upset simulated by 3D mixed mode to determine the bit separation**
Case Study I: RTAX - TMR flip-flop [Wang et al, NSREC, 03]

Logic schematic of the triple redundant latch in the SEU hardened user flip-flop.

[Diagram of the triple redundant latch]
3D simulations for Embedded Memory

Schematic showing the 3D device structure and SPICE circuit net. The device structure assumes the worst scenario, NMOSFET junction at high state is the sensitive area. Ion strikes at the sensitive junction of SRAM2 to simulate single-bit upset. Ion strikes at the center in all three directions of the structure to simulate double-bit upset.

[Fig A] Ion strike 0°-tilt at center of junction
[Fig B] Ion strike 60°-tilt at center of structure

[Wang et al, NSREC, 03]
Results

3D mixed mode simulation showing ion-strike-induced transient voltages of the sensitive junctions in SRAM1 and SRAM2. Heavy ion with LET of 60 MeV•cm²/mg and 60° tilt strikes a location of equal distance to SRAM1 and SRAM2. The first voltage drop near 10 ps is due to the electric field collapsing. The main voltage drop near 10 ns is due to the charge collection of the diffused carriers at the sensitive junctions.

[Wang et al, NSREC, 03]
Case-Study II: Actel Flash-based FPGA
TMR in Volatile FPGAs as seen...
Non-Volatile FPGAs

Non-Volatile FPGA: TMR is not required for Combinational Logic or the scrubbing of the configuration memory
Non-Volatile FPGA: SEU in ffps - TMR

1. Sequential Logic should be TMR’d.
2. Combinational Logic should be filtered at the inputs of the sequential logic.
3. No Scrubbing of the configuration memory is required because the configuration memory simply does not upset.

[Rezgui et al, MAFA, 07]
Is SET important?

- SET Characterization

M. Baze, Boeing, NSREC 2006.

FPGA Implementation

SET Cross-Section Measurements

SET Pulse Width Measurements & Mitigation

[Rezgui et al, MAFA, 07]
Proposed SET Mitigation Techniques

[Rezgui et al, MAFA, 07]
SET Radiation Data

[Rezgui et al, MAFA, 07]

- SEU in DFF can be mitigated by TMR
- At low frequency (2 MHz), no SET was observed on the IOs (including the Clock).
- At 16 MHz, SET on the IOs (including the Clock) were seen only at very high LET (68 MeV/cm²/mg).

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programados por Antifuse e Flash
SET Mitigation for IOs

Each set of tripped Input or Output must use 3 different IO banks

Design: 486 LCI: So 100% of logic tiles are used

[Rezgui et al, MAFA, 07]
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SET Radiation Data  
[Rezgui et al, MAFA, 07]
Case-studies

[Rezgui et al, MAFA, 07]

Partial SEE Mitigation

Without Mitigation of the IO Banks

- SET Filtering (Comb. Logic) + TMR (Seq. Logic)
- 75% of the FPGA Core
- All IOs are tripled and separated on 3 # IO Banks

Full SEE Mitigation

With Mitigation of the IO Banks

- TMR ALL
- 85% of the FPGA Core
- All IOs are tripled and separated on 3 # IO Banks
More Radiation Results

[Rezgui et al, MAFA, 07]

**Partial SEE Mitigation**
- TMR_ALL 50MHz
- SET Filtering(6LCI) 50MHz

**Full SEE Mitigation**
- SET_Filtering(6LCI) 50MHz
- TMR_ALL 50MHz

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**TMR-ALL**
- XS/IO-Bank = 2 x 10^-6 cm²/IO-Bank
- 10 % time penalty

**SET Filtering (+ TMR)**
- XS/IO-Bank = 2 x 10^-6 cm²/IO-Bank
- XS/IO-Bank = 2 x 10^-7 cm²/IO-Bank if Clock filtered
- 30 % time penalty

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**TMR-ALL**
- Full SEE Immunity
- 10 % time penalty

**SET Filtering (+ TMR)**
- A delay of 6 LCI guarantee SEE immunity for LET < 43 MeV-cm²/mg
- 30 % time penalty
More Radiation Results...

[Rezgui et al, MAFA, 07]
Another Flash-based FPGA

AGL - IGLOO

Técnicas de tolerância a falhas em FPGAs programados por Antifuse e Flash

[Rezgui et al, MAFA, 07]
AGL Characterization

[Rezgui et al, MAFA, 07]
Comparison

[Rezgui et al, MAFA, 07]

To Be Done

- SET Characterization (measurements of SET pulse widths)
- SEE Characterization in Freeze Mode

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Summary

Complete SEE Characterization & Mitigation of A3P => RTA3P

- TMR All
  - Full SEE Immunity
  - 4 times Hardware overhead; 15% time penalty
- SET Filtering (combinational logic) + TMR (sequential logic)
  - A delay of 6 LCI guarantee SEE immunity for LET < 43 MeV·cm²/mg
    ▶️ 30% time penalty
  - A delay of 8 LCI guarantee Full SEE immunity for LET < 96 MeV·cm²/mg
    ▶️ 40% time penalty
  - Logic Duplication guarantee SEE immunity for LET < 43 MeV·cm²/mg
    ▶️ 10% time penalty
- Embedded Systems Applications: Processors (8051, ARM, FT-Leon3, DSP...)
- Flight Parts should be available in 2009

AGL: Lowest Power FPGA

- SEE Characterization & Mitigation
- Results show the same radiation sensitivity as for the A3P
- TBD: SEE Characterization in Freeze Mode

[Rezgui et al, MAFA, 07]