IEEE 1149.1 JTAG Boundary Scan Standard

• Bed-of-nails tester
• Motivation
• System view of boundary scan hardware
• Elementary scan cell
• Test Access Port (TAP) controller
• Boundary scan instructions
• Summary
Bed-of-Nails Tester Concept
Bed-of-Nails Tester
Motivation for Standard

- *Bed-of-nails printed circuit board* tester gone
  - We put components on both sides of PCB & replaced DIPs with flat packs to reduce inductance
    - Nails would hit components
  - Reduced spacing between PCB wires
    - Nails would short the wires
  - Need standard System Test Port and Bus
  - Integrate components from different vendors
    - Test bus identical for various components
    - One chip has test hardware for other chips
Purpose of Standard

- Lets test instructions and test data be serially fed into a *component-under-test* (CUT)
  - Allows reading out of test results
- JTAG can operate at chip, PCB, & system levels
- Allows control of tri-state signals during testing
- Lets other chips collect responses from CUT
- Lets system interconnect be tested separately from components
- Lets components be tested separately from wires
System Test Logic

- Boundary Register Cell
- System Circuitry
- Device ID Register
- Bypass Register
- Instruction Register (Control Signals)
- TAP Controller
- TDI
- TCK
- TMS
- TRST*
- TDO
Instruction Register Loading with JTAG
Boundary Scan Chain View
Elementary Boundary Scan Cell
Serial Board / MCM Scan

Diagram showing a block diagram of Serial Board / MCM Scan with various chips (Chip 1, Chip 2, Chip 3, Chip 4) interconnected through TDI (serial data in), TDO (serial data out), TCK, and TMS signals. The diagram also highlights Boundary-scan cell, Serial test interconnect, and System interconnect.
Parallel Board / MCM Scan
Independent Path Board / MCM Scan
Tap Controller Signals

- **Test Access Port (TAP)** includes these signals:
  - **Test Clock Input (TCK)** -- Clock for test logic
    - Can run at different rate from system clock
  - **Test Mode Select (TMS)** -- Switches system from functional to test mode
  - **Test Data Input (TDI)** -- Accepts serial test data and instructions -- used to shift in vectors or one of many test instructions
  - **Test Data Output (TDO)** -- Serially shifts out test results captured in boundary scan chain (or device ID or other internal registers)
  - **Test Reset (TRST)** -- Optional asynchronous TAP controller reset
Tap Controller State Diagram
Boundary Scan Instructions
SAMPLE / PRELOAD Instruction - SAMPLE

Purpose:
1. Get snapshot of normal chip output signals
2. Put data on bound. scan chain before next instr.

On-chip System Logic

Component boundaries

Data transfer paths activated in SAMPLE mode.
SAMPLE / PRELOAD Instruction --
PRELOAD

On-chip System Logic

Data transfer paths activated in PRELOAD mode.
EXTEST Instruction

- Purpose: Test off-chip circuits and board-level interconnections
**INTEST Instruction**

**Purpose:**
1. Shifts external test patterns onto component
2. External tester shifts component responses out
RUNBIST Instruction

- Purpose: Allows you to issue BIST command to component through JTAG hardware

- Optional instruction

- Lets test logic control state of output pins
  1. Can be determined by pin boundary scan cell
  2. Can be forced into high impedance state

- BIST result (success or failure) can be left in boundary scan cell or internal cell
  - Shift out through boundary scan chain
**CLAMP Instruction**

- **Purpose:** Forces component output signals to be driven by boundary-scan register

- Bypasses the boundary scan chain by using the one-bit *Bypass Register*

- **Optional instruction**
**IDCODE** Instruction

- **Purpose:** Connects the component device identification register serially between **TDI** and **TDO**
  - In the *Shift-DR* TAP controller state

- Allows board-level test controller or external tester to read out component ID

- Required whenever a JEDEC identification register is included in the design
## Device ID Register -- JEDEC Code

<table>
<thead>
<tr>
<th>MSB</th>
<th>31 28</th>
<th>27 12</th>
<th>11 1</th>
<th>LSB</th>
<th>0</th>
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</thead>
<tbody>
<tr>
<td>Version (4 bits)</td>
<td>Part Number (16 bits)</td>
<td>Manufacturer Identity (11 bits)</td>
<td>‘1’ (1 bit)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**USERCODE** Instruction

- **Purpose**: Intended for user-programmable components (FPGA’s, EEPROMs, etc.)
  - Allows external tester to determine user programming of component

- Selects the *device identification register* as serially connected between *TDI* and *TDO*

- Required when *Device ID register* included on user-programmable component
**HIGHZ Instruction**

- **Purpose:** Puts all component output pin signals into high-impedance state

- Control chip logic to avoid damage in this mode

- Optional instruction
BYPASS Instruction

- Purpose: Bypasses scan chain with 1-bit register
## Optional / Required Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BYPASS</strong></td>
<td>Mandatory</td>
</tr>
<tr>
<td><strong>CLAMP</strong></td>
<td>Optional</td>
</tr>
<tr>
<td><strong>EXTEST</strong></td>
<td>Mandatory</td>
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</table>
Summary

- Boundary Scan Standard has become absolutely essential --
  - No longer possible to test printed circuit boards with *bed-of-nails* tester
  - Not possible to test multi-chip modules at all without it
  - Supports BIST, external testing with Automatic Test Equipment, and boundary scan chain reconfiguration as BIST pattern generator and response compacter
  - Now getting widespread usage