

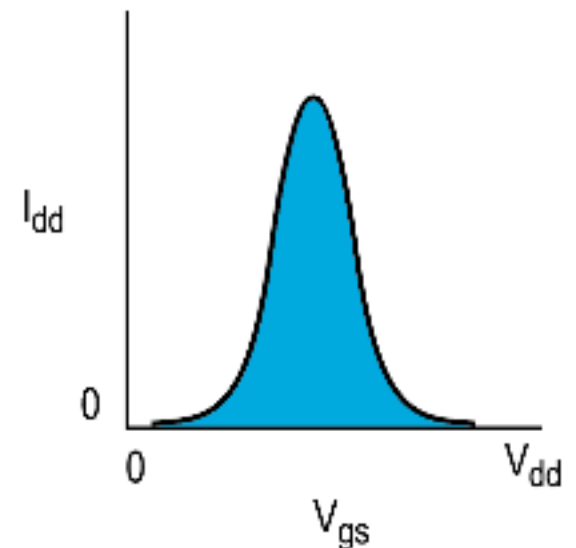
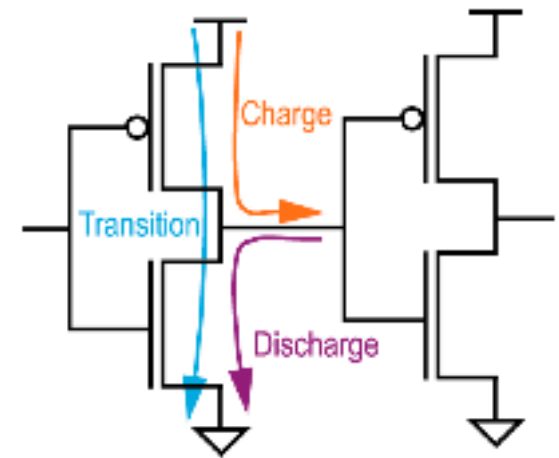
Power Estimation

FPGA

ASIC

Power in CMOS

- Total Current is composed of two types of current
 - Static
 - Dynamic
- Static Current
 - Leakage current in the turned off transistor channel
 - Ideally zero (varies with technology)
 - Fixed component of Total Current
- Dynamic Current
 - Switching of the CMOS gate when in the linear region causing transition (crowbar) current
 - Transition time is very fast
 - Relatively small component
 - Charge/Discharge of capacitive poly gate in subsequent logic element
 - XPower combines transition current with capacitive current in the power model



Calculating Power

- Calculating Dynamic Current is an overwhelmingly tedious task
- XPower is necessary for this calculation
- Dynamic Current equation

$$I_{Dynamic} = C \cdot V \cdot f$$

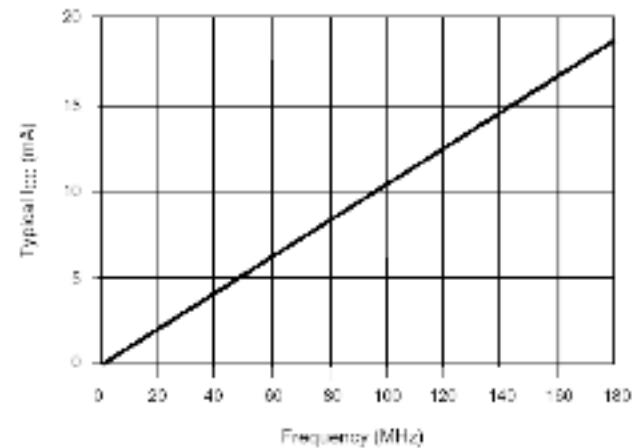
- Total Current equation

$$I_{Total} = I_{Dynamic} + I_{Static}$$

$$I_{Total} = C \cdot V \cdot f + I_{Static}$$

- Total Power equation

$$P_{Total} = I_{Total} \cdot V$$



Data Entry Method

- Data entry by hand
 - Most accurate, but most tedious method
 - Requires very detailed knowledge of FPGA architecture
 - Must specify activity rates for all nets
 - Depending on the design, it may be nearly impossible to determine activity rates for all nets
- Estimate Activity Rates tool
 - Algorithm estimates absolute frequencies of nets not yet set by the user
 - Does not estimate toggle rates
 - Alleviates the tedium, but is less accurate than data entry by hand
 - Must enter all absolute frequencies for primary I/Os by hand
 - Must enter all toggle rates by hand including buried registers

Data Entry Method

- Simulation with ModelSim XE
 - Easiest method
 - Value Change Dump (VCD) file contains frequency data
 - Simulate for sufficient length of time
 - Currently, only top level nets are contained in VCD file
 - Hand edit remaining primary I/Os and registers including buried registers
 - Use Estimate Activity Rates tool

VCD: Design file that provides detailed design activity rates for all nets. This file is generated during timing simulation using ModelSim simulator.

ModelSim (Simulação)

ModelSim XE II/Starter 5.8c - Custom Xilinx Version

File Edit View Compile Simulate Tools Window Help

Workspace

Name	Status	Type	Order	Modified
gold_fi1_multiplier16bits.vhd	?	VHDL	3	02/03/05 0
application_fi1_multiplier16bits.vhd	?	VHDL	5	02/03/05 0
multiplier_16bits.vhd	✓	VHDL	1	02/02/05 0
mem_init_rom.vhd	✓	VHDL	4	02/02/05 0
DUT_fi1_multiplier16bits.vhd	?	VHDL	2	02/03/05 0
bitadder.vhd	✓	VHDL	0	12/07/01 0

Reading C:/Modeltech_xe_starter/tcl/vsim/pref.tcl
Loading project simulacao_modelsim
ModelSim>

Compilar

Ordem de compilação

Inserir arquivos VHDL

Project : simulacao_modelsim <No Design Loaded> <No Context>

Sources in Project

- Multiplier_fault_injection1_xcv300
- xcv300-6pq240
- application_fi1_multiplier16bits-arq1 (.\vhd_files\application_fi1_multiplier16bits.vhd)
 - application_fi1_multiplier16bits.ucf
 - dut_fi1_multiplier16bits-a (.\vhd_files\DUT_fi1_multiplier16bits.vhd)
 - multiplier_16bits-a (.\vhd_files\multiplier_16bits.vhd)
 - bitadder-part (.\vhd_files\bitadder.vhd)
 - gold_fi1_multiplier16bits-arq1 (.\vhd_files\gold_fi1_multiplier16bits.vhd)
 - multiplier_16bits-a (.\vhd_files\multiplier_16bits.vhd)
 - bitadder-part (.\vhd_files\bitadder.vhd)
 - mem_init_rom-prim (.\vhd_files\mem_init_rom.vhd)

Arquivos VHDL

Processes for Source: "application_fi1_multiplier16bits-arq1"

- Add Existing Source
- Create New Source
- Design Entry Utilities
 - Create Schematic Symbol
 - Launch ModelSim Simulator
 - View Command Line Log File
 - View VHDL Instantiation Template
- User Constraints
 - Create Timing Constraints
 - Assign Package Pins
 - Create Area Constraints
 - Edit Constraints (Text)
- Synthesize - XST
 - View Synthesis Report
 - View RTL Schematic
 - Check Syntax
- Implement Design
 - Translate
 - Translation Report
 - Floorplan Design
 - Generate Post-Translate Simulation Model
 - Assign Package Pins Post-Translate
 - Map
 - Map Report
 - Generate Post-Map Static Timing
 - Manually Place & Route (FPGA Editor)
 - Generate Post-Map Simulation Model
 - Place & Route
 - Place & Route Report
 - Asynchronous Delay Report
 - Pad Report
 - Guide Results Report
 - Generate Post-Place & Route Static Timing
 - View/Edit Placed Design (Floorplanner)
 - View/Edit Routed Design (FPGA Editor)
 - Analyze Power (XPower)
 - Generate Power Data
 - Generate Post-Place & Route Simulation Model
 - Generate IBIS Model
 - Multi Pass Place & Route
 - Back-annotate Pin Locations
 - Back-annotate Pin Report
 - View Locked Pin Constraints
 - Generate Programming File
 - Programming File Generation Report
 - Generate PROM, ACE, or JTAG File
 - Configure Device (MPACT)

Module View Snapshot View Library View

Ver detalhes

Análise de potencia

Criar .bit

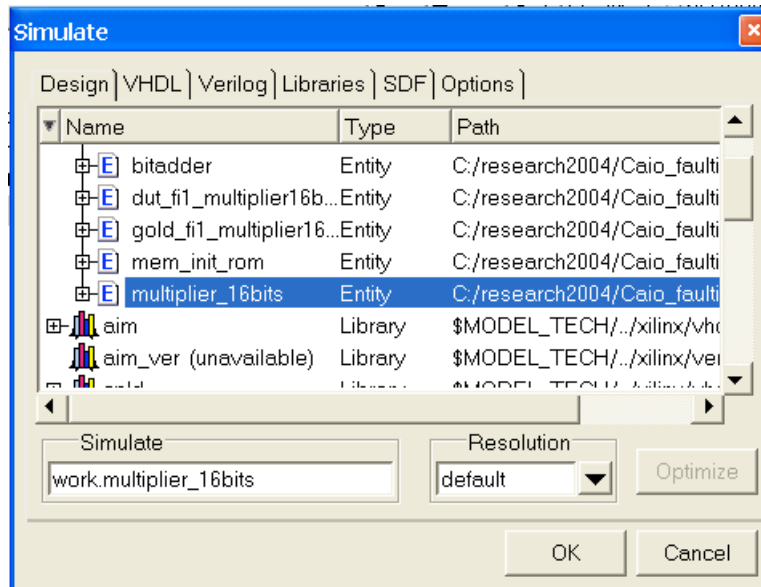
Definir pinos

Definir posicionamento da logica

Implementação na matriz

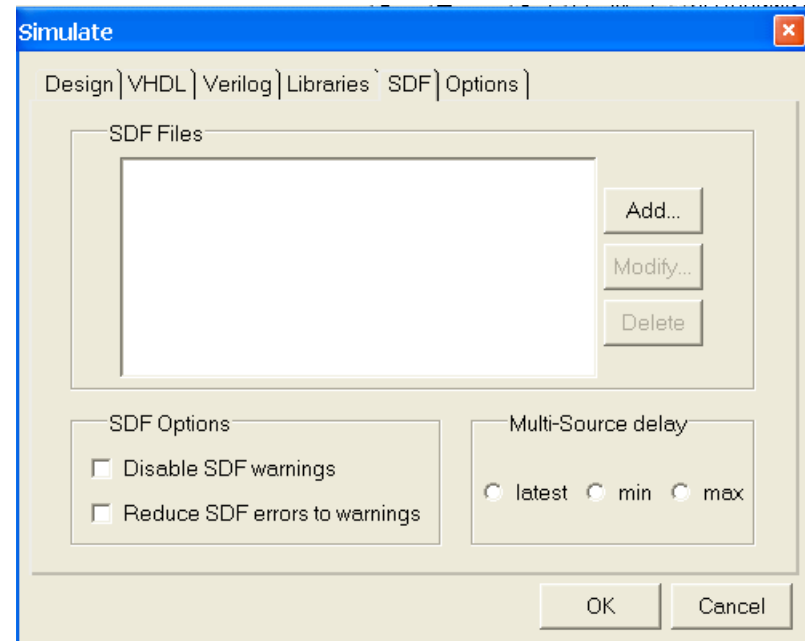
Gerar modelo de atraso para simulação

Programar



- Escolher qual arquivo compilado queres simular
- Caso haja hierarquia, escolha o de maior hierarquia para simular o conjunto.

Para simular com atraso, debes inserir o **SDF file** gerado pela ferramenta de mapeamento, posicionamento e roteamento do ISE.



View > signals

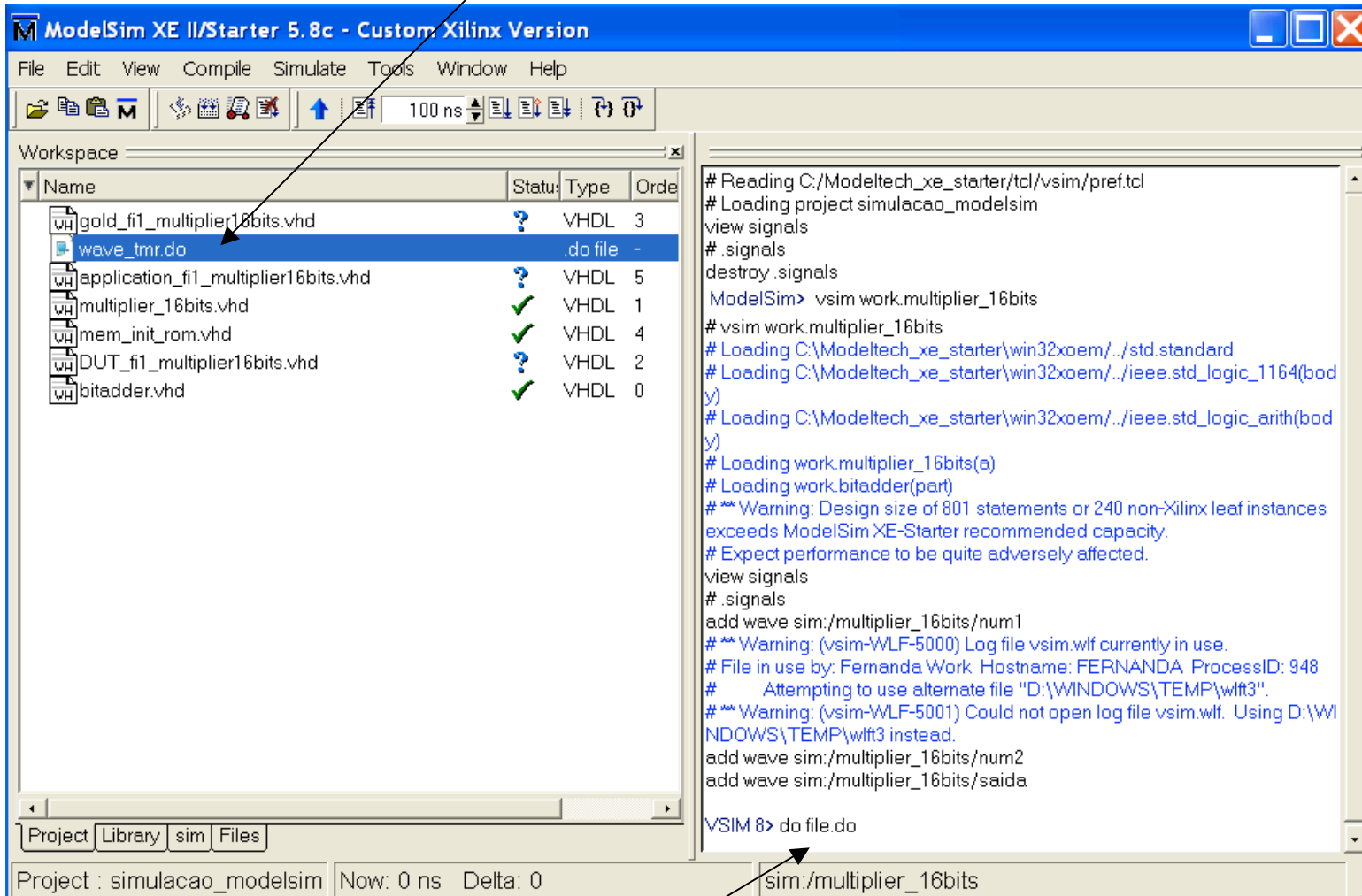
The image shows two windows from a software application. The top window, titled "signals", has a menu bar with "File", "Edit", "View", "Add", "Tools", and "Window". The "Wave" menu is open, showing options: "Selected Signals", "Signals in Region", and "Signals in Design". Below the menu is a list of signals with columns for Name, Value, and Location. The signals listed are num1, num2, saida, x0y0 through x0y10. The bottom window, titled "wave - default", has a menu bar with "File", "Edit", "View", "Insert", "Format", "Tools", and "Window". It contains a waveform viewer with a toolbar and a list of signals. The signals listed are /multiplier_16bit... with values UUUUUUUUUUUU. The waveform viewer shows a time axis from 0 ns to 1 us, with a cursor at 0 ns.

sim:/multiplier_16bits

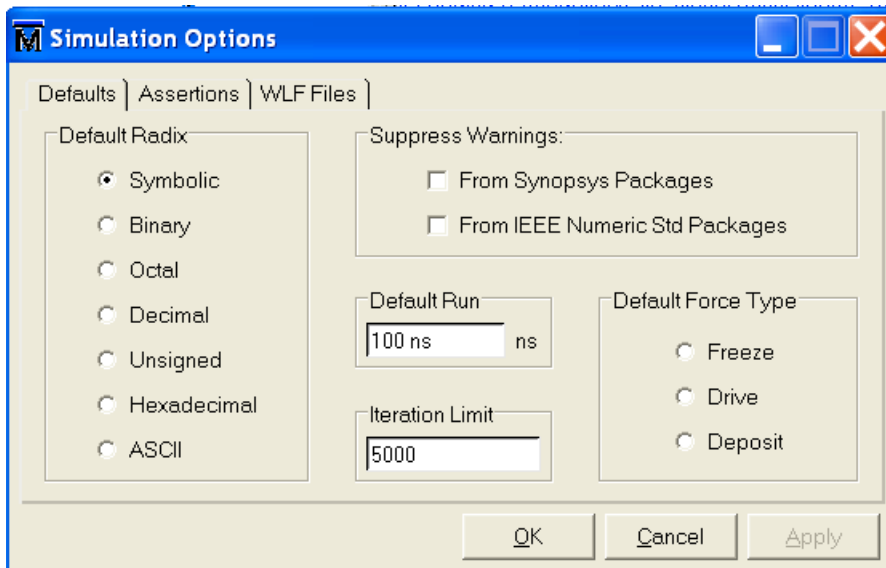
0 ns to 1 us

Podes salvar a configuração como arquivo file.do

Outro arquivo .do para simulação



Comando: do file.do



Configurar corretamente as opções de simulação:

-Tipo de dados que iras inserir na entrada conforme file.do

-Tempo de simulação é muito importante.

```
vcd file multiplicacao_16bits_power_noreg.vcd
vcd on
vcd add multiplier_16bits/*
```

Usado para estimar potência depois na ferramenta XPOWER

```
force num1 1024 0ns, 1025 50ns,1026 100ns,2333 150ns,4567 200ns,2987 250ns, 9056 300ns, 167 350ns, 13 400ns,1999 450ns,2349 500ns,
17758 550ns, 23450 600ns, 10875 650ns, 1345 700ns,1024 750ns,1000 800ns,1028 850ns,2333 900ns,4567 950ns,2987 1000ns,
1024 1050ns, 1025 1100ns, 1026 1150ns, 2333 1200ns, 4567 1250ns, 2987 1300ns, 9056 1350ns, 167 1400ns,
13 1450ns,1999 1500ns,2349 1550ns, 17758 1600ns, 23450 1650ns, 10875 1700ns, 1345 1750ns,
1024 1800ns, 1000 1850ns, 1028 1900ns, 2333 1950ns, 4567 2000ns
```

```
force num2 1024 0ns, 1025 50ns,1026 100ns,2333 150ns,4567 200ns,2987 250ns, 9056 300ns, 167 350ns, 13 400ns,1999 450ns,2349 500ns,
17758 550ns, 23450 600ns, 10875 650ns, 1345 700ns,1024 750ns,1000 800ns,1028 850ns,2333 900ns,4567 950ns,2987 1000ns,
1024 1050ns, 1025 1100ns, 1026 1150ns, 2333 1200ns, 4567 1250ns, 2987 1300ns, 9056 1350ns, 167 1400ns,
13 1450ns,1999 1500ns,2349 1550ns, 17758 1600ns, 23450 1650ns, 10875 1700ns, 1345 1750ns,
1024 1800ns, 1000 1850ns, 1028 1900ns, 2333 1950ns, 4567 2000ns
```

```
run 2000ns
```

Tempo de simulação

Xpower

The screenshot displays the Xilinx XPower application window. The main window title is "Xilinx XPower - [application_fi1_multiplier16bits]". The interface includes a menu bar (File, Edit, View, Tools, Window, Help) and a toolbar. A table in the background shows power and current data for different voltage levels.

	Voltage (V)	Current (mA)	Power (mW)
Vccint	2.5		
Dynamic		0.00	
Quiescent		9.15	
Vcco33	3.3		
Dynamic		0.00	
Quiescent		2.00	
Total Pow			

An "Open" dialog box is overlaid on the main window. It contains fields for Design File, Physical Constraints File, Settings File, and Simulation File, each with a "Browse ..." button. The "Simulation File" field is highlighted by an arrow pointing to the text "Criado pelo Modelsim VCD file". The dialog also includes "View Types" (Types selected, Hierarchical (FPGA designs only) unselected), "Do Time Based Power Analysis" (checkbox unselected), and "Launch New Design Wizard" (checkbox unselected). "OK" and "Cancel" buttons are at the bottom.

The console window at the bottom shows the following text:

```
"application_fi1_mult
-6
Loading device for application XPower from file 'v3UU.nph' in environment C:/Xilinx.
Reading constraints file: application_fi1_multiplier16bits.pcf
INFO:
-----
The power estimate will be calculated using PRODUCTION data.
-----
package pq240, speed
```

Xpower from Xilinx

- XPower allows you to change activity rate information on individual clocks, signals, logic and outputs. This allows you make specific changes to frequencies in your design to see the effect they have on power consumption. Xilinx recommends that this be done in a specific order to achieve the most accurate power estimate. The order in which you need to set or verify activity rates on different elements in your design are:
 - Set or verify voltage and ambient temperature
 - Set or verify clock frequencies
 - Set or verify input frequencies
 - Set or verify output loading
 - Set global default activity to estimated value
 - Set any specific or signal groups to estimated values

1. In the Explorer window double-click on the **Data Views** folder and then double-click on the **Types** folder. You will see four folders beneath the **Types** folder: Signals, Clocks, Logic, and Outputs.

The screenshot shows the XPower software interface for a project named 'counters.ncd'. The left sidebar shows a tree view with 'Data Views' expanded to 'Types', which contains sub-folders for 'Clocks', 'Inputs', 'Logic', 'Outputs', and 'Signals'. The main window displays a 'Summary' tab with the following data:

VCCInt (V)	Quiescent Power (mW)	Logic Block Power (mW)	Output Power (mW)
1.8	388.61	0.0	0.0
Clocks Power (mW)	Signal Power (mW)	Inputs Power (mW)	I/O's Power (mW)
17.244	0.0030	3.032	0.0
Battery Capacity (mA Hours)	Battery Life (Hours)	Total Power (mW)	
0.00	0.00	388.81	

Below the summary is a detailed table of signal power consumption:

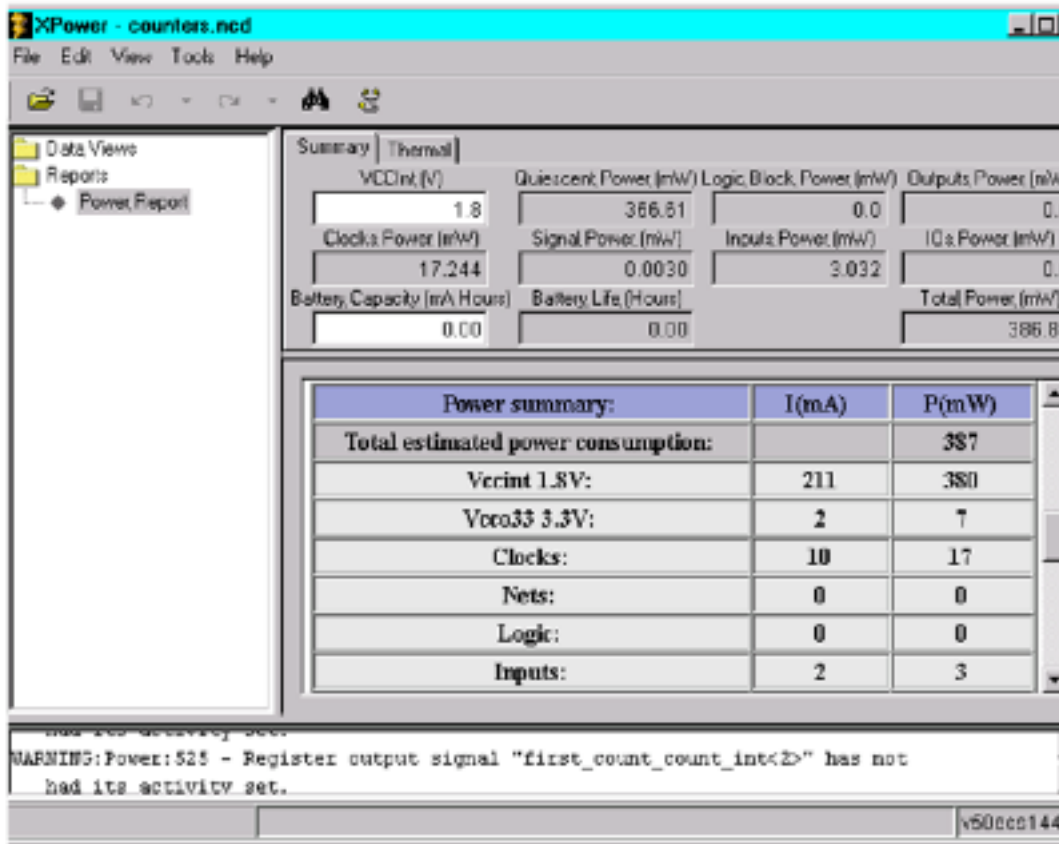
Name	Frequency (MHz)	Capacitive Load	DC Load (mA)	Output Enable	Power (mW)
ena_ibuf	0.06				0.01
enb_ibuf	0.06				0.01
first_count_count	0.0				0.0
first_count_count	0.0				0.0
first_count_count	0.0				0.0
first_count_count	0.0				0.0
first_count_count	0.0				0.0
rst_ibuf	0.06				0.01
second_count	0.0				0.0
second_count	0.0				0.0

A red arrow points to the 'Capacitive Load' column in the detailed table, with a red text overlay that reads: "Changing activity manually to analyze the impact".

At the bottom of the window, a warning message is visible: "WARNING: Power:525 - Register output signal 'first_count_count_intc15' has not been assigned yet." The status bar at the bottom right shows 'v508cs14'.

2. Click on the "+" sign beside the **Signals** folder to expand it, and then single-click the folder itself to list all of the signal names in the main window.

Xpower Report



- The first displays the the design name, the device series, the package name, the VCCInt, the default extension load, and the data version.
- The second part displays current and power summaries for the whole design, including Total Power consumption but also broken down into power consumed by Nets, Logic, Output, and Quiescent Power.
- The third part is a thermal summary which consists of Estimated junction temperature, Ambient temperature, and Theta J-A.
- Finally, the fourth part gives the date and time the analysis was completed.

It shows the dynamic power according to the simulation activity and duration time => Energy!

Exercicio

- Dado o VHDL de um contador sincrono de 8 bits (reset, clk, habilita cotagem, saida), estimar sua potencia no Xpower apos a sintese do FPGA VirtexII.
- Usar o ModelSim para a simulacao do VHDL mapeado + SDF file
- Gerar o VDC para o Xpower
- Verificar potencia para 2 VCD files com dois diferentes tempos de simulacao.
- Verificar potencia para 2 VCD files com duas frequencias de operacao.
- Comparar resultados.