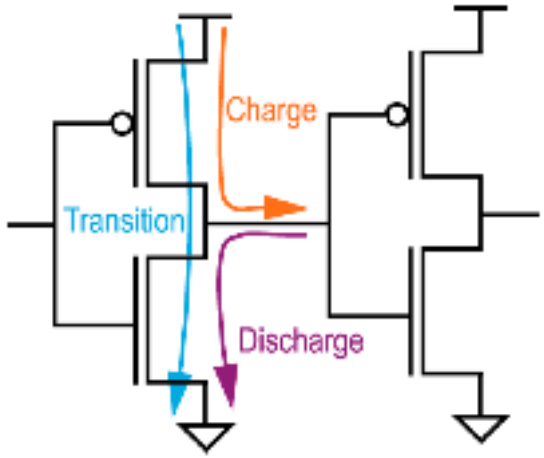
Power Estimation

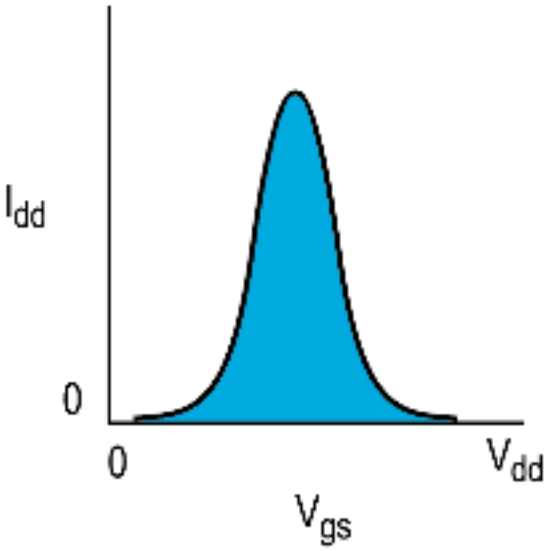
FPGA

ASIC

Power in CMOS

- Total Current is composed of two types of current
  - Static
  - Dynamic
- Static Current
  - Leakage current in the turned off transistor channel
  - Ideally zero (varies with technology)
  - Fixed component of Total Current
- Dynamic Current
  - Switching of the CMOS gate when in the linear region causing transition (crowbar) current
- Transition time is very fast
- Relatively small component
  - Charge/Discharge of capacitive poly gate in subsequent logic element
  - XPower combines transition current with capacitive current in the power model





Calculating Power

- Calculating Dynamic Current is an overwhelmingly tedious task
- XPower is necessary for this calculation
- Dynamic Current equation

$$I_{Dynamic} = C \cdot V \cdot f$$

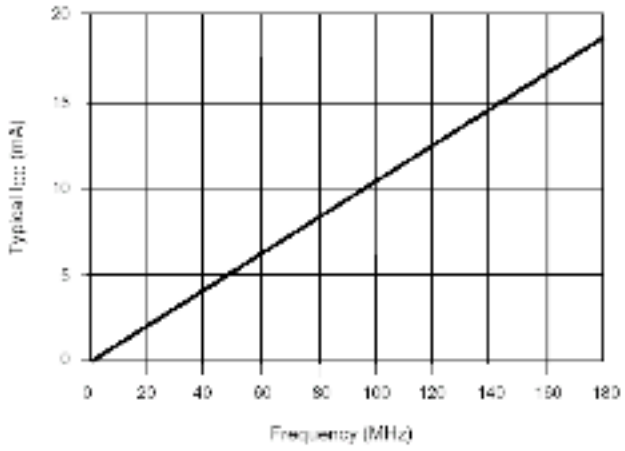
- Total Current equation

$$I_{Total} = I_{Dynamic} + I_{Static}$$

$$I_{Total} = C \cdot V \cdot f + I_{Static}$$

- Total Power equation

$$P_{Total} = I_{Total} \cdot V$$



Data Entry Method

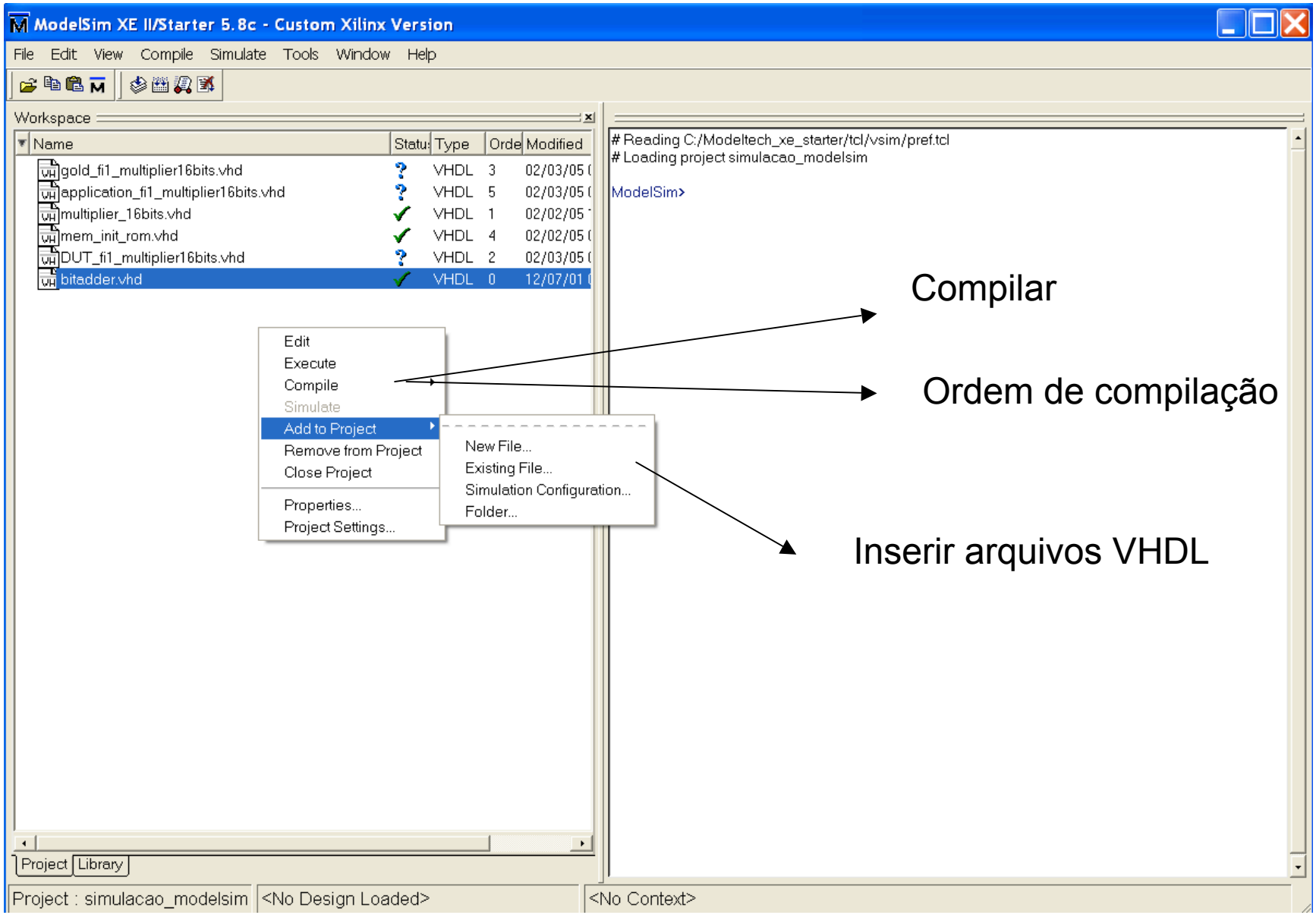
- Data entry by hand
  - Most accurate, but most tedious method
  - Requires very detailed knowledge of FPGA architecture
  - Must specify activity rates for all nets
  - Depending on the design, it may be nearly impossible to determine activity rates for all nets
- Estimate Activity Rates tool
  - Algorithm estimates absolute frequencies of nets not yet set by the user
  - Does not estimate toggle rates
  - Alleviates the tedium, but is less accurate than data entry by hand
  - Must enter all absolute frequencies for primary I/Os by hand
  - Must enter all toggle rates by hand including buried registers

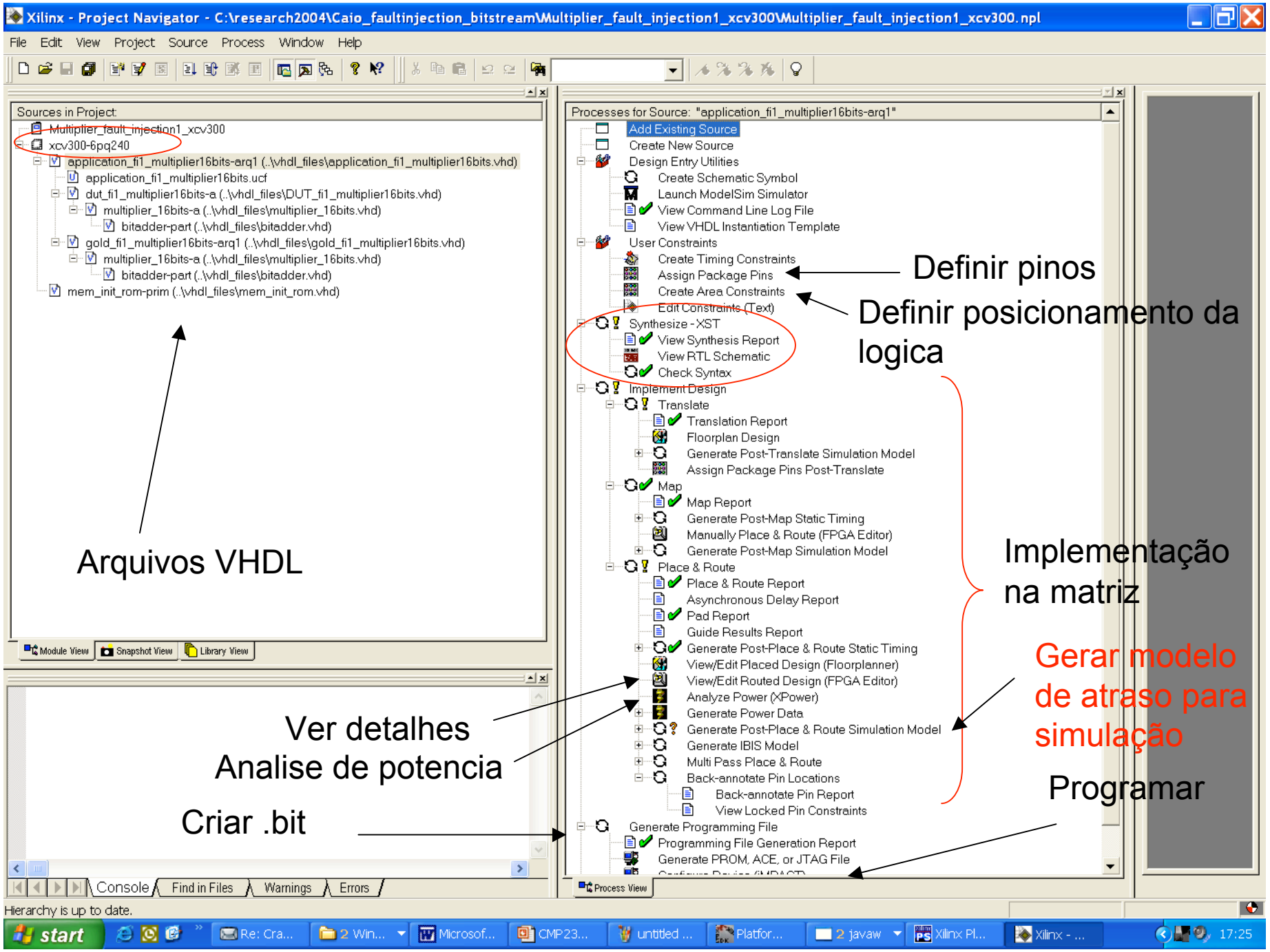
Data Entry Method

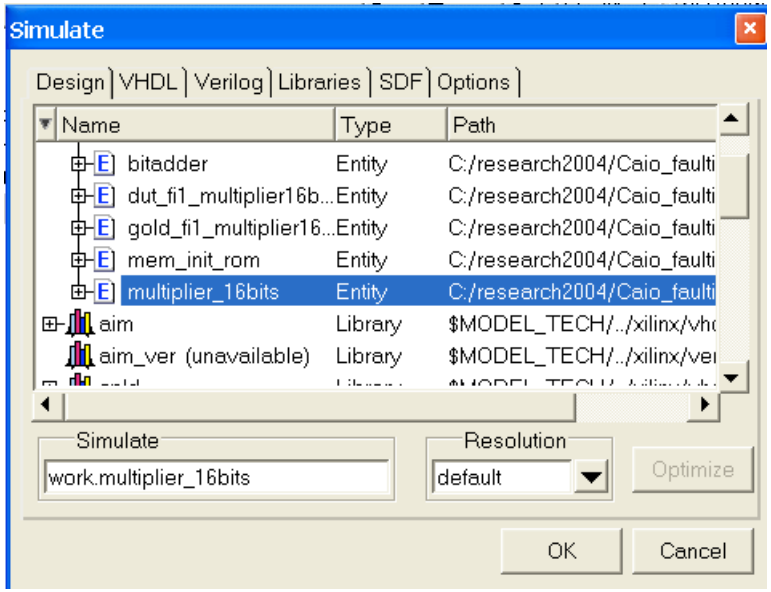
- Simulation with ModelSim XE
  - Easiest method
  - Value Change Dump (VCD) file contains frequency data
  - Simulate for sufficient length of time
  - Currently, only top level nets are contained in VCD file
  - Hand edit remaining primary I/Os and registers including buried registers
  - Use Estimate Activity Rates tool

VCD: Design file that provides detailed design activity rates for all nets. This file is generated during timing simulation using ModelSim simulator.

ModelSim (Simulação)

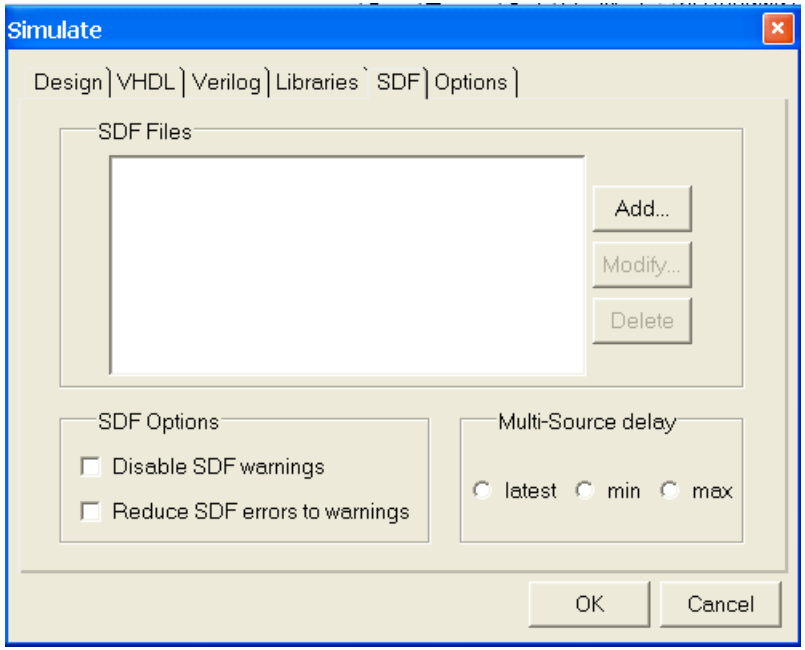



Xilinx - Project Navigator - C:\research2004\Caio_faultinjection_bitstream\Multiplier_fault_injection1_xcv300\Multiplier_fault_injection1_xcv300.npl
File Edit View Project Source Process Window Help
Sources in Project:
Multiplier_fault_injection1_xcv300
xcv300-6pq240
application_fi1_multiplier16bits-arq1 (..\vhdl_files\application_fi1_multiplier16bits.vhd)
application_fi1_multiplier16bits.ucf
dut_fi1_multiplier16bits-a (..\vhdl_files\DUT_fi1_multiplier16bits.vhd)
multiplier_16bits-a (..\vhdl_files\multiplier_16bits.vhd)
bitadder-part (..\vhdl_files\bitadder.vhd)
gold_fi1_multiplier16bits-arq1 (..\vhdl_files\gold_fi1_multiplier16bits.vhd)
multiplier_16bits-a (..\vhdl_files\multiplier_16bits.vhd)
bitadder-part (..\vhdl_files\bitadder.vhd)
mem_init_rom-prim (..\vhdl_files\mem_init_rom.vhd)
Module View
Snapshot View
Library View
Arquivos VHDL
Processes for Source: "application_fi1_multiplier16bits-arq1"
Add Existing Source
Create New Source
Design Entry Utilities
Create Schematic Symbol
Launch ModelSim Simulator
View Command Line Log File
View VHDL Instantiation Template
User Constraints
Create Timing Constraints
Assign Package Pins
Create Area Constraints
Edit Constraints (Text)
Synthesize - XST
View Synthesis Report
View RTL Schematic
Check Syntax
Implement Design
Translate
Translation Report
Floorplan Design
Generate Post-Translate Simulation Model
Assign Package Pins Post-Translate
Map
Map Report
Generate Post-Map Static Timing
Manually Place & Route (FPGA Editor)
Generate Post-Map Simulation Model
Place & Route
Place & Route Report
Asynchronous Delay Report
Pad Report
Guide Results Report
Generate Post-Place & Route Static Timing
View/Edit Placed Design (Floorplanner)
View/Edit Routed Design (FPGA Editor)
Analyze Power (XPower)
Generate Power Data
Generate Post-Place & Route Simulation Model
Generate IBIS Model
Multi Pass Place & Route
Back-annotate Pin Locations
Back-annotate Pin Report
View Locked Pin Constraints
Generate Programming File
Programming File Generation Report
Generate PROM, ACE, or JTAG File
Process View
Definir pinos
Definir posicionamento da logica
Implementação na matriz
Gerar modelo de atraso para simulação
Programar
Ver detalhes
Analise de potencia
Criar .bit
Console
Find in Files
Warnings
Errors
Hierarchy is up to date.
start
Re: Cra...
2 Win...
Microsof...
CMP23...
untitled ...
Platfor...
2 javaw
Xilinx Pl...
Xilinx - ...
17:25

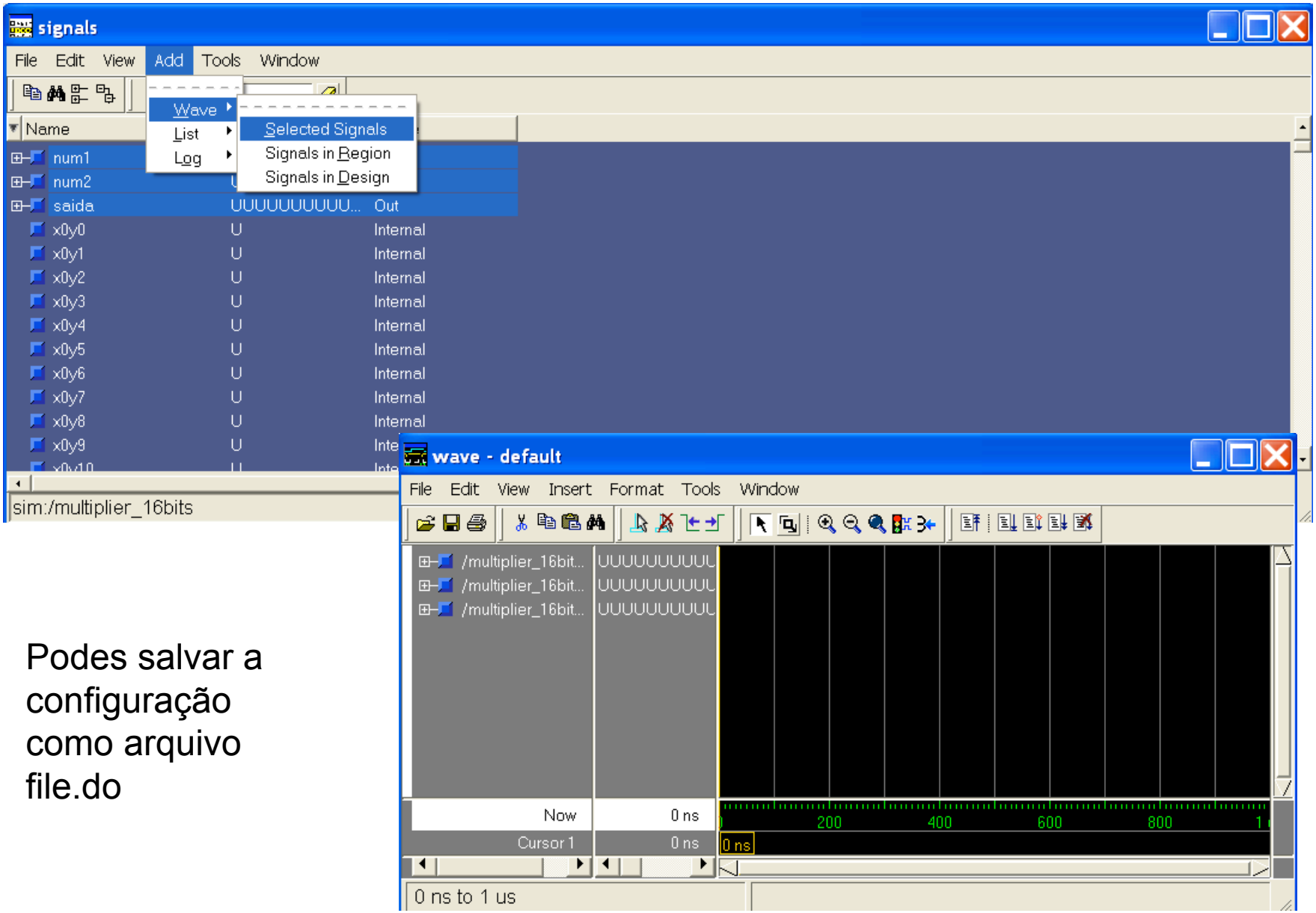


•Escolher qual arquivo compilado queres simular
•Caso haja hierarquia, escolha o de maior hierarquia para simular o conjunto.

Para simular com atraso, deves inserir o SDF file gerado pela ferramenta de mapeamento, posicionamento e roteamento do ISE.

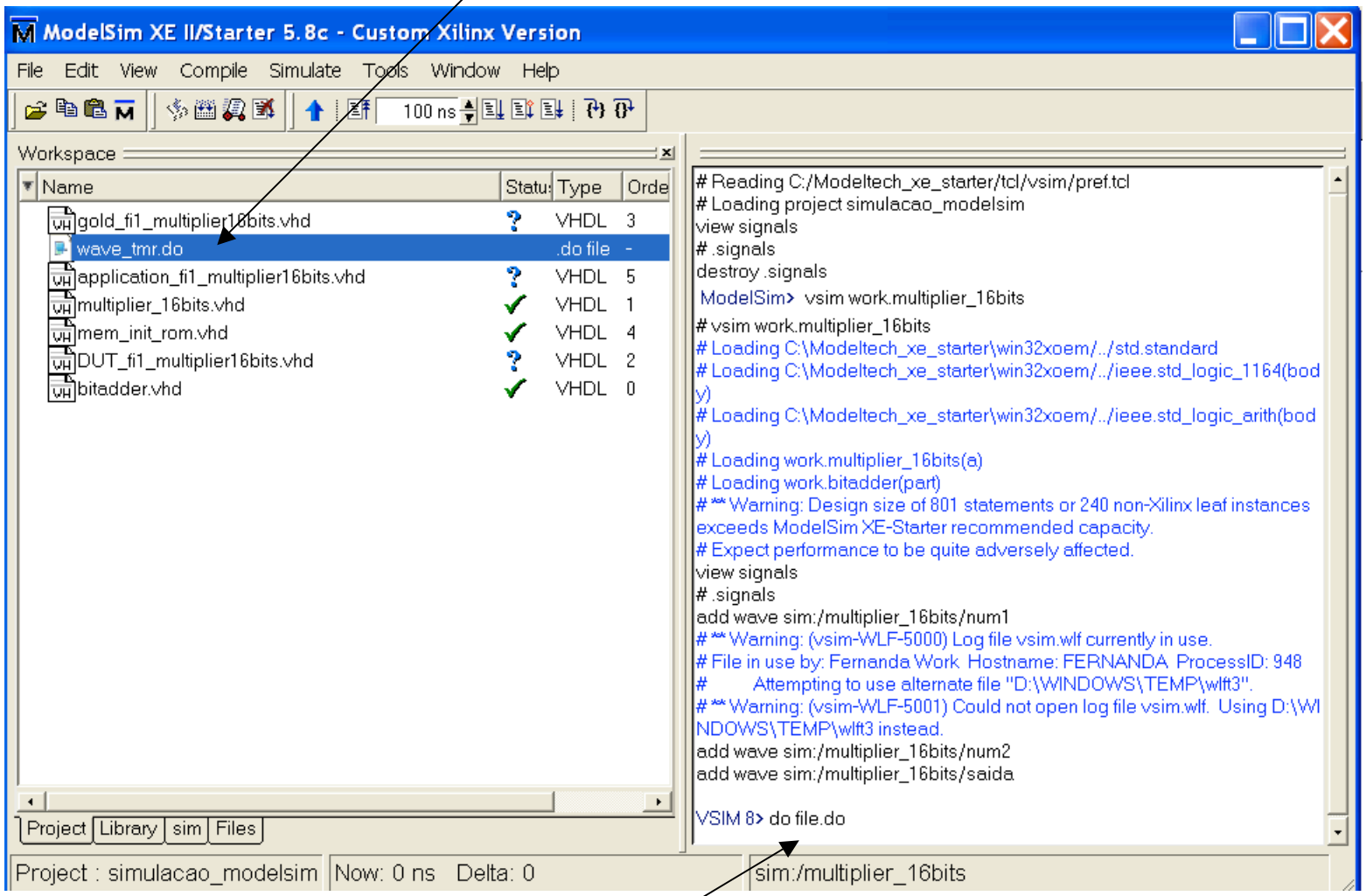


View > signals

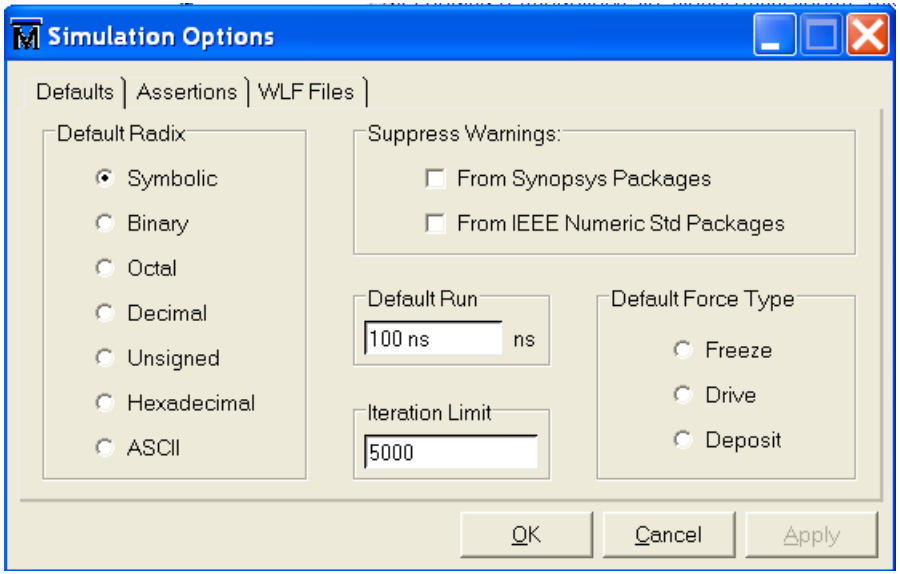


Podes salvar a configuração como arquivo file.do

Outro arquivo .do para simulação



Comando: do file.do



Configurar corretamente as opções de simulação:

-Tipo de dados que iras inserir na entrada conforme file.do

-Tempo de simulação é muito importante.

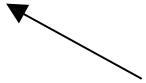
vcd file multiplicacao_16bits_power_noreg.vcd
vcd on
vcd add multiplier_16bits/*

Usado para estimar potência depois na ferramenta XPOWER

force num1 1024 0ns, 1025 50ns,1026 100ns,2333 150ns,4567 200ns,2987 250ns, 9056 300ns, 167 350ns, 13 400ns,1999 450ns,2349 500ns, 17758 550ns, 23450 600ns, 10875 650ns, 1345 700ns,1024 750ns,1000 800ns,1028 850ns,2333 900ns,4567 950ns,2987 1000ns, 1024 1050ns, 1025 1100ns, 1026 1150ns, 2333 1200ns, 4567 1250ns, 2987 1300ns, 9056 1350ns, 167 1400ns, 13 1450ns,1999 1500ns,2349 1550ns, 17758 1600ns, 23450 1650ns, 10875 1700ns, 1345 1750ns, 1024 1800ns, 1000 1850ns, 1028 1900ns, 2333 1950ns, 4567 2000ns

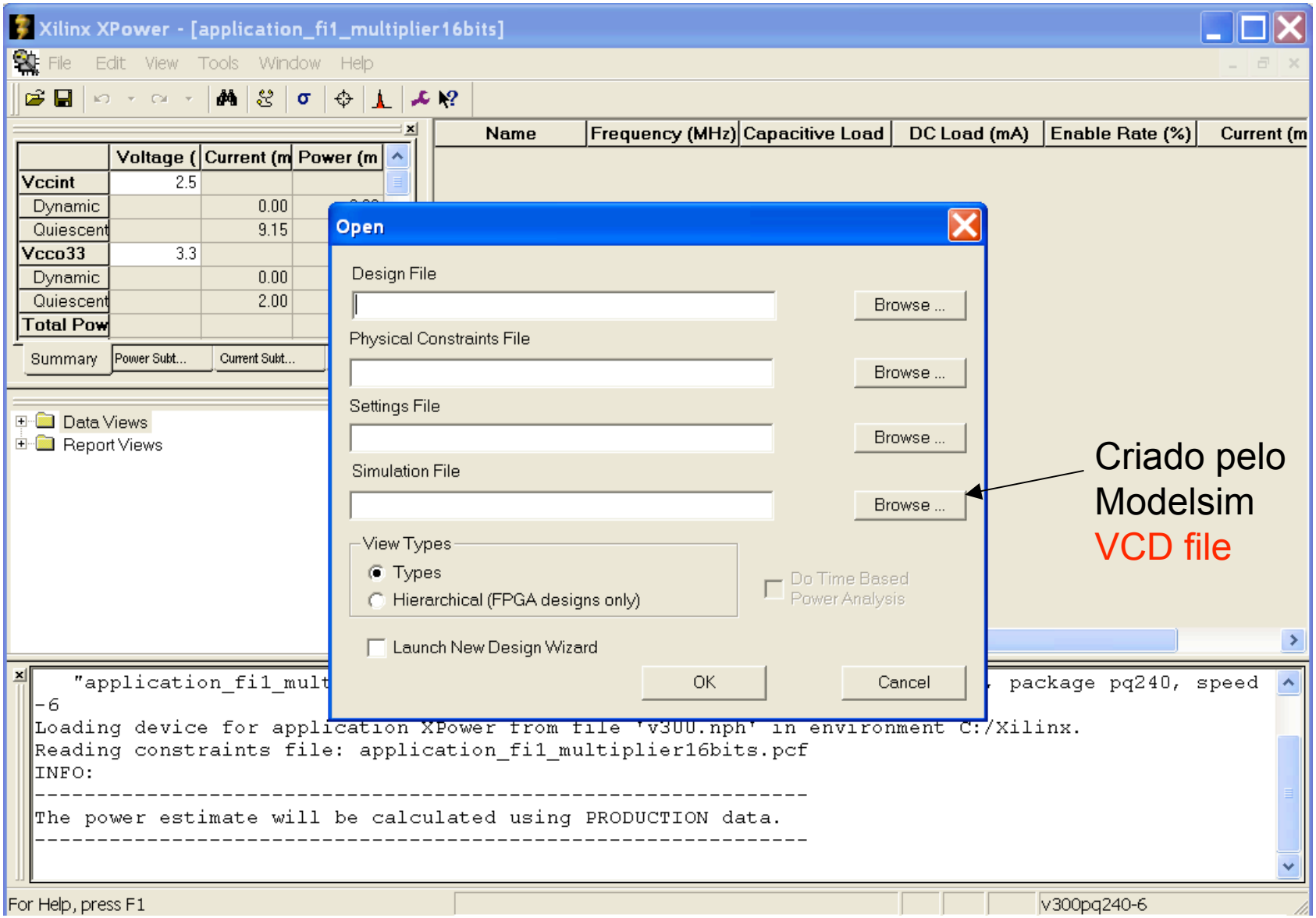
force num2 1024 0ns, 1025 50ns,1026 100ns,2333 150ns,4567 200ns,2987 250ns, 9056 300ns, 167 350ns, 13 400ns,1999 450ns,2349 500ns, 17758 550ns, 23450 600ns, 10875 650ns, 1345 700ns,1024 750ns,1000 800ns,1028 850ns,2333 900ns,4567 950ns,2987 1000ns, 1024 1050ns, 1025 1100ns, 1026 1150ns, 2333 1200ns, 4567 1250ns, 2987 1300ns, 9056 1350ns, 167 1400ns, 13 1450ns,1999 1500ns,2349 1550ns, 17758 1600ns, 23450 1650ns, 10875 1700ns, 1345 1750ns, 1024 1800ns, 1000 1850ns, 1028 1900ns, 2333 1950ns, 4567 2000ns

run 2000ns



Tempo de simulação

Xpower

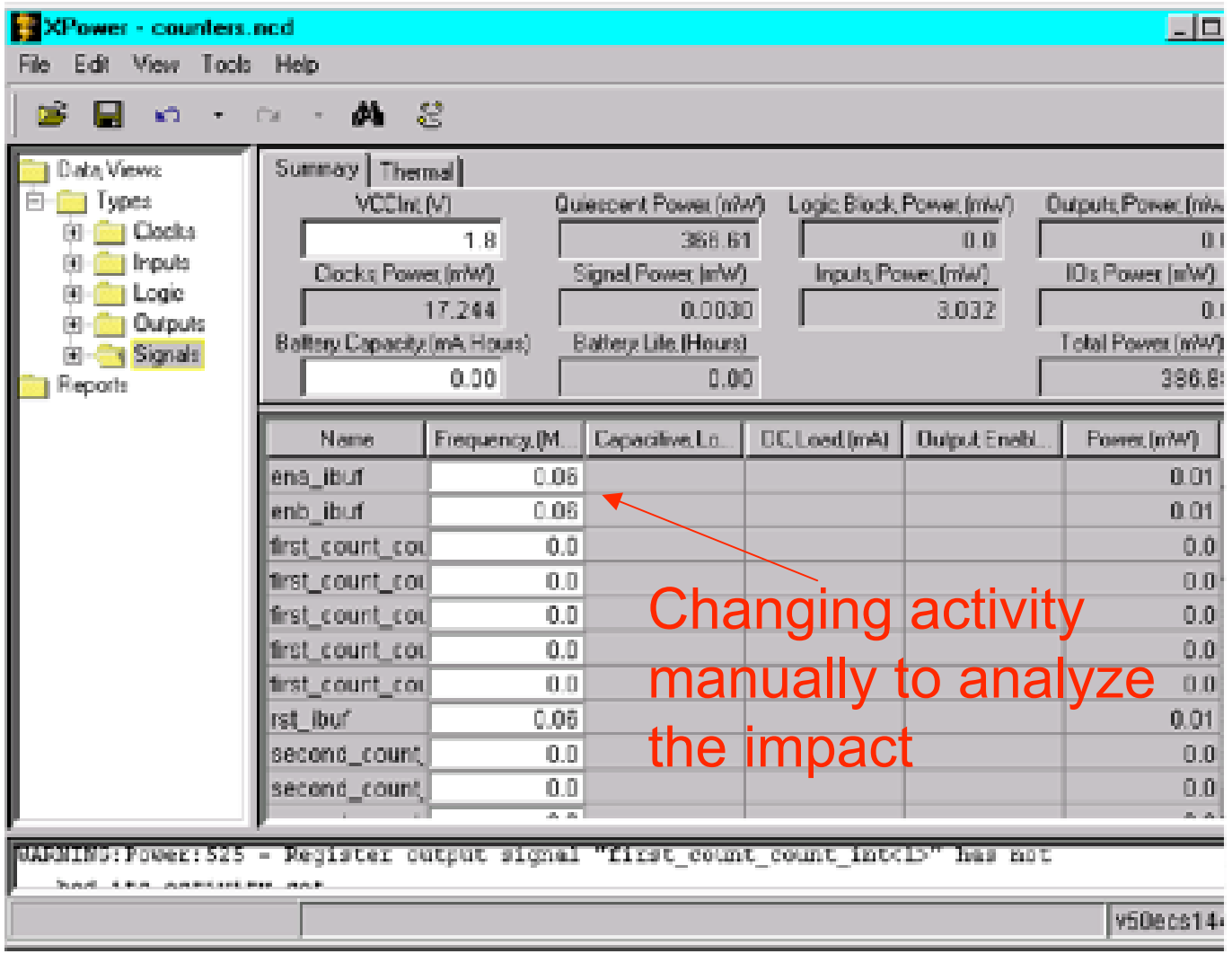

Xilinx XPower - [application_fi1_multiplier16bits]
File Edit View Tools Window Help
Name
Frequency (MHz)
Capacitive Load
DC Load (mA)
Enable Rate (%)
Current (m
Voltage (
Current (m
Power (m
Vccint
2.5
Dynamic
0.00
Quiescent
9.15
Vcco33
3.3
Dynamic
0.00
Quiescent
2.00
Total Pow
Summary
Power Subt...
Current Subt...
Data Views
Report Views
Open
Design File
Browse ...
Physical Constraints File
Browse ...
Settings File
Browse ...
Simulation File
Browse ...
View Types
Types
Hierarchical (FPGA designs only)
Do Time Based Power Analysis
Launch New Design Wizard
OK
Cancel
Criado pelo Modelsim
VCD file
"application_fi1_mult
, package pq240, speed
-6
Loading device for application XPower from file 'v300.nph' in environment C:/Xilinx.
Reading constraints file: application_fi1_multiplier16bits.pcf
INFO:
The power estimate will be calculated using PRODUCTION data.
For Help, press F1
v300pq240-6

Xpower from Xilinx

- XPower allows you to change activity rate information on individual clocks, signals, logic and outputs. This allows you make specific changes to frequencies in your design to see the effect they have on power consumption. Xilinx recommends that this be done in a specific order to achieve the most accurate power estimate. The order in which you need to set or verify activity rates on different elements in your design are:

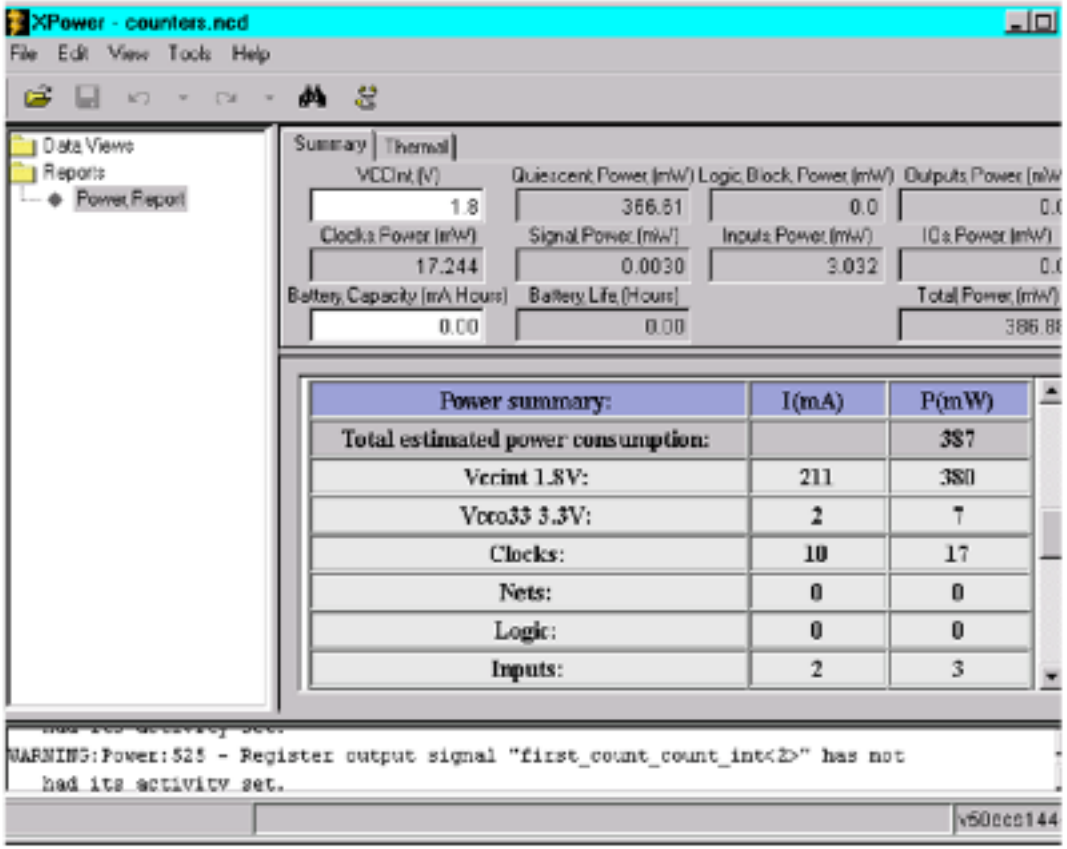
- Set or verify voltage and ambient temperature
- Set or verify clock frequencies
- Set or verify input frequencies
- Set or verify output loading
- Set global default activity to estimated value
- Set any specific or signal groups to estimated values

1. In the Explorer window double-click on the **Data Views** folder and then double-click on the **Types** folder. You will see four folders beneath the **Types** folder: Signals, Clocks, Logic, and Outputs.



2. Click on the "+" sign beside the **Signals** folder to expand it, and then single-click the folder itself to list all of the signal names in the main window.

Xpower Report



-The first displays the the design name, the device series, the package name, the VCCInt, the default extension load, and the data version.
- The second part displays current and power summaries for the whole design, including Total Power consumption but also broken down into power consumed by Nets, Logic, Output, and Quiescent Power.
-The third part is a thermal summary which consists of Estimated junction temperature, Ambient temperature, and Theta J-A.
- Finally, the fourth part gives the date and time the analysis was completed.

It shows the dynamic power according to the simulation activity and duration time => Energy!

Exercicio

- Dado o VHDL de um contador sincrono de 8 bits (reset, clk, habilita cotagem, saida), estimar sua potencia no Xpower apos a sintese do FPGA VirtexII.
- Usar o ModelSim para a simulacao do VHDL mapeado + SDF file
- Gerar o VDC para o Xpower
- Verificar potencia para 2 VCD files com dois diferentes tempos de simulacao.
- Verificar potencia para 2 VCD files com duas frequencias de operacao.
- Comparar resultados.