On the Design of CMOS Vision Systems on Chip

Angel Rodríguez-Vázquez

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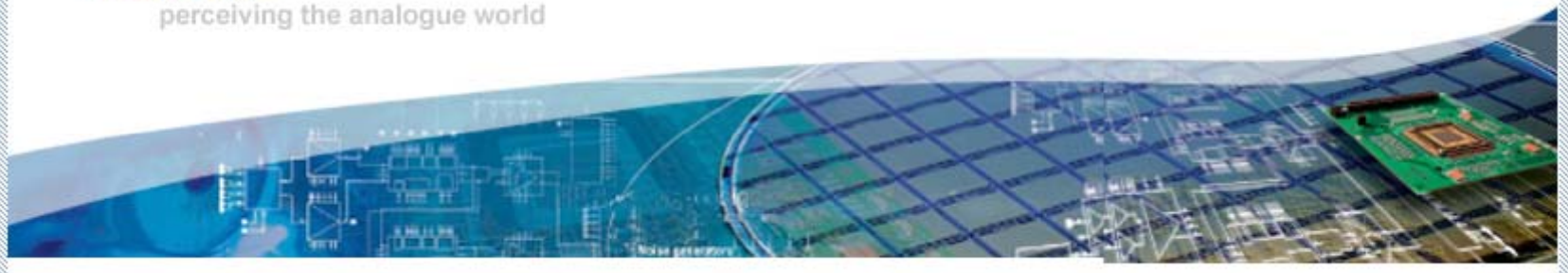
Outline of the Talk

- ***Some Basic Concepts:***
  - ***Concept of Vision Systems and VSoCs***
  - ***Conventional Vision System Architecture***
  - ***Rationale for Using CMOS***
- ***Architectures for Vision Systems***
  - ***Progressive Distributed Processing***
  - ***Bio-Inspired Vision System Architectures***
  - ***Shifting the Analog-to-Digital Border***
- ***Topographical Sensor-Processors***
  - ***Concept of Concurrent Sensory-Processing***
  - ***Multi-Functional Pixel***
  - ***Rationale for Analog Pre-Processing***
- ***The Eye-RIS Vision Systems***
  - ***Architecture***
  - ***The System in Operation***
  - ***Some Prospects for Future Developments***

ANAFOCUS
perceiving the analogue world



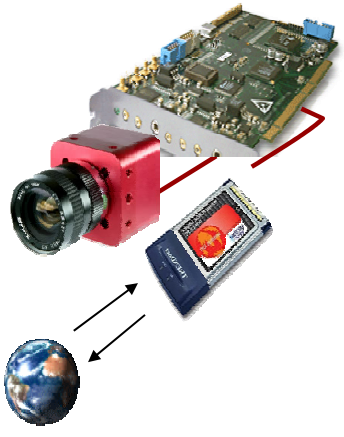
Some Basic Concepts

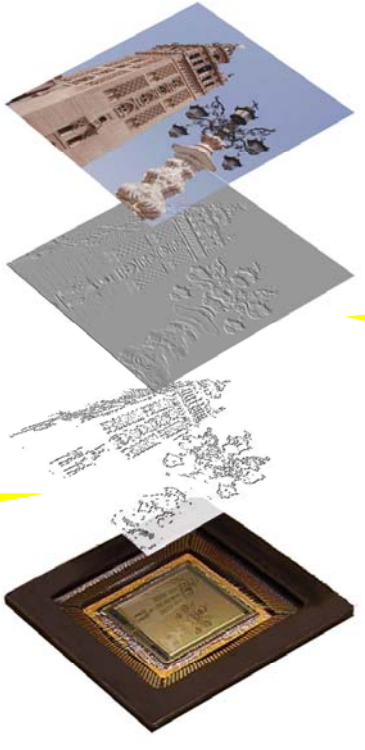
Concept of Vision Systems

Conventional MV Architectures

Rationale for CMOS Implementation

Concept and Ingredients of Vision

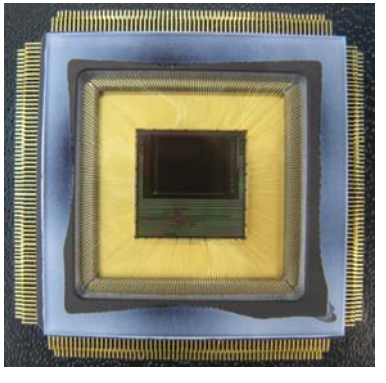




Interpretation and Decision

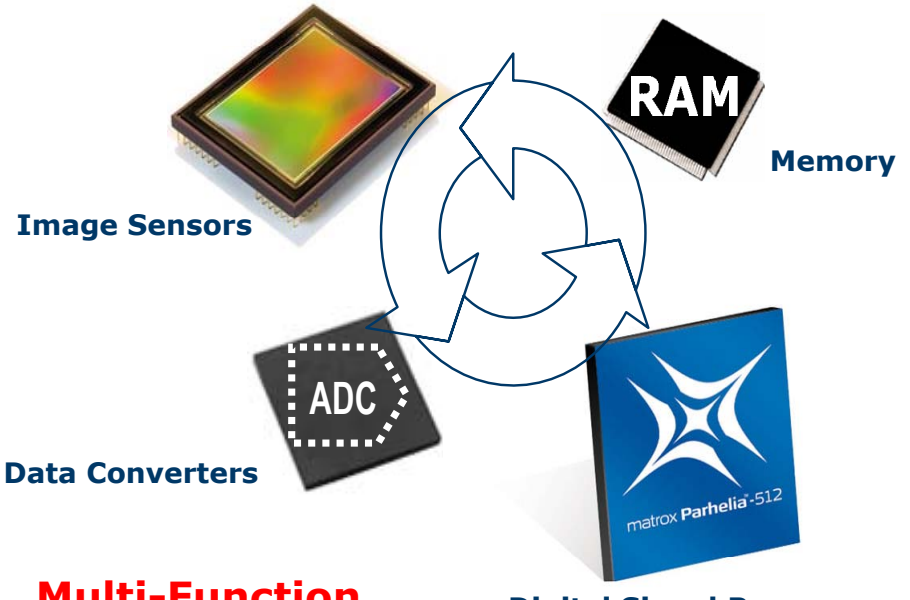
Image Processing

Image Acquisition

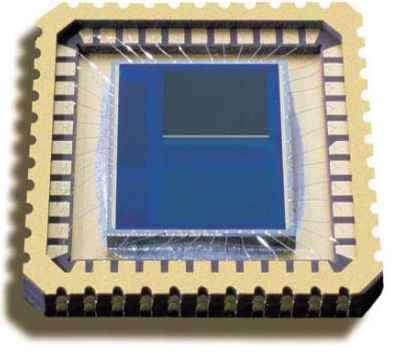


The Concept of CMOS Vision System on-Chip

All functions for smart imaging and vision systems on chip



Multi-Function System



Single-Chip Solution

Illustrating the Challenge of Autonomy

Systems capable to make autonomous decisions for vision-based guidance

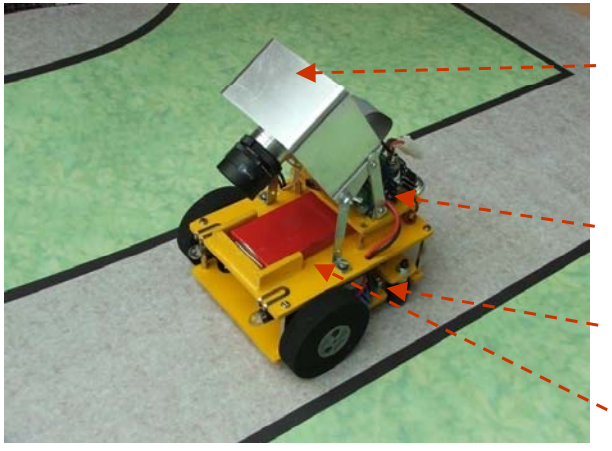
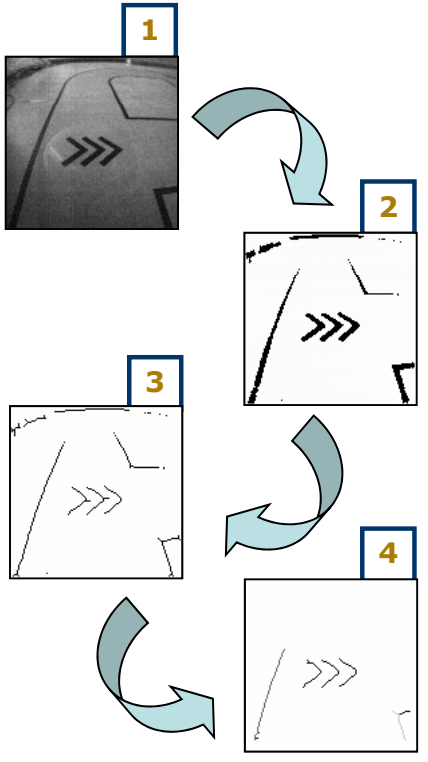
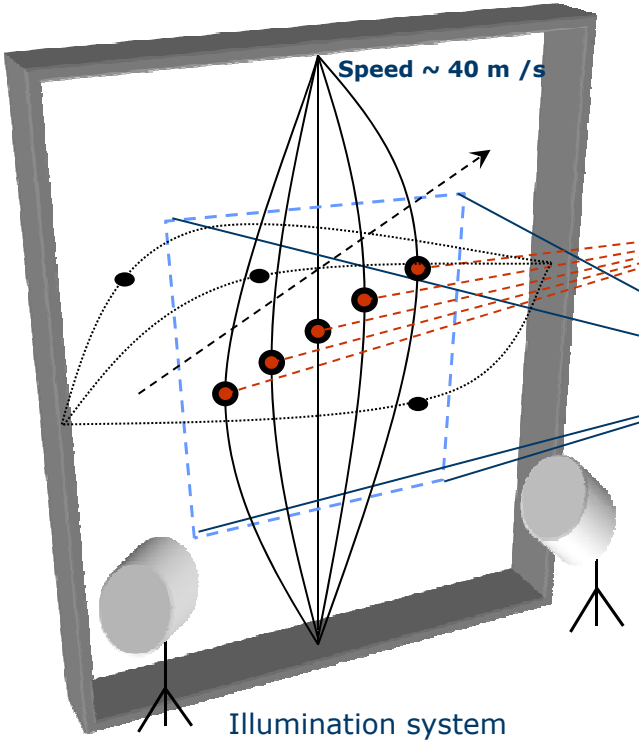


Image acquisition | Low-pass filtering | tresholding | skeletonization |morphological filtering | signal recognition | road-lanes recognition | actuation on the robot wheels.



Illustrating the Challenge of Speed

Systems to close the Perception-to-Action Loop at Thousands Images-per-Second



Illumination system

Up to 3,000 frames per second

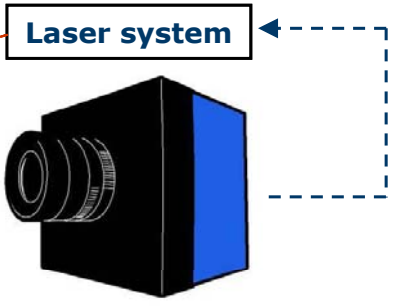


Image acquisition | Low-pass filtering | activity detection | motion estimation | object tracking | Loop control | position prediction | coordinates translation | actuation on the laser system.

Goals of Artificial Vision Systems

- ***Perceive lightness and colour under various illuminations***
- ***Detect intensity changes and perform 2-D segmentation***
- ***Infer 3-D structures from stereo or motion images***
- ***Organize surface and regions into objects of interest***
- ***Generate description of objects and recognize them among a potentially large class of objects***
- ***Make non-visual inferences about the scene based on visual processing (abstraction)***

Emulate the capabilities of human visual systems

[*H.R. Myler, Fundamentals of Machine Vision*]

The Vision Processing Chain

Task n°	Processing Task	Example	Amount of data
			$b \times N^2$
①	Image Acquiring	Light sensing	$b \times N^2$
②	Noise reduction	Lowpass, median filtering...	$b \times N^2$
③	Segmentation	Edge detection	N^2
④	Feature extraction	shape detection	N
⑤	Classification	identification	1

N=image width & heigh

b=number of bits of resolution

☹ ***Huge amount of data at Early Stages***

RGB 8-bit coded @ 512 x 512 implies 200Mbit/s data rate

☹ ***Most data are useless***

Illustrating the Computational Demands

Per-Pixel 3x3 Linear Convolution

9 Products

+

8 Sums

---

17 Operations

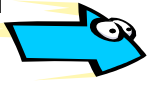
If the image is ***N***x***M***

17x***N***x***M* **Oper.**

If the algorithm contains N_s convs.

17x N_sx***N***x***M* **Oper.**

At ***F*** Frames per second



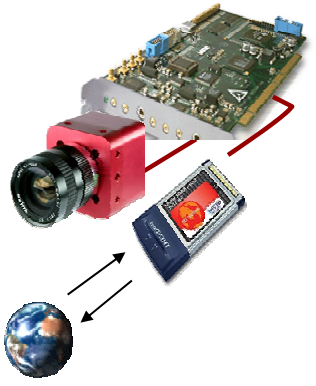
17x***F***x N_sx***N***x***M* **OPS**

10 convolutions on 8-bit gray-scale VGA images at 100 FPS requires 5 GOPS

Memory operations must be accounted for as well

[Original from Gustavo Liñán]

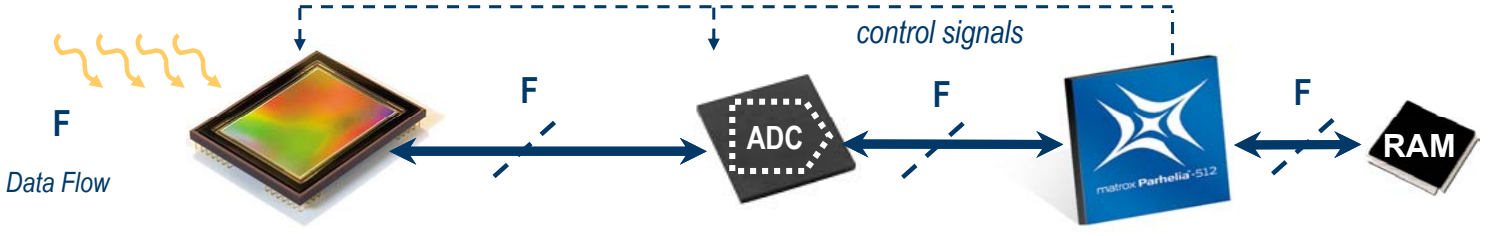
Conventional Vision System Architecture



- **Conventional systems are heterogeneous**

  Sensors, Memory, Processors, Communications

- **Involve multiple technologies**

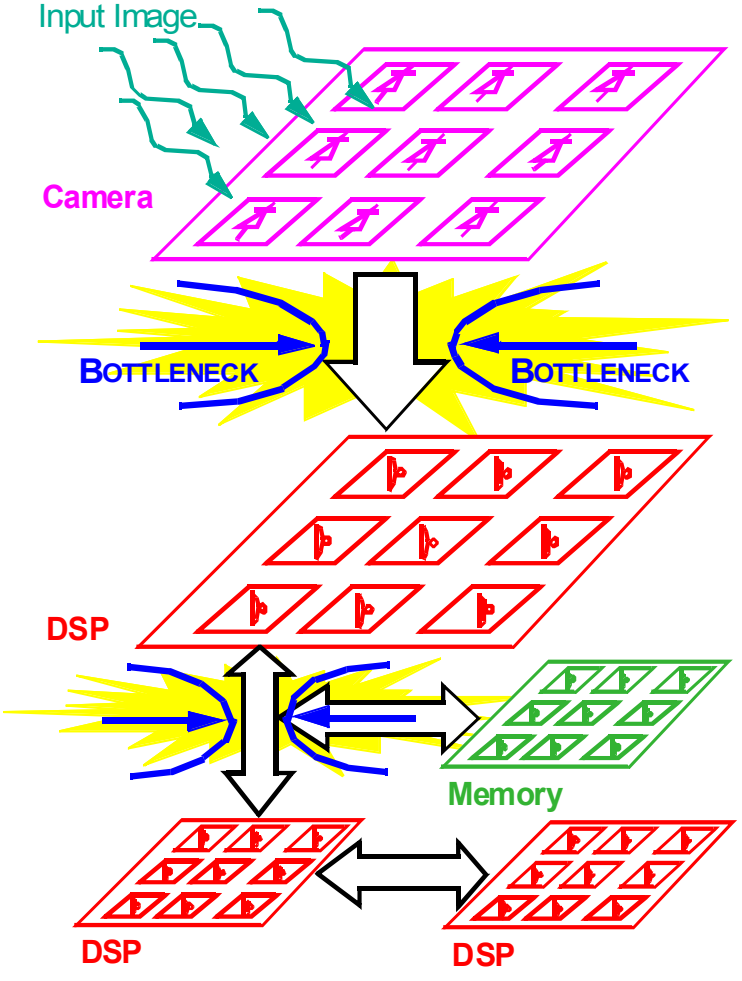


CMOS / CCD sensor — *Image Acquisition*

High-performance A/D Converters — *Image Coding*

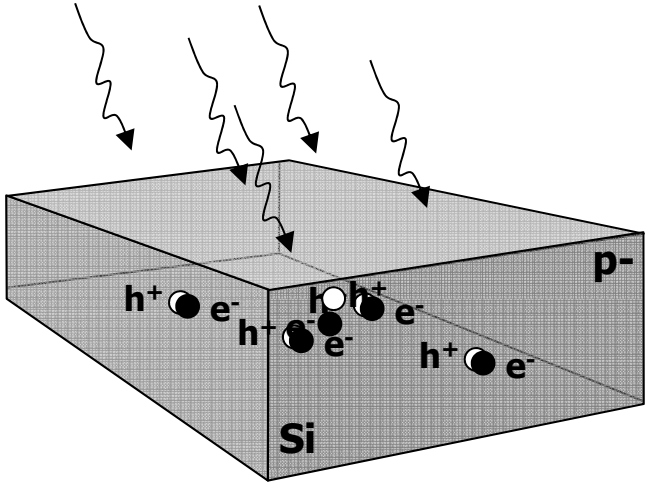
Advanced DSP & High Density Memory — *Image Processing and Storage*

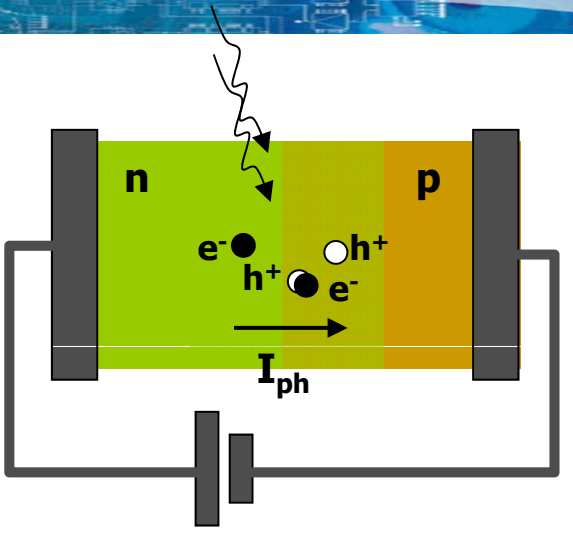
Troubles of Conventional MV Architectures



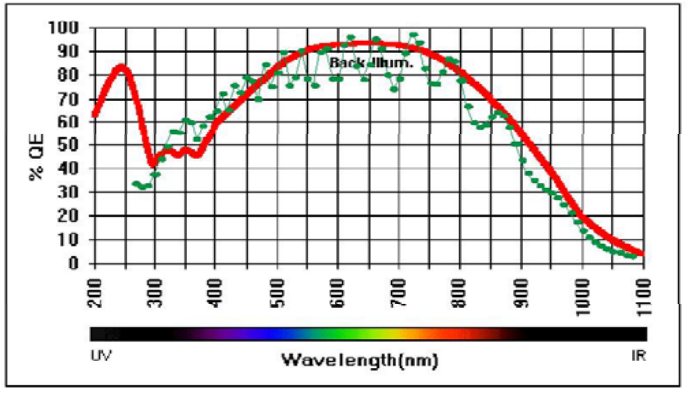
- *Physical separation:*
  - *Sensors*
  - *Processors*
- *Heterogeneous technologies*
  - *CCD or CMOS for sensing*
  - *CMOS: FPGA, Power-PC, DSP, etc for processing*
- ***Bottlenecks at different stages***
  - *Image coding*
  - *Image transmission*
  - *Image processing*

Photo-transduction Mechanisms



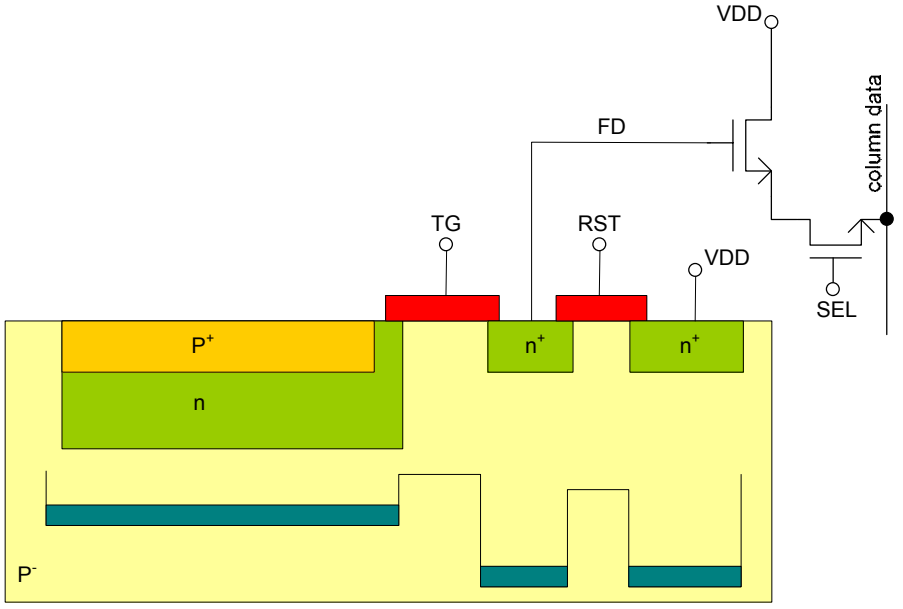


- *Incident photons create electron-hole pairs*
- *The absorption length depends upon the wavelength*
- *An electrical field separate the hole-electron pairs*



CCD: Hamamatsu S7030
CMOS: Perkin Elmer RL0512T

Pinned Photodiodes



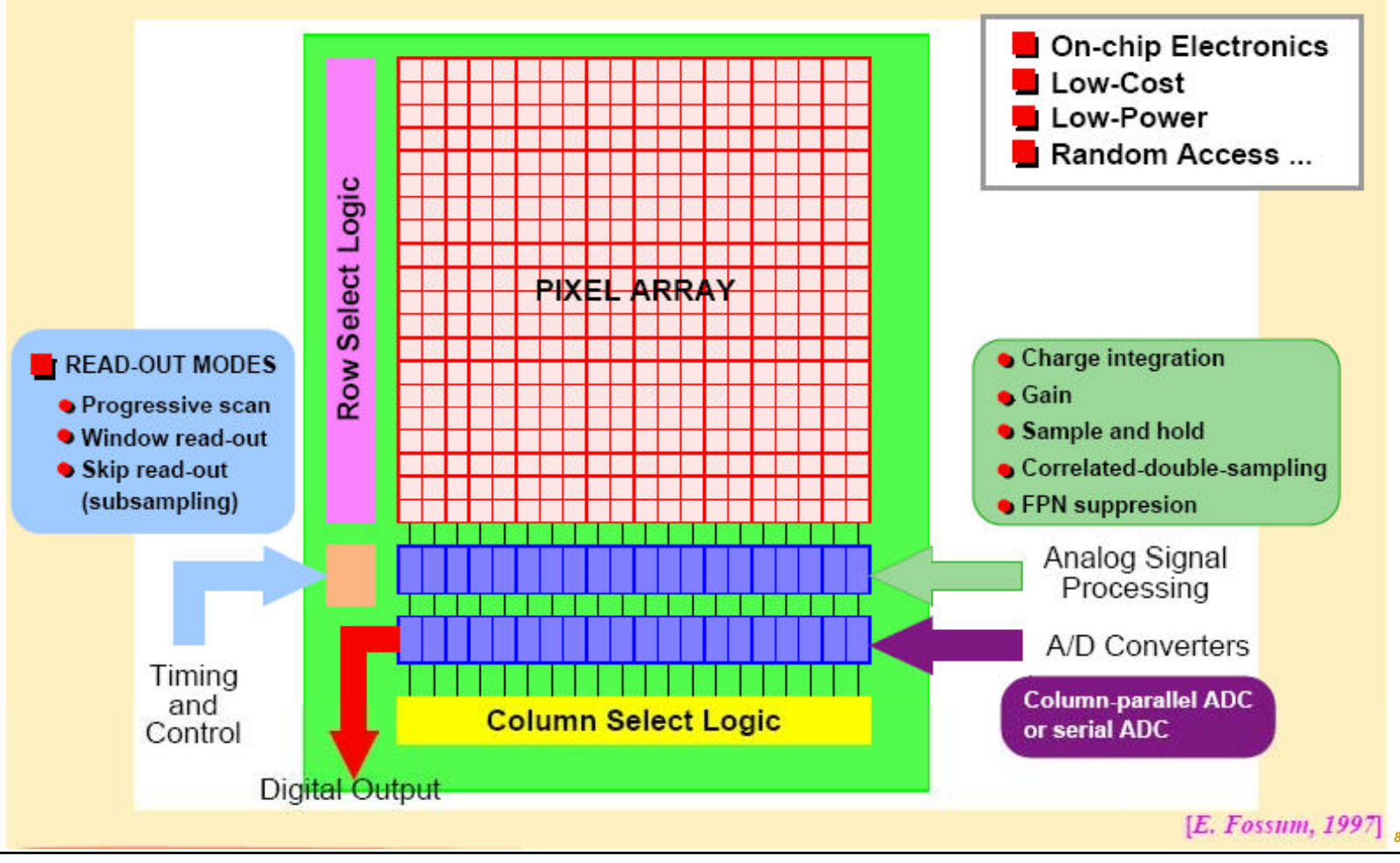
Features:

- $p^+ n p^-$ structure
- Low-dark current
- Operation similar to photogate
- Decrease reset noise (Correlated Double Sampling)
- Better response to blue

During integration phase, photo-generated majority carriers are stored in the depletion region. (Device is fully depleted)

The Concept of CMOS Camera on Chip

Fossum´s Camera on Chip



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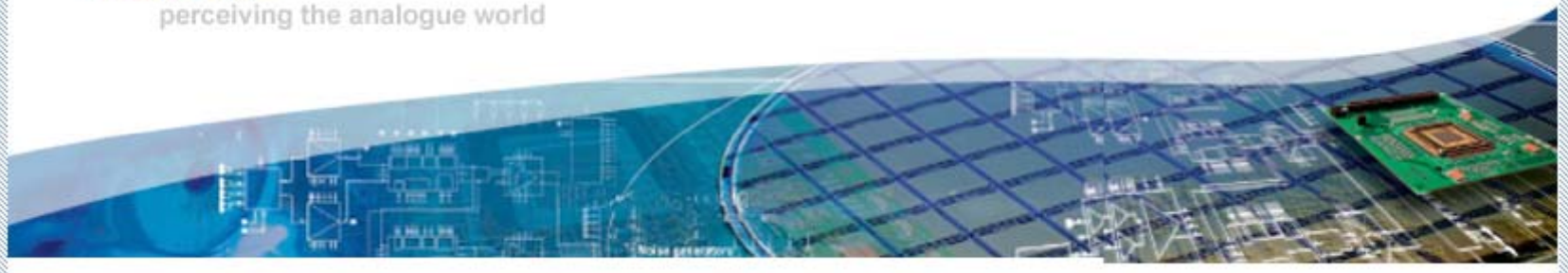
perceiving the analogue world



Architectures for Sensory-Processing

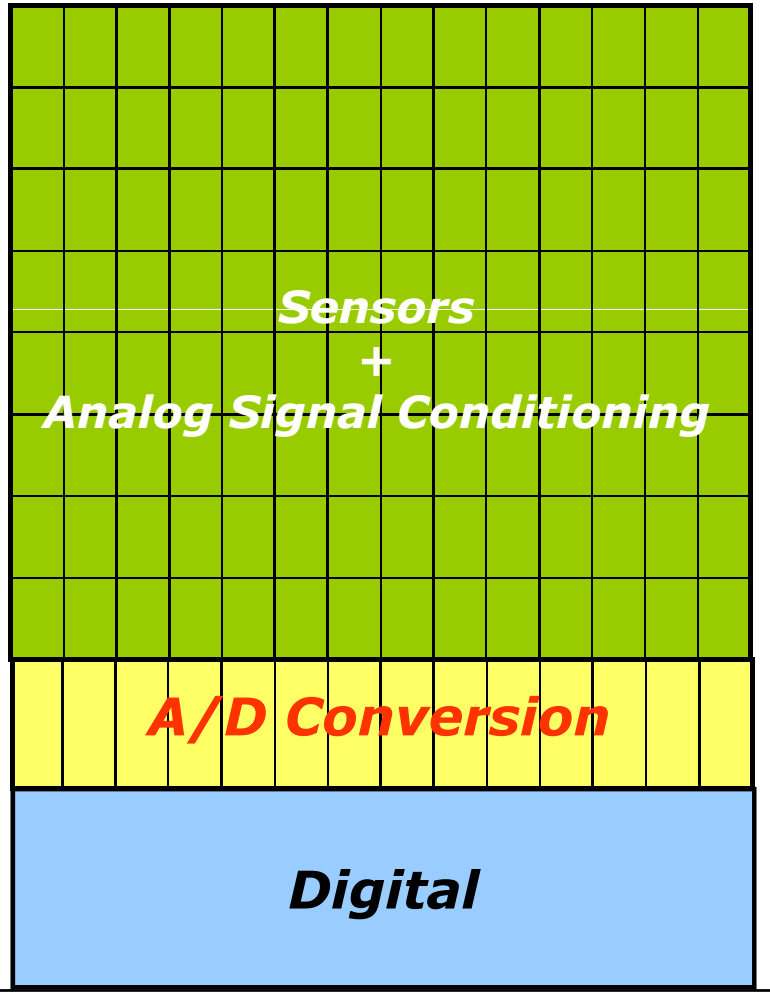
Progressive Distributed Processing

Bio-Inspired Vision Architectures

Shifting the Analog-to-Digital Border

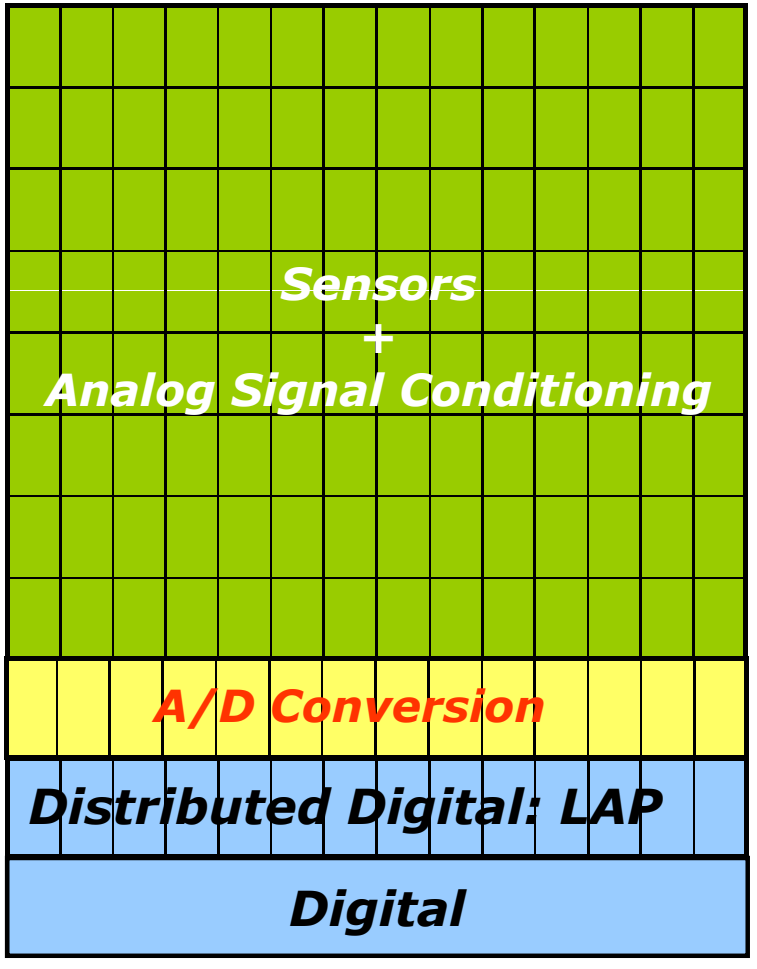
Conceptual Architectural Choices

Conventional Architecture



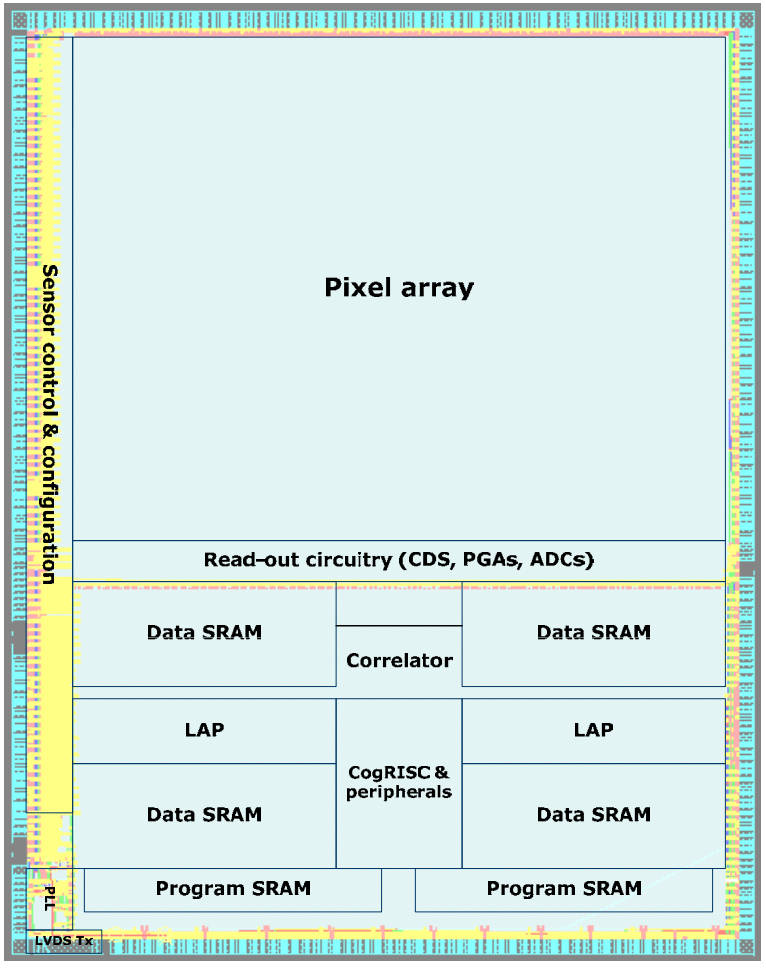
- ☺ Large **spatial resolution** limited only by pixel SNR
- ☺ Large **circuit operation predictability and robustness** analog only at the ADCs
- ☺ Small **spurious signal interactions**
- ☺ Large **flexibility and programmability**: mostly digital circuits and codes
- ☹ Small **computational power and efficiency**
- ☹ Large **memory requirements**
- ☹ Data transfer **bottlenecks**

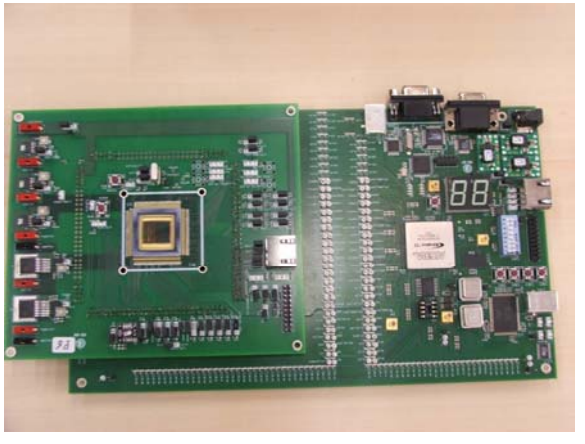
Linear Array of Digital Processors



- Smaller spatial resolution: trade-off with processing
- Large circuit operation predictability and robustness: analog only at the ADCs
- Small spurious signal interactions
- Large flexibility and programmability: mostly digital circuits and codes
- Larger computational power and efficiency
- Smaller memory requirements
- Data transfer bottlenecks

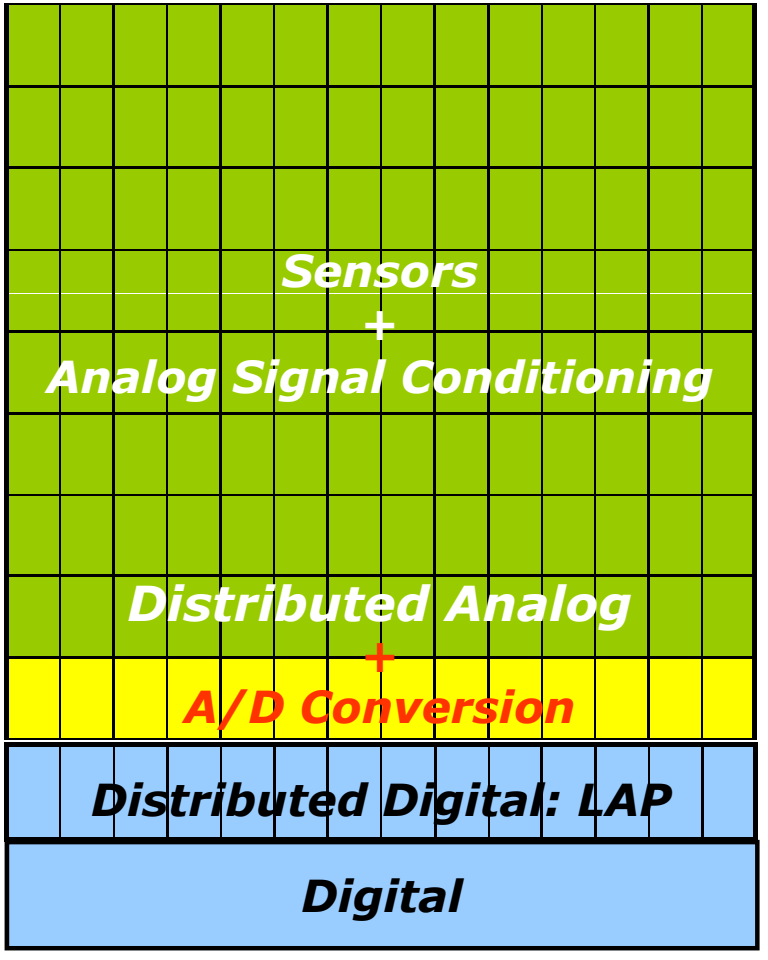
A True LAP VSoC for Machine Vision





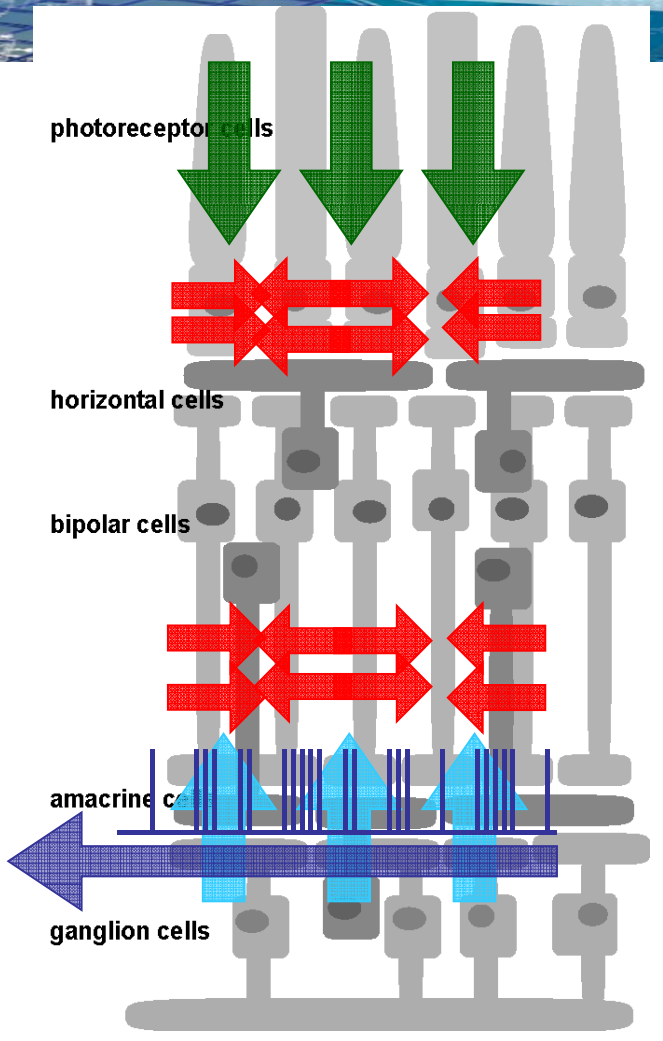
- Pinned photodiode pixel
- High-speed rolling and global electronic shutter with programmable exposure time.
- Programmable controls: gain, offset, frame rate and frame size (RoI)
- 100MHz clock frequency
- Per-column readout path permitting up to 500fps readout speeds
- Multiple I/Os and high-speed communications

Linear Array of Analog-Digital Processors



- 😟 Smaller **spatial resolution**: trade-off with processing
- 😟 Smaller circuit operation **predictability and robustness**: analog also for processing
- 😟 Larger **spurious signal interactions**
- 😐 Smaller **flexibility and programmability**: both analog and digital circuits
- 🙂 Larger **computational power and efficiency**
- 🙂 Smaller **memory requirements**
- 🙂 Smaller transfer **bottlenecks**

How Does The Retina Work ?[21]



- ***Sensors and processors are merged***
- ***Processing and sensing are simultaneous***
- ***Significant data compression is achieved***

How Does Retina Work ? 22

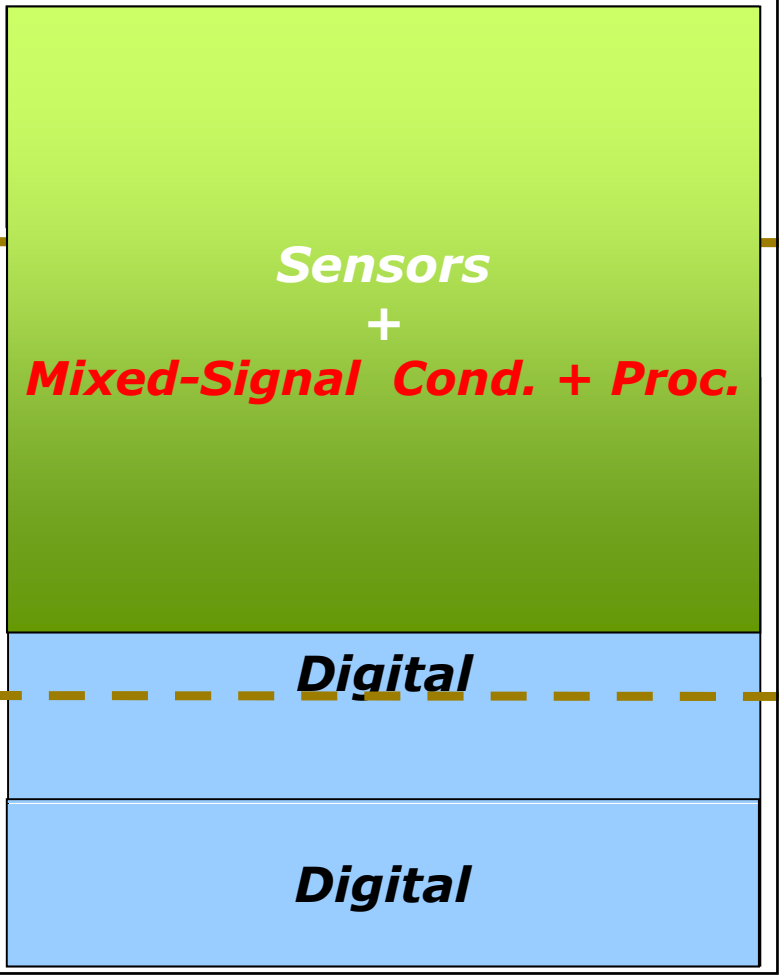
[*Roska & Werblin 2001*]

Shifting the Analogue-Digital Border

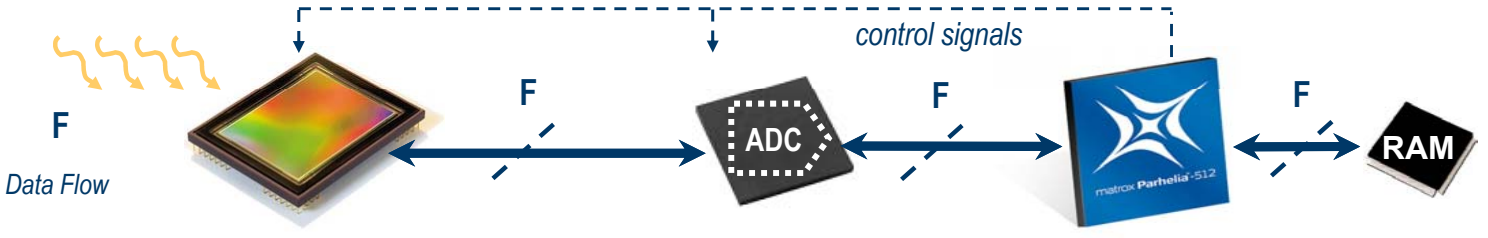
Task n°	Processing Task	Example	Amount of data
			$b \times N^2$
①	Image Acquiring	Light sensing	
			$b \times N^2$
②	Noise reduction	Lowpass, median filtering...	
			$b \times N^2$
③	Segmentation	Edge detection	
			N^2
④	Feature extraction	shape detection	
			N
⑤	Classification	identification	
			1

N=image width & heigh

b=number of bits of resolution



Using the Bio-Inspiration Concept



CMOS / CCD sensor

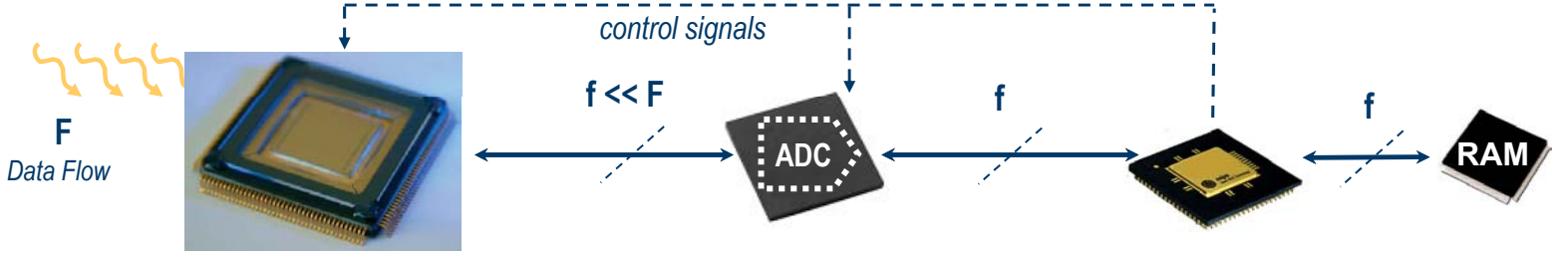
Image Acquisition

High-performance A/D Converters

Image Coding

Advanced DSP & High Density Memory

Image Processing and Storage



Focal-Plane Sensor-Processor

Image Acquisition & Pre-processing

Low-Profile A/D Converters

Pre-processed Image Conversion

Simple DSP & Low Memory

Image Post-Processing and Storage

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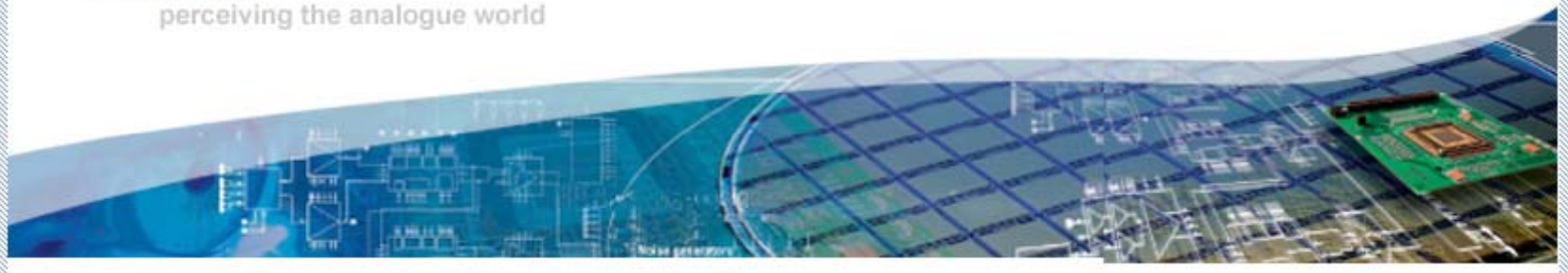
perceiving the analogue world



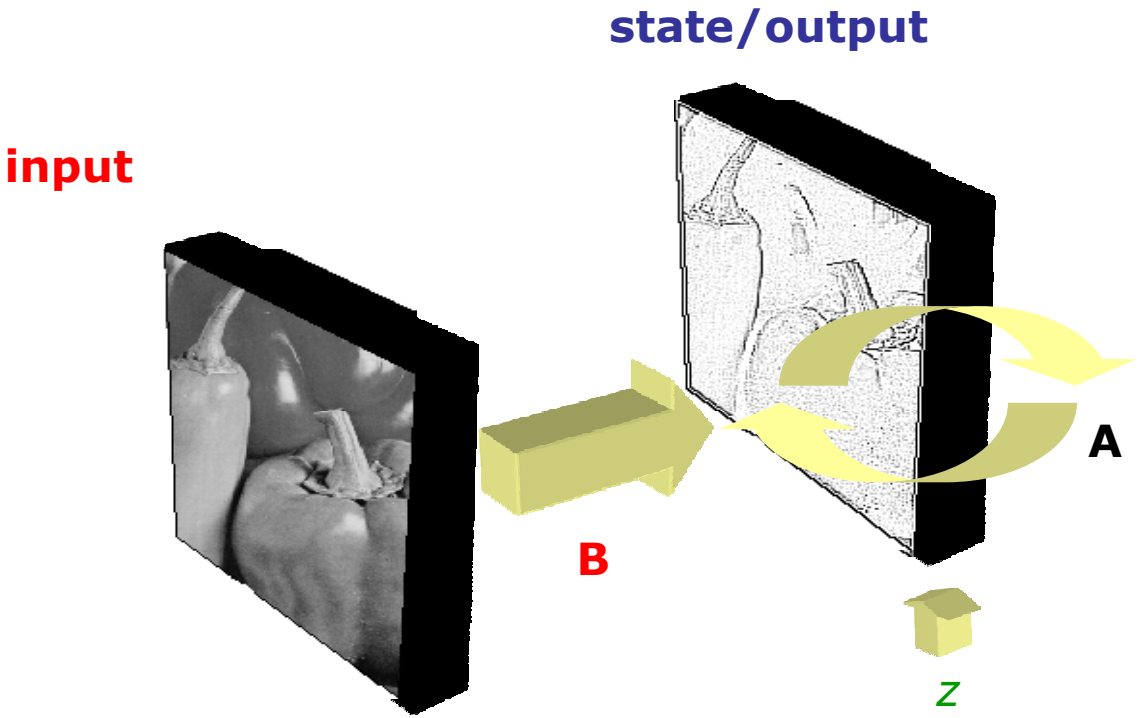
Topographic Sensor-Processors

Concept of Concurrent Sensory-Processing

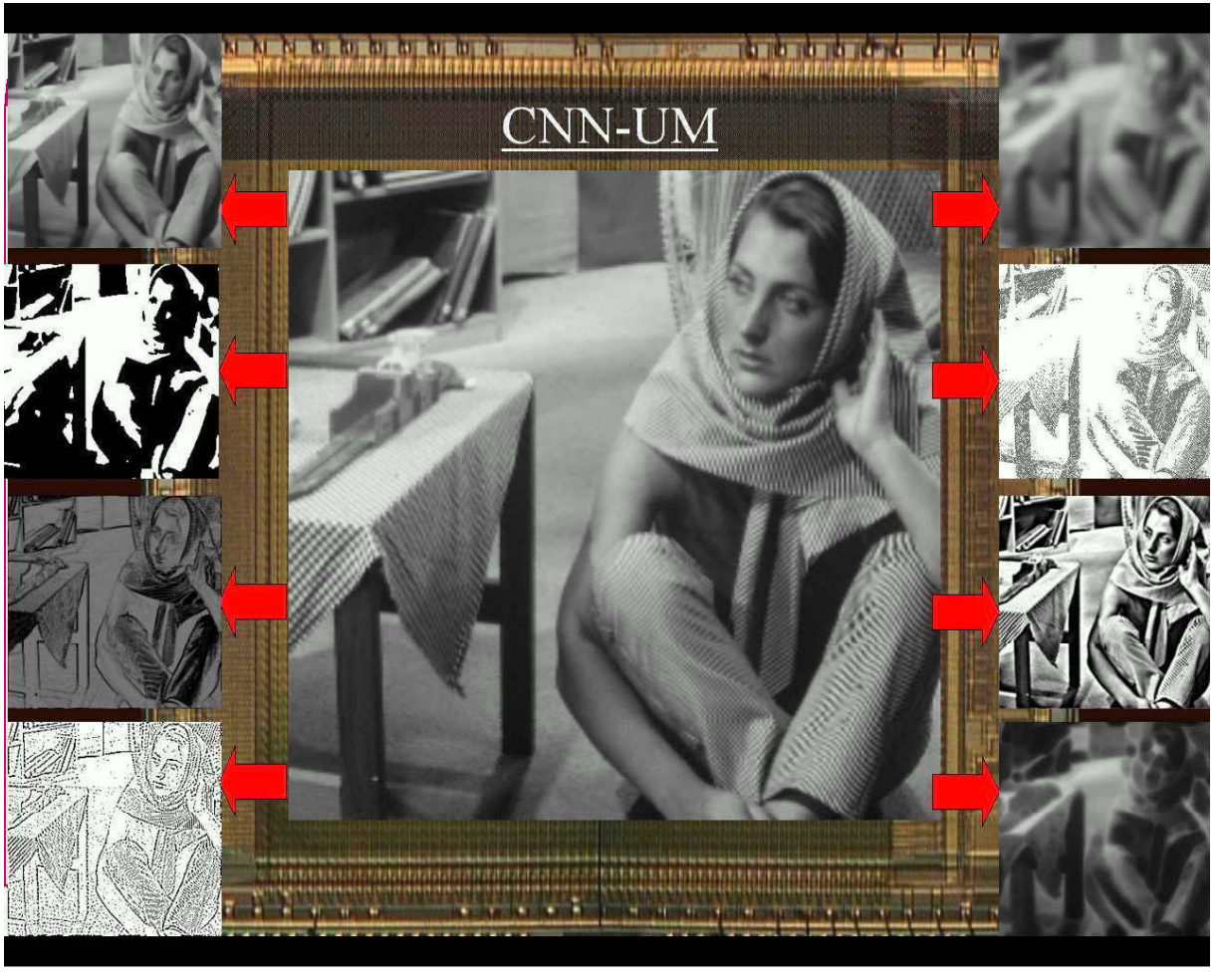
Multi-Functional Pixels

Rationale for Analog Pre-Processing

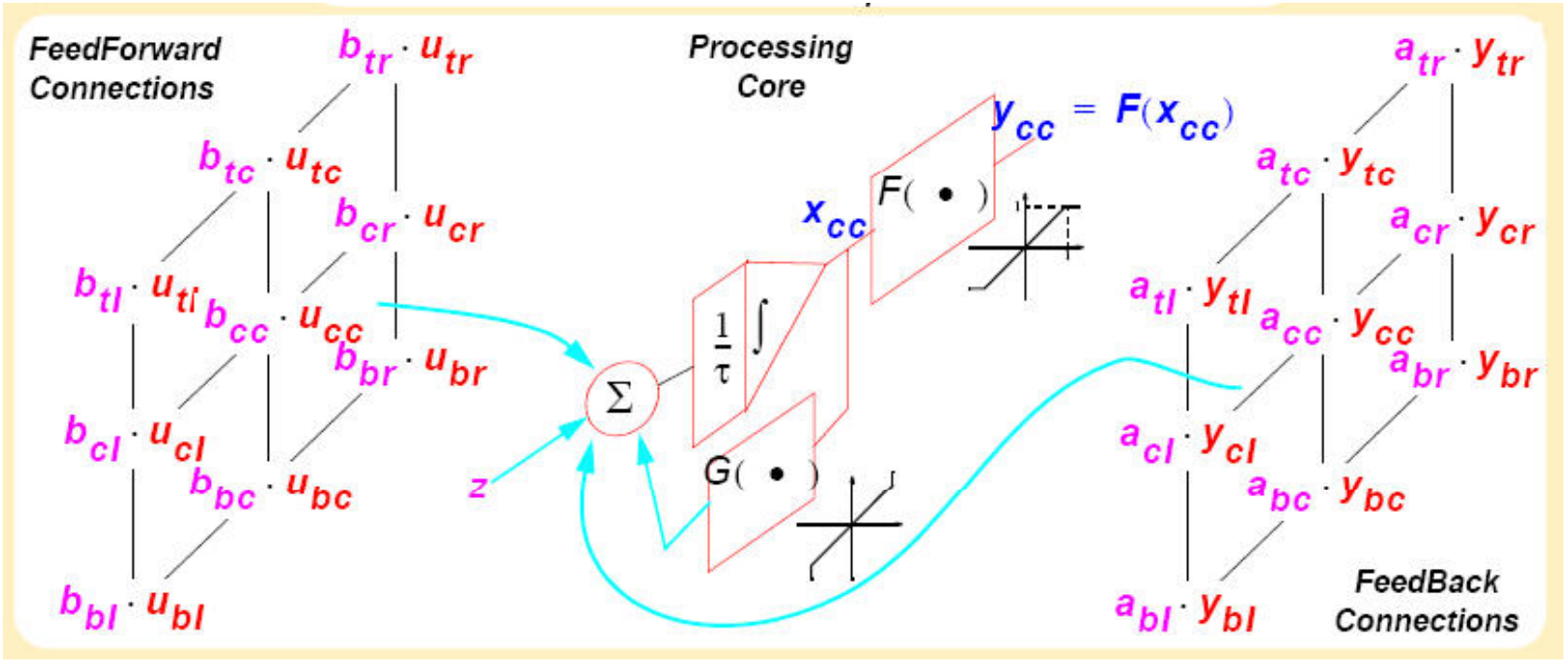
Concept of Concurrent Sensor-Processing



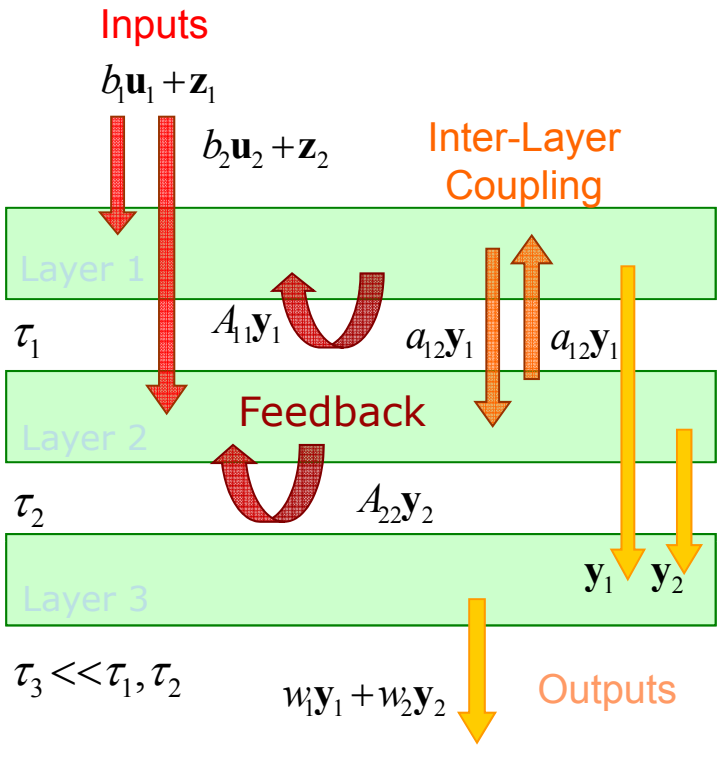
Multiple Signal Representations

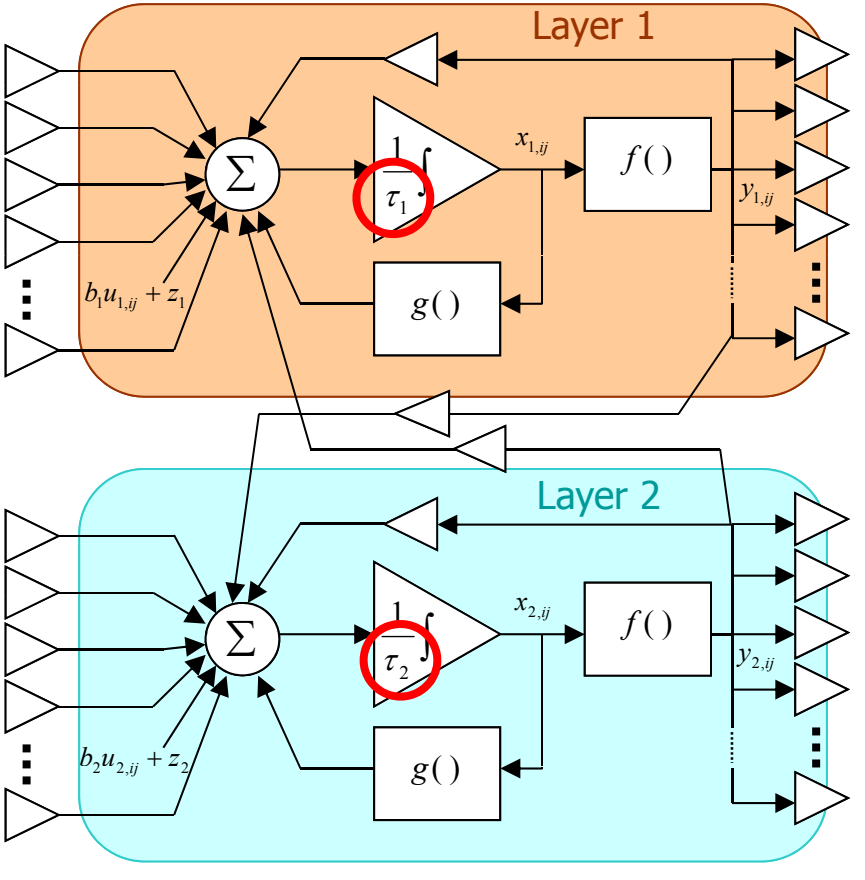


CNN Single Layer Interactions



CNN Multi-Layer Interactions





Programming Reaction-Diffusion Equations

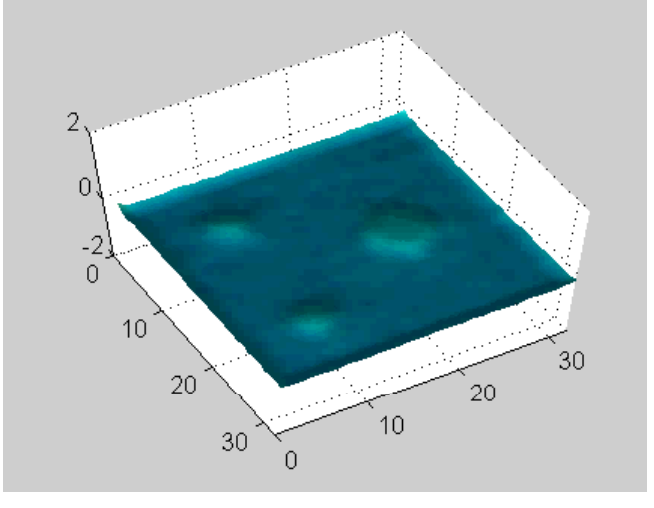
Multi-Layer Interactions

$$\frac{d}{dt}\phi_i(x,y,t) - c_i\nabla^2\phi_i(x,y,t) = \alpha_i\phi_i(x,y,t) + \beta_i\phi_i(x,y,t_0) + \gamma_{ij}\phi_j(x,y,t)$$

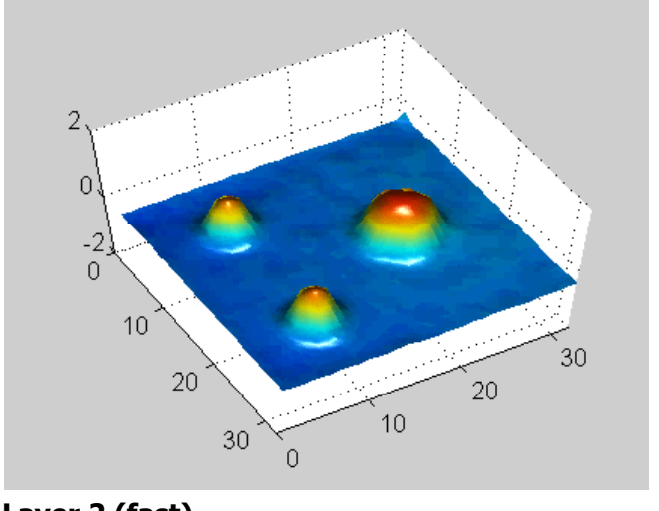
diffusion reaction

Wave propagation in active media

[*Perona & Malik 1990*]



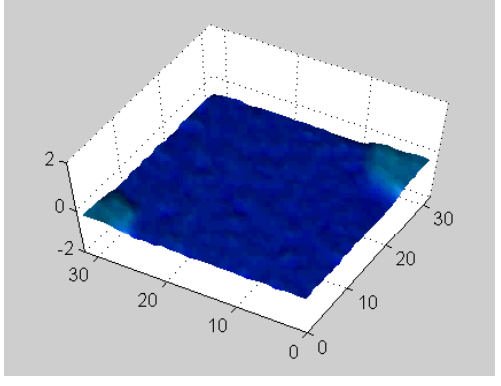
Layer 1 (slow)



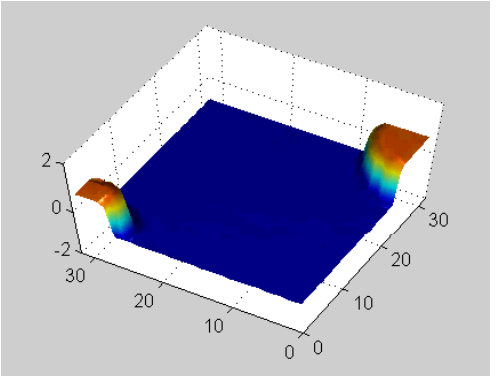
Layer 2 (fast)

Multi-Layer Interactions

Traveling Waves



Layer 1 (slow)



Layer 2 (fast)

$$\mathbf{A}_1 = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1.5 & 1 \\ 1 & 1 & 1 \end{bmatrix} \quad \mathbf{A}_2 = \begin{bmatrix} 0.6 & 0.8 & 0.6 \\ 0.8 & -0.6 & 0.8 \\ 0.6 & 0.8 & 0.6 \end{bmatrix}$$

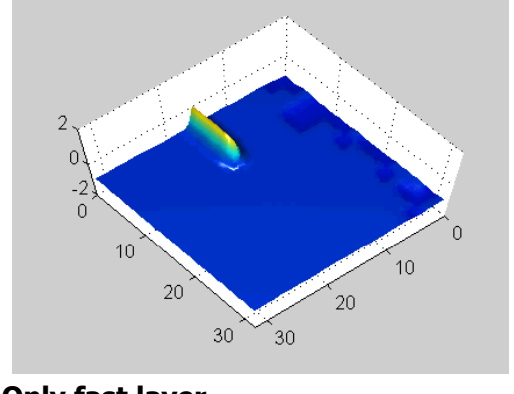
$$a_{21} = 4.5 \quad a_{12} = -4.2$$

$$b_1 = 0 \quad b_2 = 5$$

$$z_1 = 0.6 \quad z_2 = -2.7$$

$$\boldsymbol{\tau}_1 : \boldsymbol{\tau}_2 = 16 : 1$$

Spiral Wave



Only fast layer

$$\mathbf{A}_1 = \begin{bmatrix} 0.6 & 0.8 & 0.6 \\ 0.8 & -0.3 & 0.8 \\ 0.6 & 0.8 & 0.6 \end{bmatrix} \quad \mathbf{A}_2 = \begin{bmatrix} 0.6 & 0.8 & 0.6 \\ 0.8 & -0.9 & 0.8 \\ 0.6 & 0.8 & 0.6 \end{bmatrix}$$

$$a_{21} = 6 \quad a_{12} = -3$$

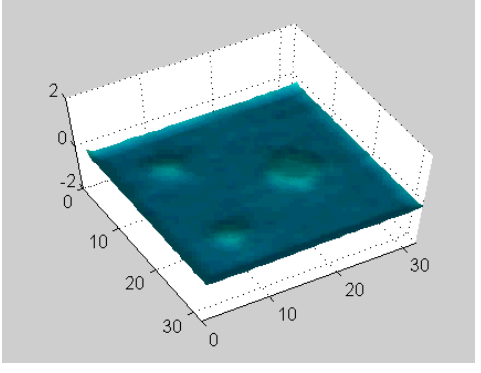
$$b_1 = 0.0 \quad b_2 = 3.9$$

$$z_1 = -4.5 \quad z_2 = -3.6$$

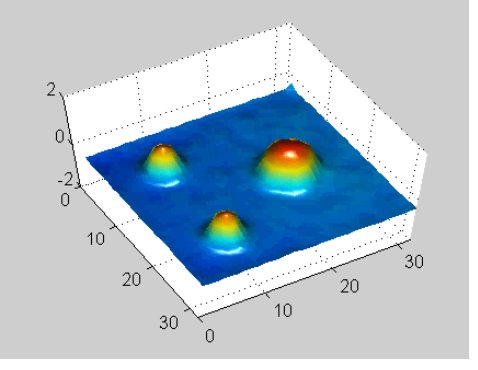
$$\boldsymbol{\tau}_1 : \boldsymbol{\tau}_2 = 8 : 1$$

Multi-Layer Interactions

Long Distance Inhibition in the IPL



Layer 1 (slow)



Layer 2 (fast)

$$\mathbf{A}_1 = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1.5 & 1 \\ 1 & 1 & 1 \end{bmatrix} \quad \mathbf{A}_2 = \begin{bmatrix} 0.6 & 0.8 & 0.6 \\ 0.8 & -0.6 & 0.8 \\ 0.6 & 0.8 & 0.6 \end{bmatrix}$$

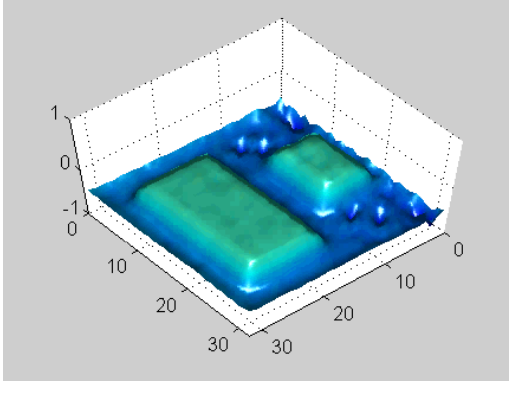
$$a_{21} = 3.3 \quad a_{12} = -5.4$$

$$b_1 = 0 \quad b_2 = 3$$

$$z_1 = 0.6 \quad z_2 = -2.7$$

$$\boldsymbol{\tau}_1 : \boldsymbol{\tau}_2 = 16 : 1$$

Spatial-Temporal Detection of Edges in the OPL



Only fast layer

$$\mathbf{A}_1 = \begin{bmatrix} 0.5 & 0.8 & 0.5 \\ 0.8 & -3.6 & 0.8 \\ 0.5 & 0.8 & 0.5 \end{bmatrix} \quad \mathbf{A}_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

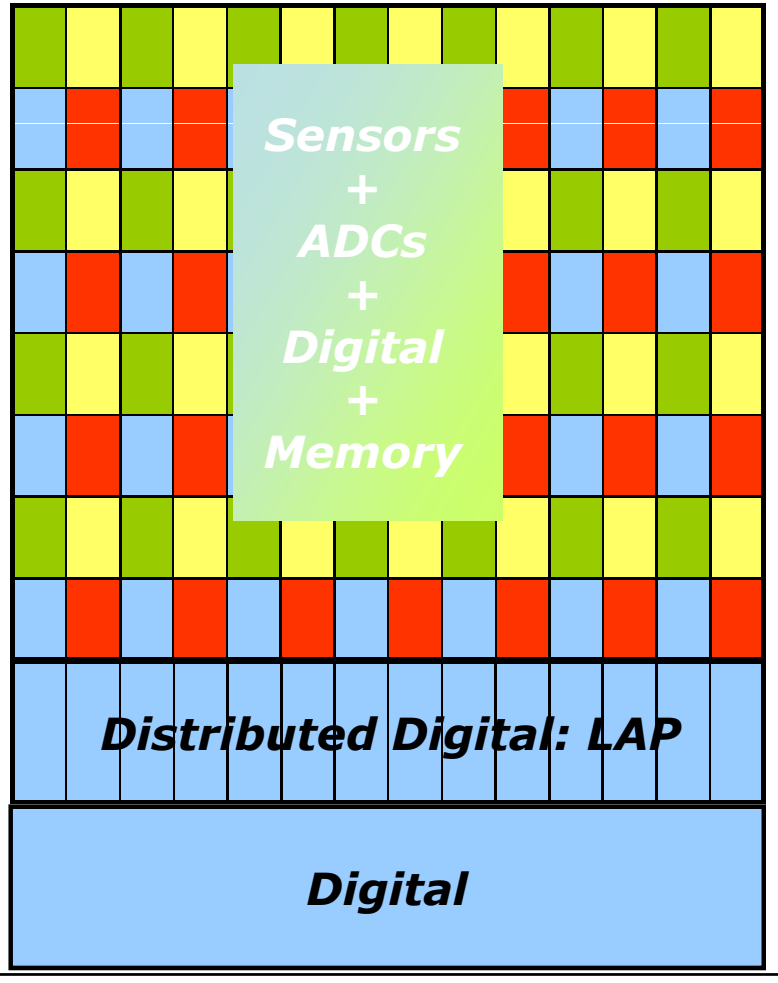
$$a_{21} = 4.5 \quad a_{12} = -5.7$$

$$b_1 = 0.0 \quad b_2 = 3.0$$

$$z_1 = -9 \quad z_2 = 0$$

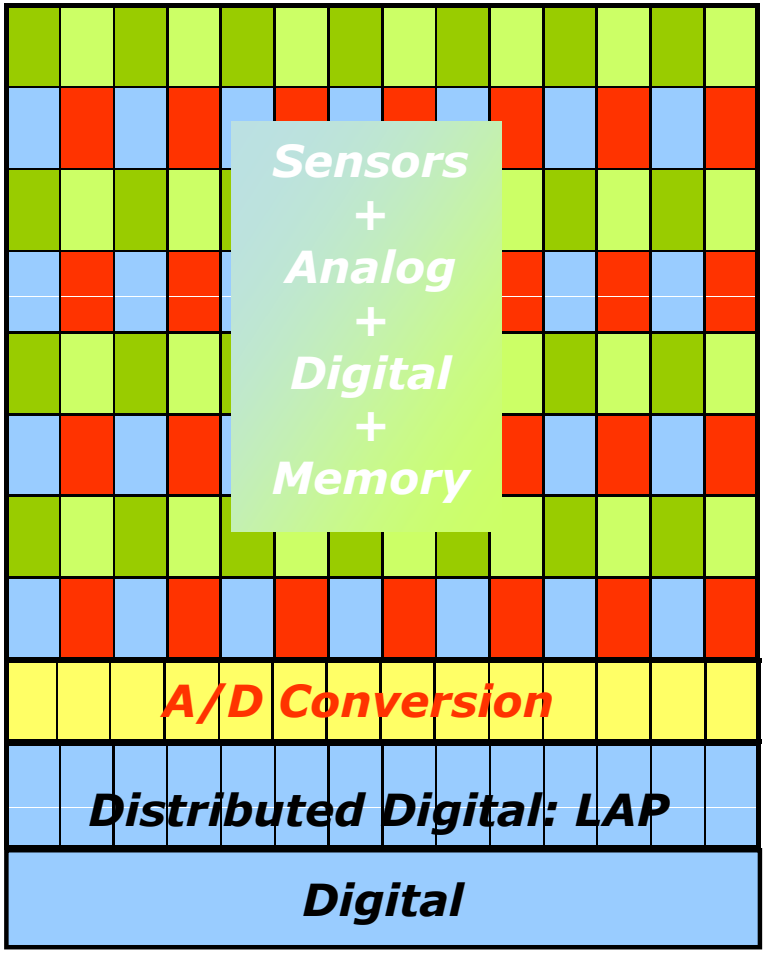
$$\boldsymbol{\tau}_1 : \boldsymbol{\tau}_2 = 6 : 1$$

Topographic ADCs + Digital Processing



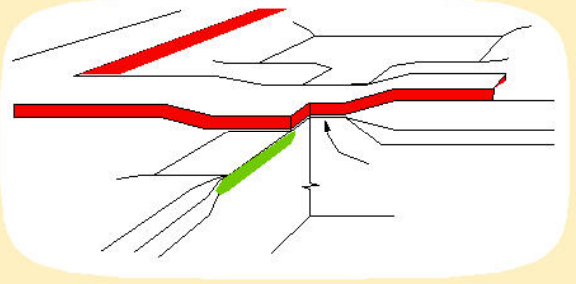
- Smaller spatial resolution: trade-off with processing
- Larger system operation predictability and robustness: analog only for ADCs
- Smaller spurious signal interactions
- Larger flexibility and programmability: only digital processing
- Functionality and efficiency compromised by ADC accuracy
- Large in-pixel memory requirements

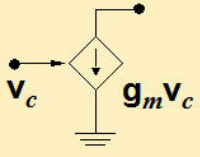
Topographic Mixed-Signal Processing



- ☹ Low spatial resolution: trade-off with processing
- ☹ Involved circuit operation predictability and robustness: analog also for processing
- ☹ Larger spurious signal interactions
- 😐 Involved flexibility and programability: both analog and digital circuits
- ☺ Large computational power and efficiency
- ☺ Small memory requirements
- ☺ Small transfer bottlenecks

The Functional Power of MOST





✓ **Ohmic SI-Region:**

$$I_D \approx k\frac{W}{L}V_{DS}(V_G - V_{T0} - nV_S)$$

V_{DS} must be kept constant

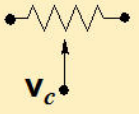
✓ **Saturation SI-Region:**

$$I_D \approx \frac{k}{2n}\frac{W}{L}(V_G - V_{T0} - nV_S)^2$$

Early Voltage is low $\propto L$

✓ **Saturation WI-Region:**

$$I_D \approx k\frac{W}{L}e^{\frac{(V_G - V_{T0} - nV_S)}{nU_T}}$$



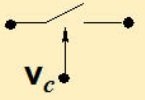
✓ **Ohmic Region:**

$$R_\Omega = \frac{L}{kW}\frac{1}{(V_G - V_{T0} - nV_S)}$$

V_{DS} must be kept small

Large Distortion

$R_\square \sim 10\text{K}\Omega$



✓ **Ohmic Region:**

$$R_\Omega \propto \frac{L}{kW}$$

No offset

Cut-off Region:

$R_{ON} \to \infty$

Charge Injection

✓ **Strong-Inv. Region:**

$$C \propto C_{ox}LW$$

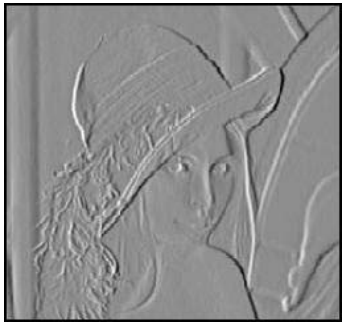
$C_{ox} \sim 3\text{fF/mm}^2$

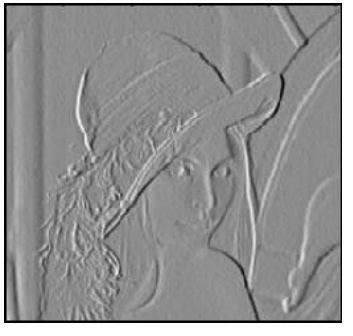
Nonlinear

✓ **Long-Term Memory with Floating Gate**

Visual Inspection of Results



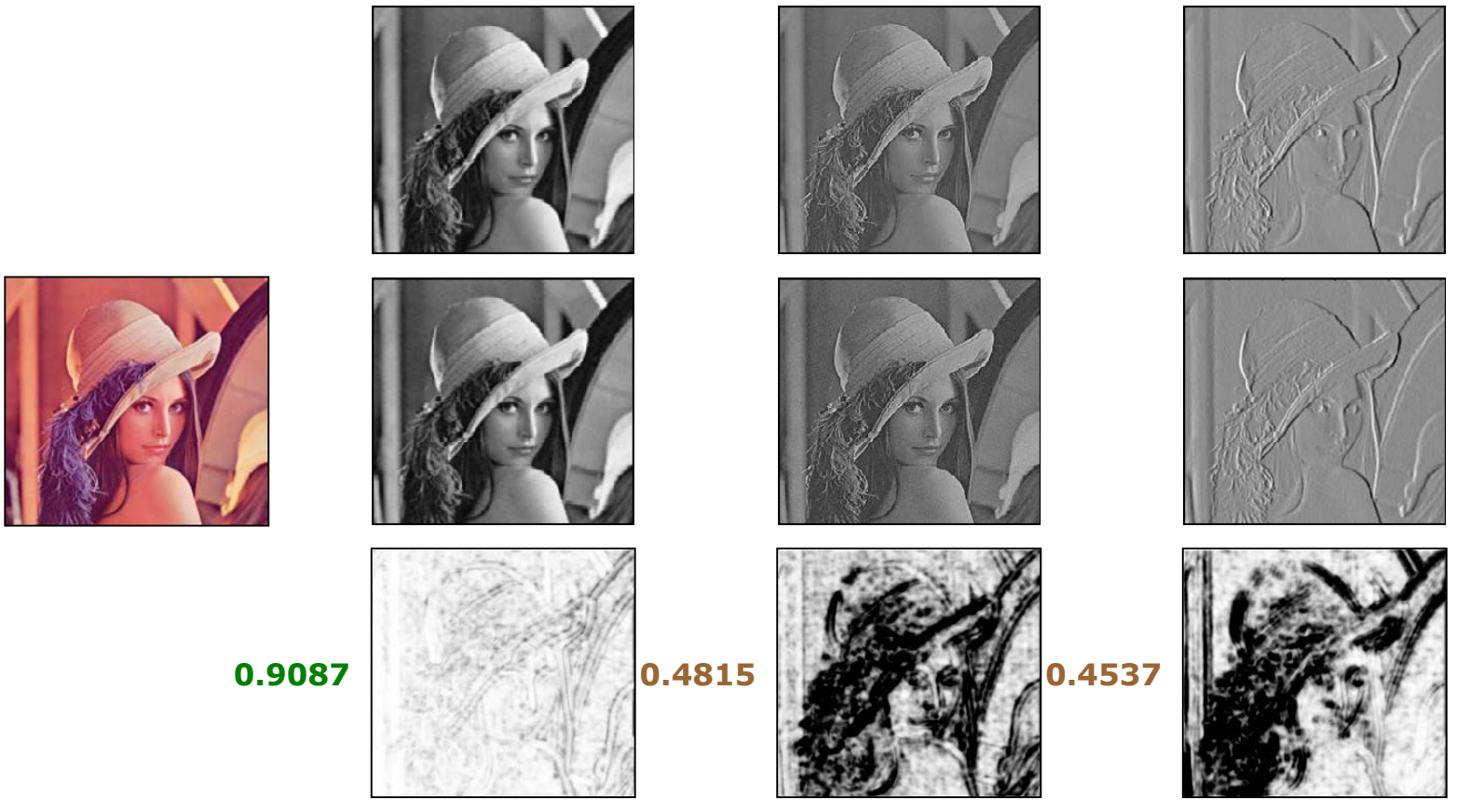



Adding random noise (σ=4LSB) to: 1) Input Image; 2) Coefficients of the convolution kernel at every position; 3) Output Image

[Original from Gustavo Liñán]

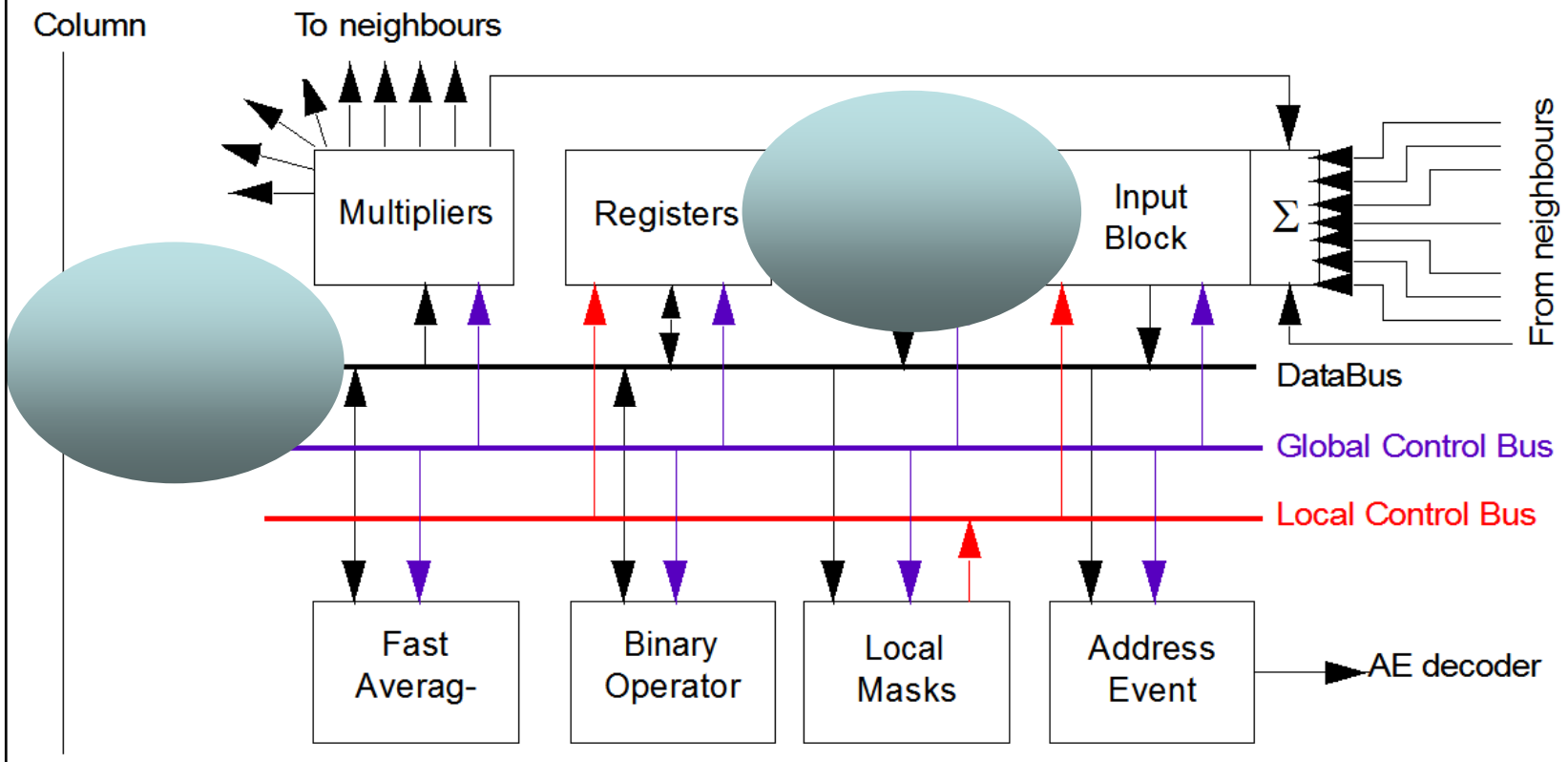
Using Quality Assessment Methods



[Original from Gustavo Liñán]

Z. Wang, et al., "Image quality assessment: From error visibility to structural similarity," *IEEE Transactions on Image Processing*, vol. 13, no. 4, pp. 600-612, Apr. 2004.

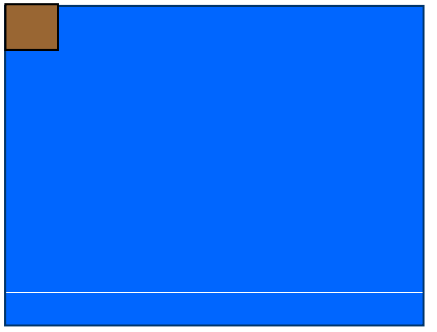
Multi-Functional Pixel Example



The Resolution Compromise

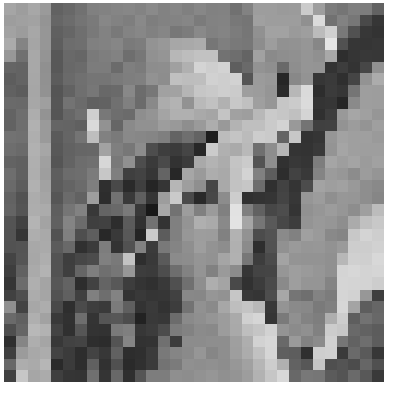
Size of Sensory Pixel

Size of Sensory-Processing Pixel



How Important is Resolution ?

How Important is Resolution ?



512 x 512 **128 x 128** **64 x 64** **32 x 32**

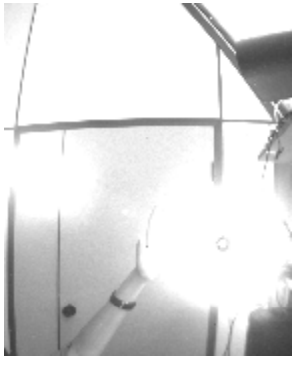
- ***Vision is possible with 25 x 25 "pixels" (within limited field of view)***
- ***Text can be read at 200 words/min (300 words/min with normal vision)***
- ***Students can navigate in complex environments (maze) with confidence***

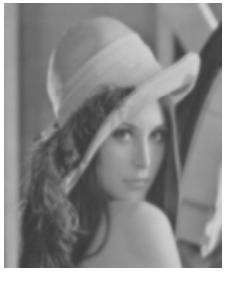
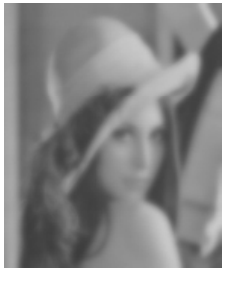
Resolution can be increased through proper design

- ***VGA and up to 1.3Mpixels resolution for Surveillance***
- ***> 1Mpixels for Machine Vision and Automotive***

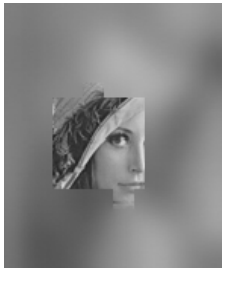
Q-Eye in Operation





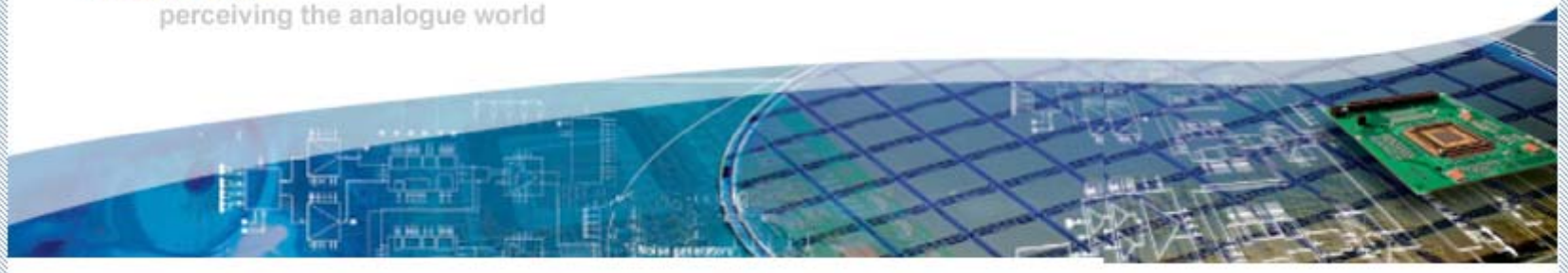







ANAFOCUS

perceiving the analogue world

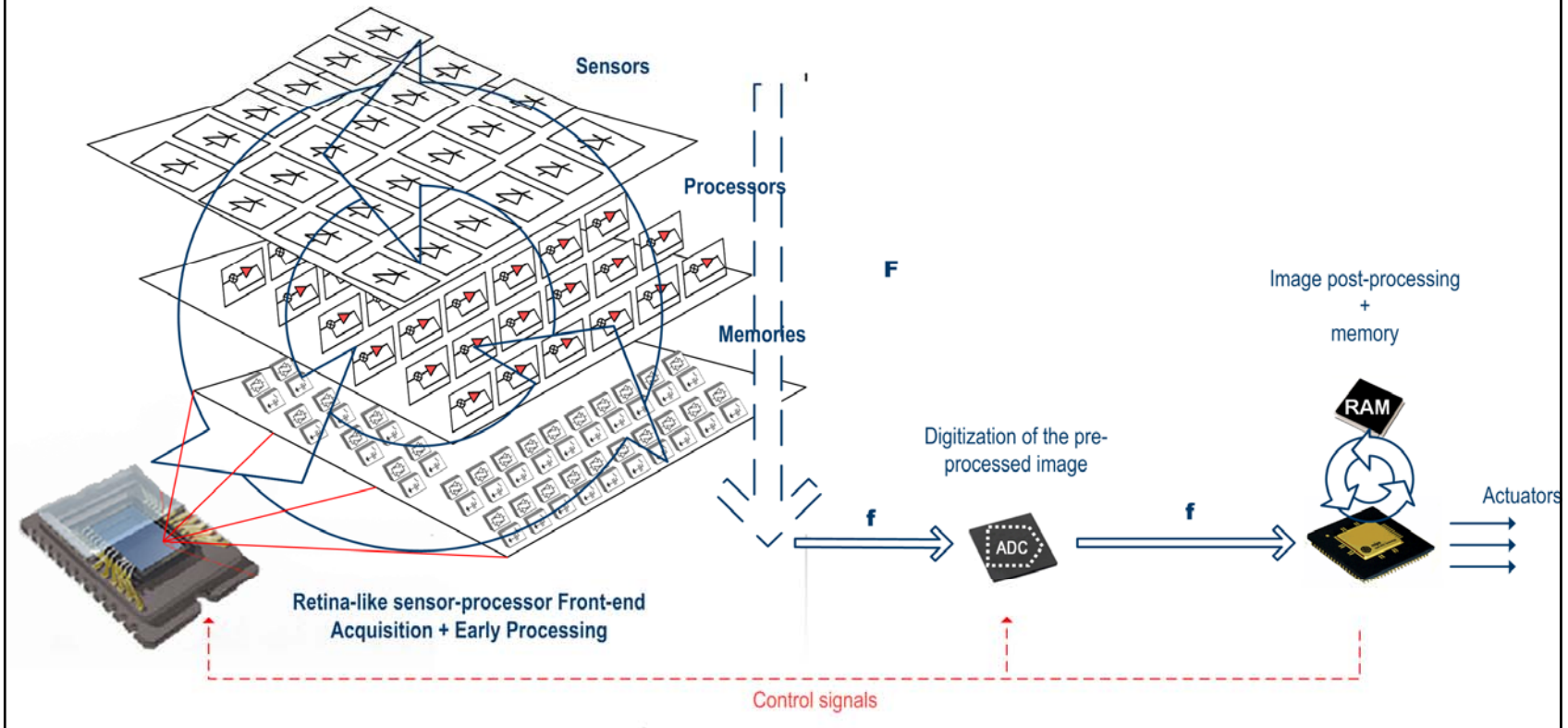


The Eye-RIS system

Architecture

The System in Operation

Multi-Functional Pixel Concept



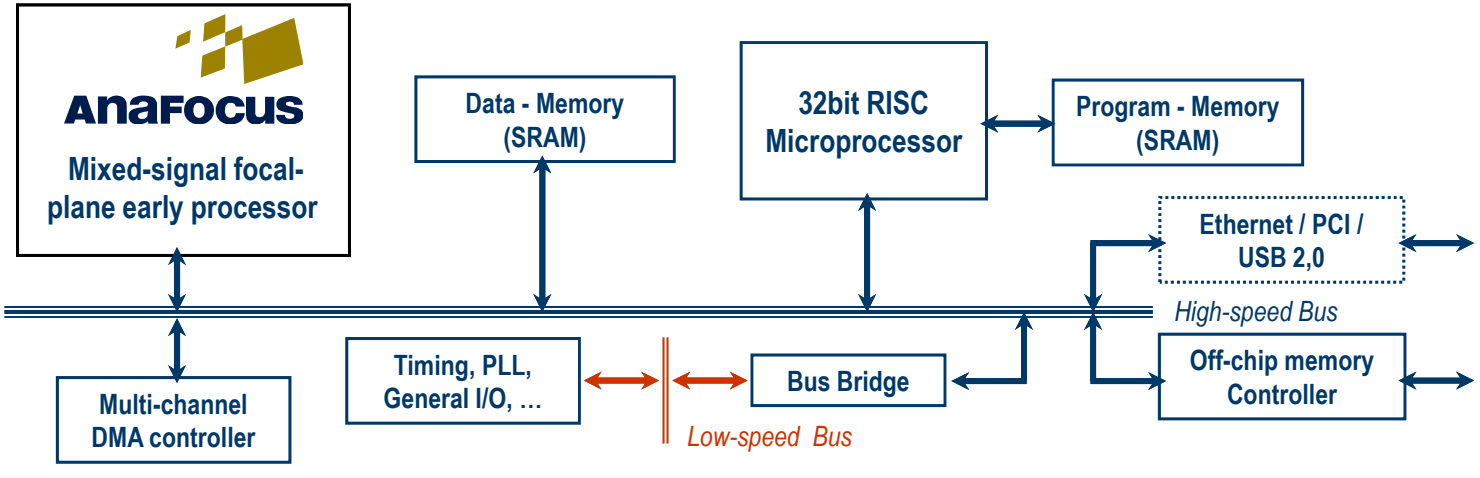
F – Input data flow @ bits per second (bps)

f – Data flow after early processing

f << F

The Eye-RIS™ System

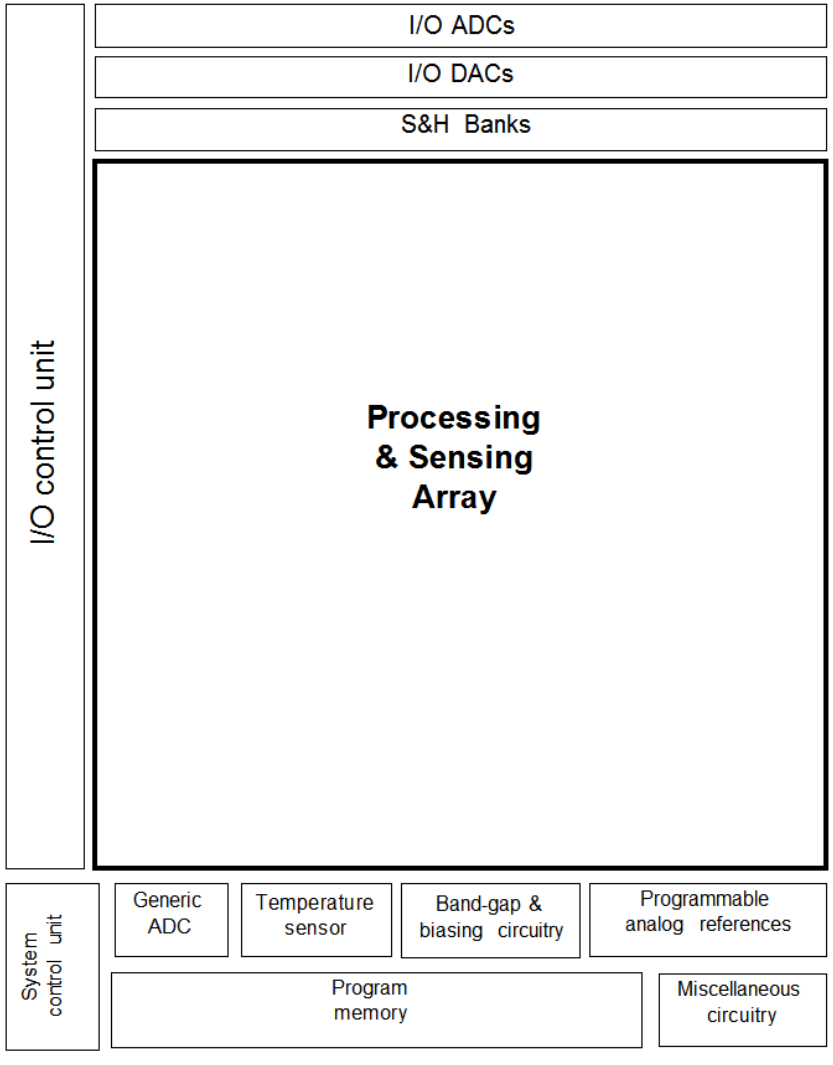
Configurable system which provides an efficient solution for low-to-medium resolution and high frame rates applications



Ultra-high frame rate: *up to 10,000fps@QCIF image resolution*

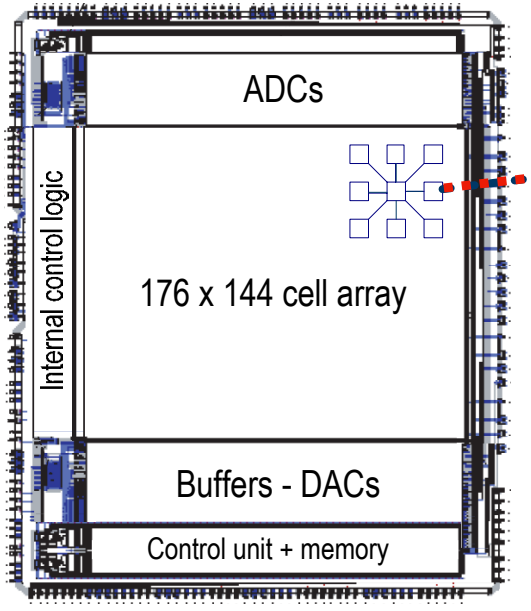
Ultra-low power consumption: *< 10mW@30fps@QCIF image resolution*

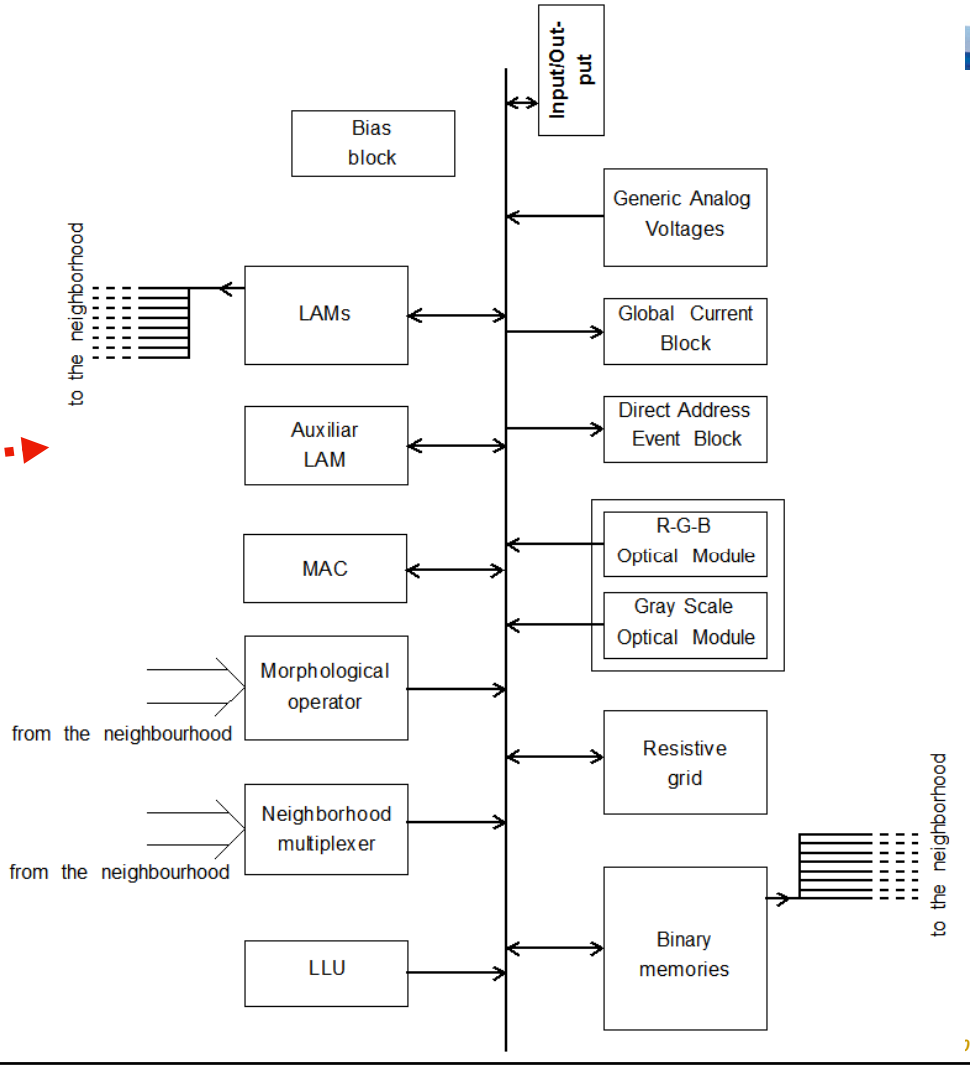
The Q-Eye Chip



- ✓ UMC 0.18µm CMOS 1P5M (1.8V/3.3V) - mixed-signal.
- ✓ High-performance Smart Image Sensor
  - 176 x 144 grey-scale pixels with 29.1µm pitch
  - High-speed non-rolling electronic shutter. Programmable exposure time (controlling step-down to 20ns)
  - Approximated sensitivity of 3V/lux-sec at 550nm
  - 4 +1 (two banks) high-retention analog and 4 binary memories
  - Analog multiplexer for image shifting and analog MAC unit
  - Programmable,3 x 3 neighbourhood pattern matching with 1/0/d.n.c.pattern definition (fast morphological functions)
- ✓ On-chip bank of high-speed ADCs and DACs.
- ✓ Multiple I/Os and high-speed communication ports

Q-Eye Pixel


ADCs
Internal control logic
176 x 144 cell array
Buffers - DACs
Control unit + memory


Input/Out-put
Bias block
Generic Analog Voltages
to the neighborhood
LAMs
Global Current Block
Auxiliar LAM
Direct Address Event Block
MAC
R-G-B Optical Module
Gray Scale Optical Module
Morphological operator
from the neighbourhood
Resistive grid
Neighborhood multiplexer
from the neighbourhood
to the neighborhood
LLU
Binary memories

Main Features

Q-Eye focal-plane processor

- 176 x 144 spatial resolution
- Monochrome image sensor with 3.2V/(lux·sec) sensitivity
- Maximum frame rate (sensing + processing) of over 10,000fps
- Advanced pixel architecture combining image acquisition, image processing and storage:
  - Multi-mode image sensing, analogue & binary memories, analogue multiplexor for image shifting, analogue MAC unit, programmable LUT, resistive grid for controllable smoothing…

Digital control & post-processing

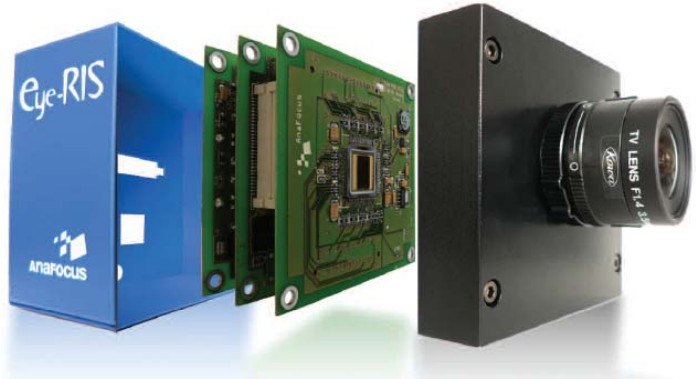
- ALTERA NIOS-II 32-bit RISC microprocessor
- 1.17 DMIPS/MHz performance at 70MHz operation frequency
- 32Mb SDRAM for program and image/data storage

Communications

- SPI port, UART, 2xPWM ports and GPIOs, USB 2.0, and GigE
- JTAG Controller
- 1.5W typical power consumption

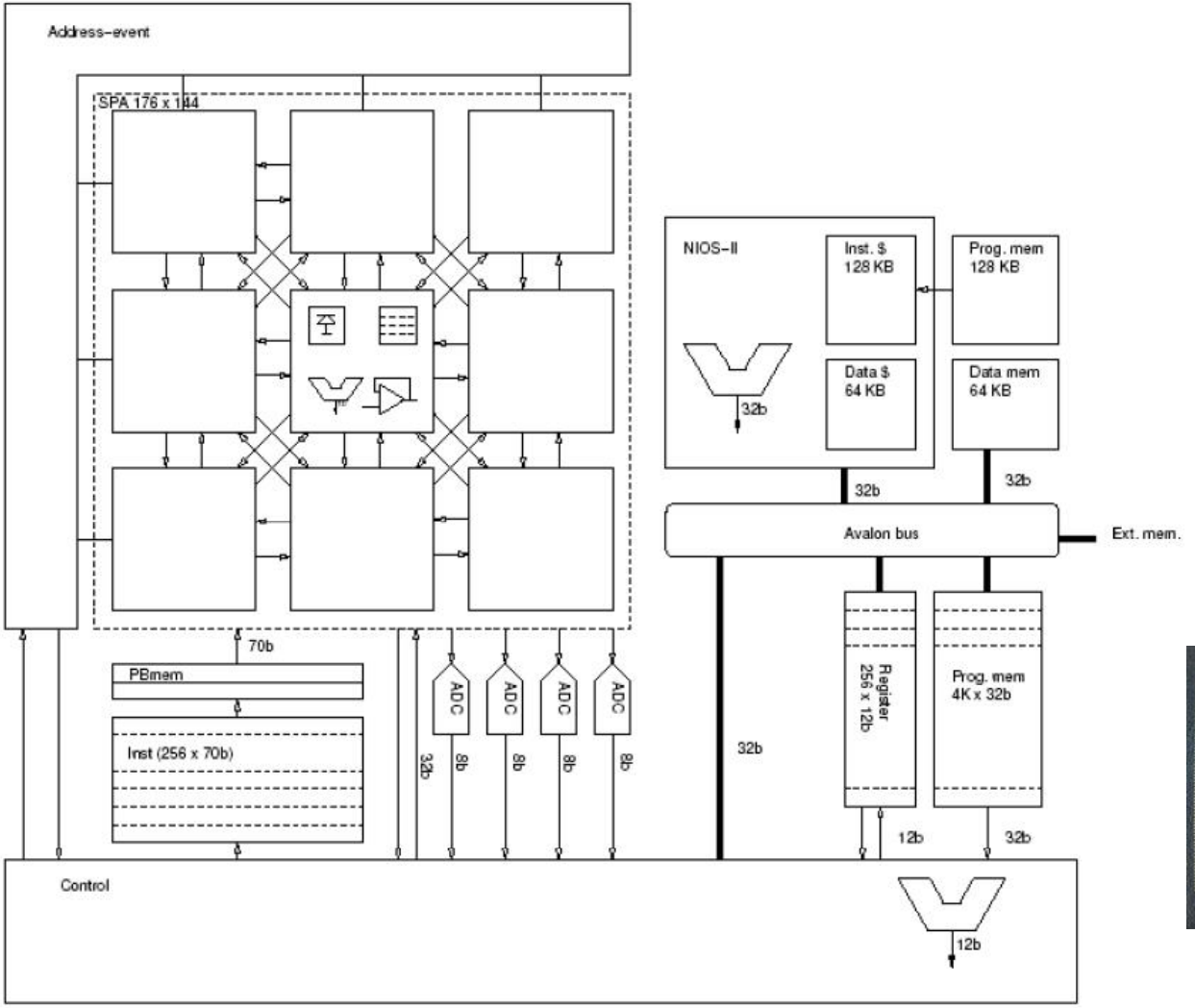
Application development kit

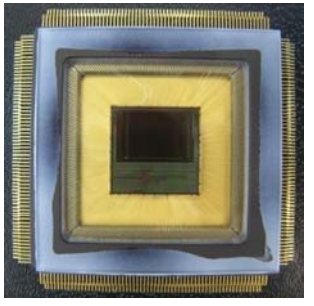
- *Application Development Kit* including: Project builder, C compiler, assembler, linker, and source-code debugger.
- *Image-processing library* including basic routines such as: point-to-point operations, spatial filtering operations, morphological operations and statistical operations



Eye-RIS™ v1.2 vision system

The First True Bio-inspired VSoC: Eye-RIS™ v2.1





The First True Bio-inspired VSoC: Eye-RIS™ v2.1

Main Features

Main Features

Q-Eye focal-plane processor

- 176 x 144 spatial resolution
- Monochrome image sensor with 3.2V/(lux·sec) sensitivity
- Maximum frame rate (sensing + processing) of over 10,000fps
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- 1.17 DMIPS/MHz performance at 100MHz operation frequency

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- SPI port, UART, 2xPWM ports and GPIOs, USB 2.0 interface, and
- JTAG Controller
- <700mW typical power consumption

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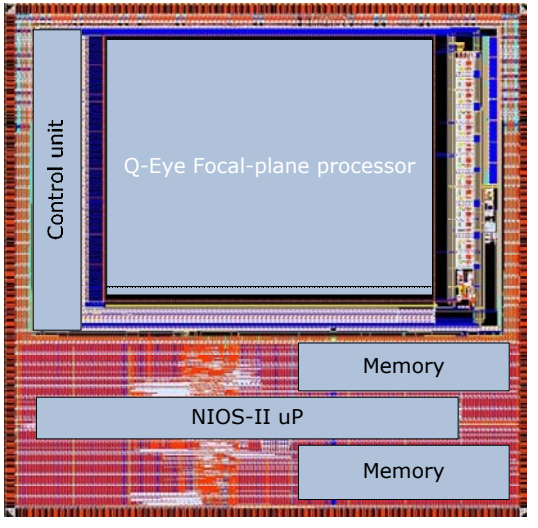
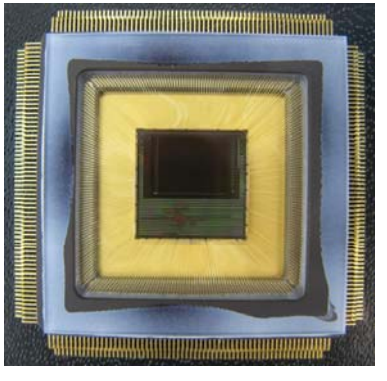
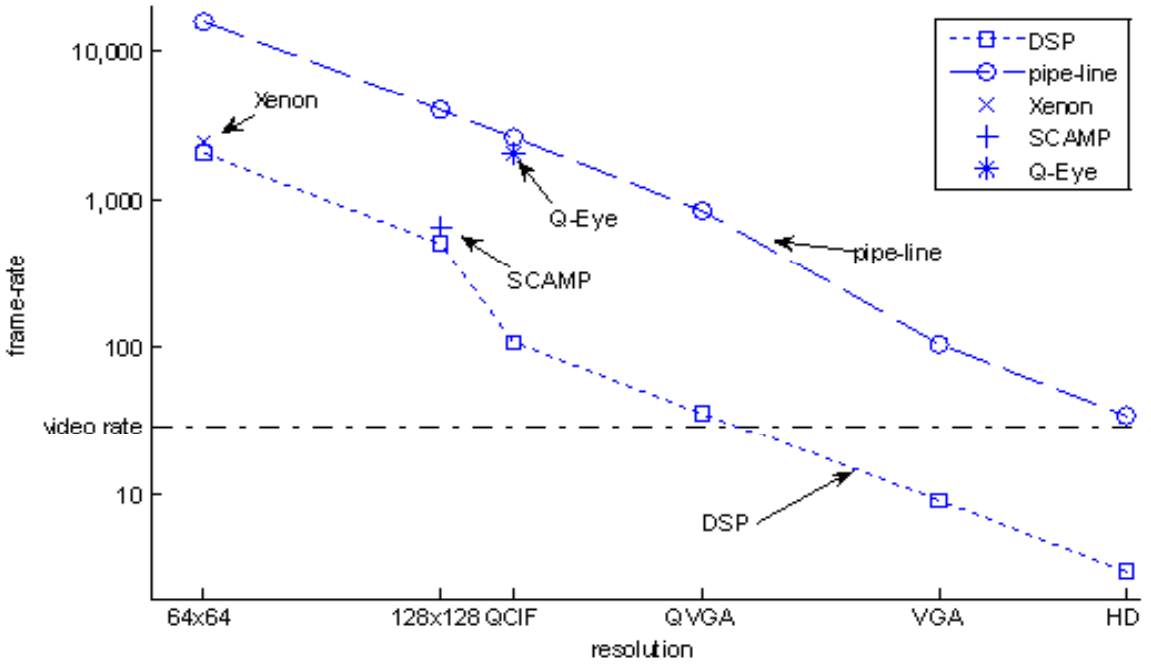




Processor Comparison



Benchmark: Each of the processors calculated 20 convolutions, 2 diffusions, 3 means, and 40 morphology and 10 global ORs. Note: Only the DSP and the pipe-line multi-core (FPGA) architectures support trading between resolution and frame-rate

[Original from Csaba Reckeczky]

Processor Comparison

	General							
	Type	Tech. [nm]	Area [mm]	Data [Mb]	Pow [W]	Clock [MHz]	GOPs	mW GOP
Xetal-1	SIMD LPA	180	25	0,05	1,6	24	5	320
IMAP	SIMD LPA	180	121	2	2	100	51,2	39,06
Xetal-2	SIMD LPA	90	74	10	0,64	84	107	6
Q_Eye	SIMD SPA	180	37,5	Int.	0,1	50	250	4
EyeRIS	SIMD SPA	180	92	0,5	1	50	250	4
(NIOS)				0,5				
CVSoC	SIMD LPA	180	165		0,8	90	92,16	8,681

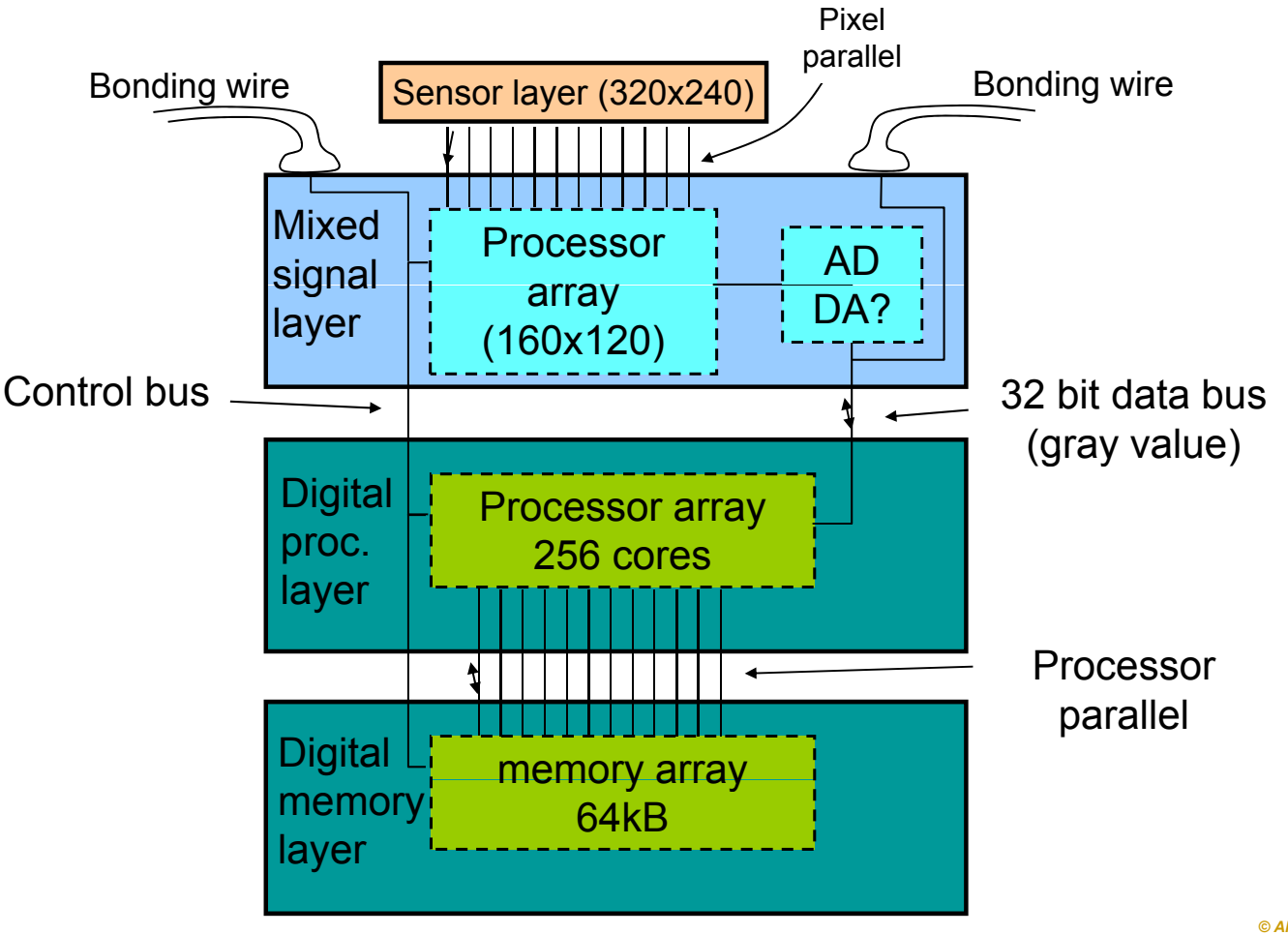
Processor Comparison

	DSP (DaVinci+)	Pipe-line (FPGA++)	Course-grain (Xenon)	Fine-grain (SCAMP/Q-Eye)
Silicon technology (micron)	0.065	0.065	0.18	0.35/0.18
Silicon area mm²			25	50/60
Power consumption	1.25 W	2-3W	0.08 W	0.20 W
Arithmetic proc. clock speed	600 MHz	250 MHz	100 MHz	1,2 -2.5 MHz
Number of arithmetic proc.	8	120	256	16384
Efficiency of arithmetic calc.	75% *	100%	80% **	50% *
Arit. computational speed	3.6 GMAC	30 GMAC	20 GMAC	~20GOPS***
3x3 convolution time	42.3 µs****	4.9 µs	12.1 µs	22 µs ***
Arithmetic speed-up	1	8.6	3.5	1.9
Morph. proc. clock speed	600 MHz	83 MHz	100 MHz	1,2 -5 MHz
Number of morphologic proc.	64	864	2048	147456
Morphologic processor kernel type	2 × 32 bit	96 × 9 bit	256 × 8 bit	16384 × 9 bit
Efficiency of morphological calc.	28% *	100%	90% **	100%
Morphologic computational power	10 GOPS	71 GOPS	184 GOPS	737 GOPS
3x3 morphologic operation time	13.6 µs****	2.05 µs	1.1 µs	0.2 µs
Morphologic speed-up	1	6.6	12.4	68.0

+ Texas Instrument DaVinci video processor (TMS320DM6443)
++ Xilinx Spartan 3A DSP FPGA (XC3SD3400A)
* due to data access
** due to pipe-line operations
*** no multiplication, scaling with a few discrete values
**** these data intensive operators slow down significantly when the image does not fit to the internal memory (typically above 128x128 for a DaVinci, which has 64kByte internal memory)

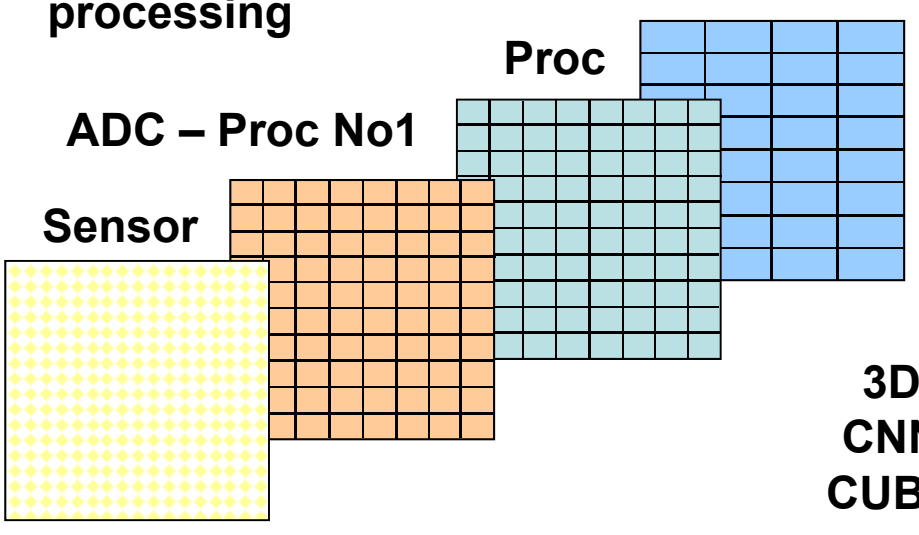
[Original from Csaba Reckeczky]

3-D Parallel Processing Multi-Layer Architectures



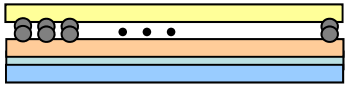
3-D Integration

Topographic, layered sensing-processing

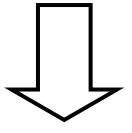


3D CNN CUBE

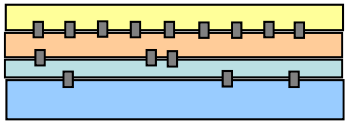
AFRL BB Process



Bump bonding:

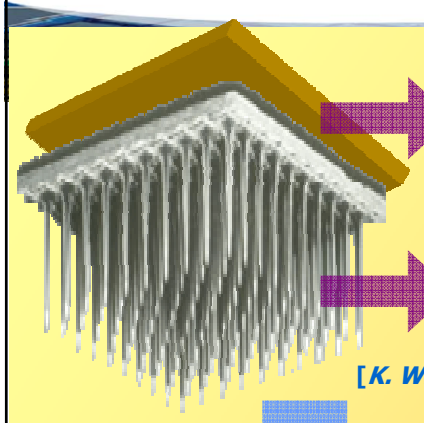


3D stacking:



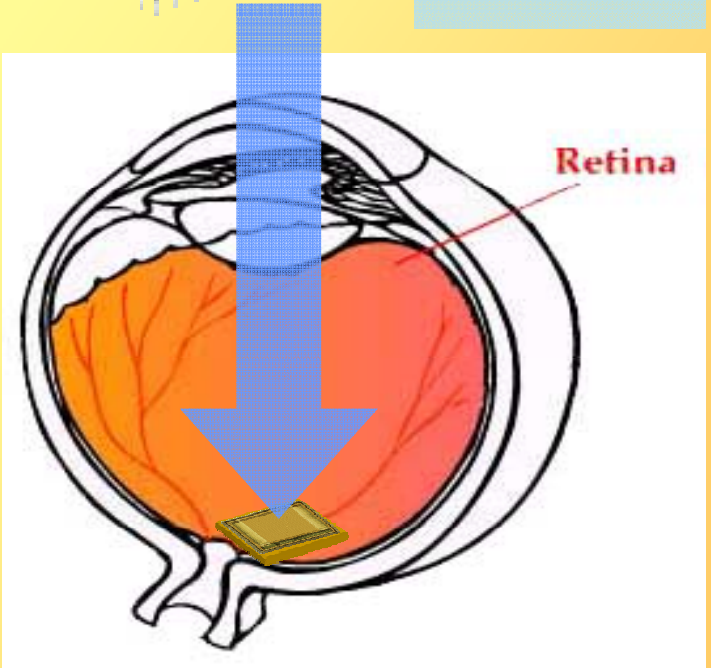
MITLL Low-Power FDSOI CMOS Process

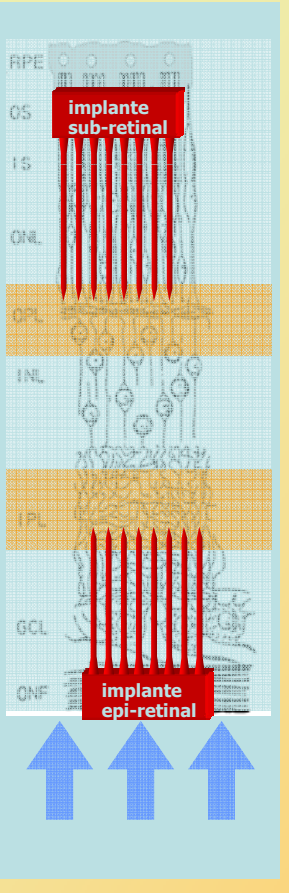
Visual Prosthesis

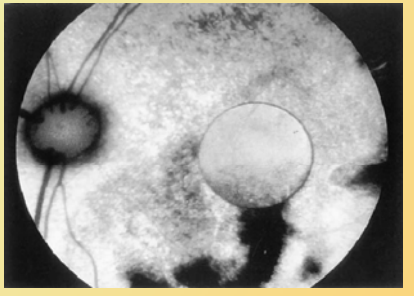


Retina Coder
+
Electrode Driving
+
Electrode Array

[K. Wise, D. Kipke,U. Michigan]

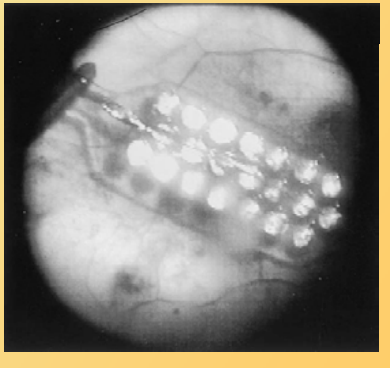






Sub-Retinal Implant

[Chow et. al 2001]



Epi-Retinal Implant

[Humayun et. al 1999]

Discussion

- ***VSoCs** are still like **science fiction** toys for industry*
- ***Even smart CMOS sensors are not common yet***

  A real challenge for engineering !!

- ***We can take advantage of nature through understanding***
  - ***Parallel and concurrent sensory-processing***
  - ***Multi-scale representation***
  - ***Signal coding***

- ***Close interaction and collaboration between analog and digital circuitry is needed for efficient VSoC design.***