

Efficiency of LBM Applications on Low-Power Heterogeneous Architectures

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Abstract—As the computing power of High-Performance Computing systems increases, and as a result, its energy consumption increases as well, new architectures arise with the purpose of minimizing energy consumption. An example of this is the hybrid architectures that integrate devices from different architectures into a single chip (System on Chip - SoC). In this work we evaluate the performance and power consumption of the Lattice Boltzmann method (LBM) in two hybrid architectures: one composed of CPU and GPU processing units integrated into a single chip (AMD Kaveri SoC), and another by CPU units and an FPGA integrated in a single chip (Intel Arria 10 SoC). The performance and power consumption of the method were evaluated using each device individually and also in a collaborative way through the decomposition of its data domain. We also evaluated the execution time of each of its five subroutines in both the architectures and their devices. The experimental results show that the collaborative execution of the method reduces its execution time. However, the execution times of each subroutine show that non-uniform partitioning for the subroutines could further optimize method execution time. Finally, by evaluating the energy consumption, it is possible to observe that, due to the high execution time of the non-optimized method in Arria 10 SoC in comparison to Kaveri SoC, the consumption is equivalent or even higher in Arria 10 SoC.