Optimization Strategies for Scientific Applications on SX-Aurora TSUBASA

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***Abstract*—A large number of architectures, while attractive and flexible, poses new challenges for the programmer. The memory subsystem, number of cores, and other design decisions increase the difficulty of implementing efficient applications. Some of these issues have been transparently reduced by compilers to the programmer. However, others require source code modifications that differ according to the application and architecture. This work analyzes the performance of loop unrolling and function inlining optimization techniques applied to a vector processor, the SX-Aurora TSUBASA architecture. As a case study, we apply these techniques to the NAS Parallel Benchmarks and an Oil & Gas real-world application, the Reverse Time Migration (RTM). Our experimental results show performance improvements of up to $1,9\times$ compared with the original parallel implementation.**

***Index Terms*—Performance Optimization, NEC SX-Aurora TSUBASA, Reverse Time Migration, Loop unrolling, Inlining.**

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DISCLAIMER

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