EMICRO/SIM 2013

XV Escola de Microeletrônica Sul / 28º Simpósio Sul de Microeletrônica

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Síntese Lógica

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Organização Promoção Apoio

UFRGS CAS SBC IEEE FAPERGS CNPq CAPES CEITEC S.A MICRON

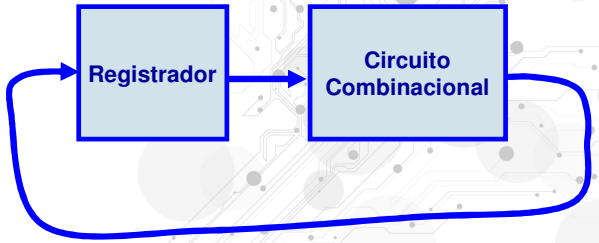
Outline

O que é sintese lógica

- É uma das etapas de síntese de circuitos integrados
- Na qual tabelas-verdade são transformadas em instâncias de primitivas lógicas

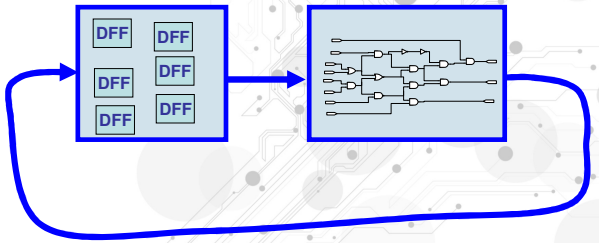
O que entra?

- A entrada da síntese lógica é tipicamente uma descrição RTL
- RTL=Register Transfer Level



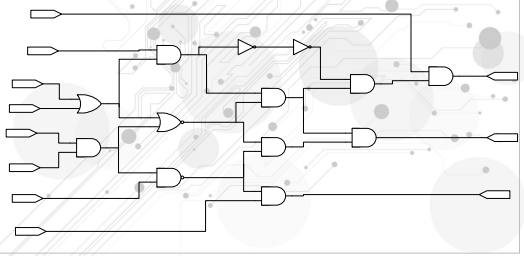
O que sai?

- Uma rede de primitivas lógicas interconnectadas



O que entra e o que sai?

- Entra tabela verdade
- Sai rede de portas lógicas

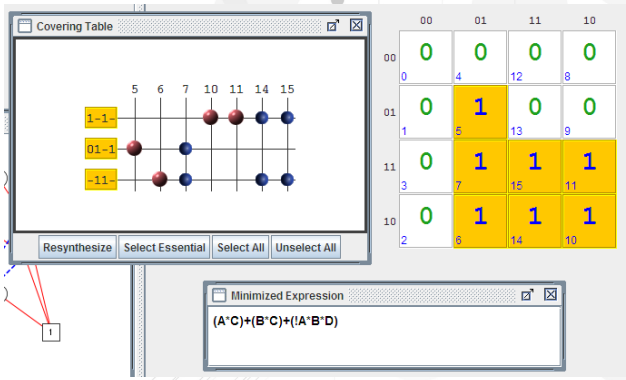


O que acontece no meio?

- Muita coisa
  - Síntese de SOP
  - Fatoração
  - Decomposição funcional
  - Cortes em AIGs
  - Reescrita de AIGs
  - Cobertura de AIGs
  - Mapeamento tecnológico
  - Matching
  - Síntese lógica dentro de células

O que se aprende?

- Método de Quine-McClusckey



O que se aprende?

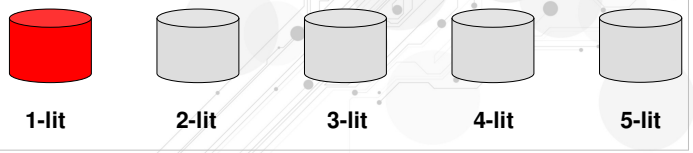
- Fatoração algébrica

ac+bc+!abd

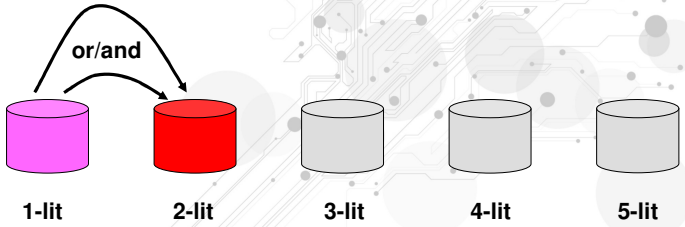
Fatora c: c(a+b)+!abd

Fatora b: ac+b(c+!ad)

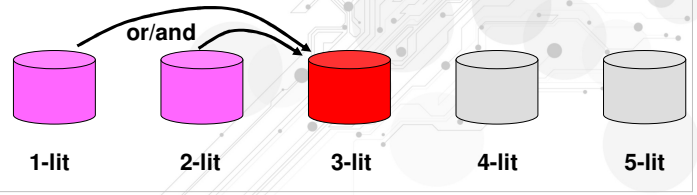
Fatoração - 1



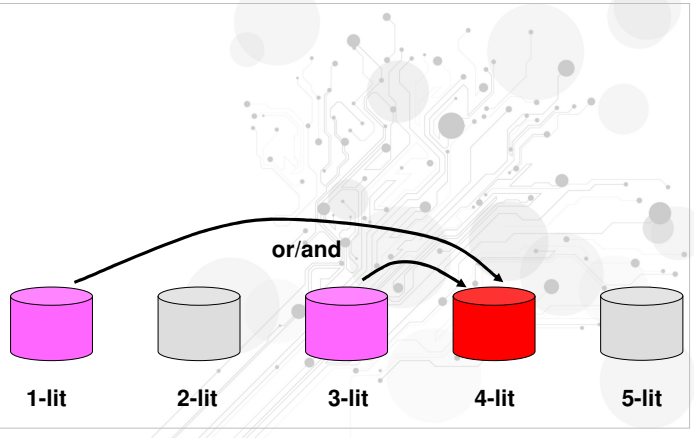
Fatoração - 2



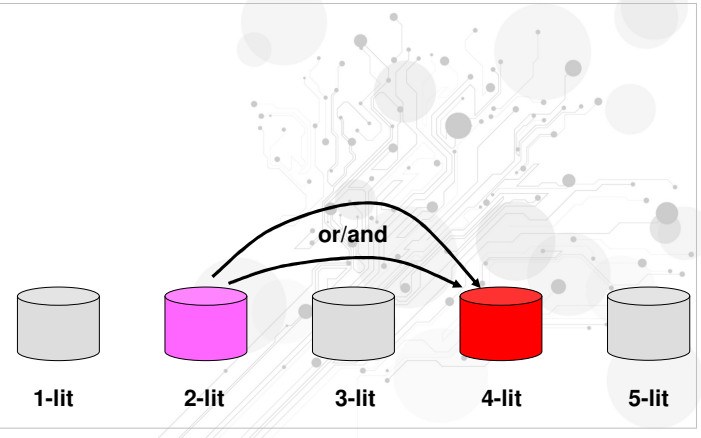
Fatoração - 3



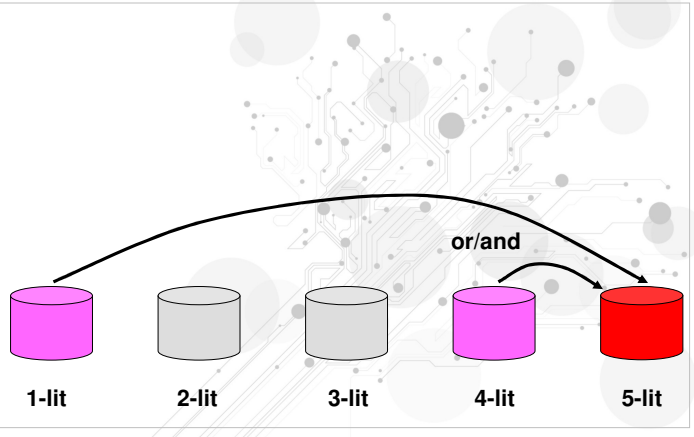
Fatoração - 4



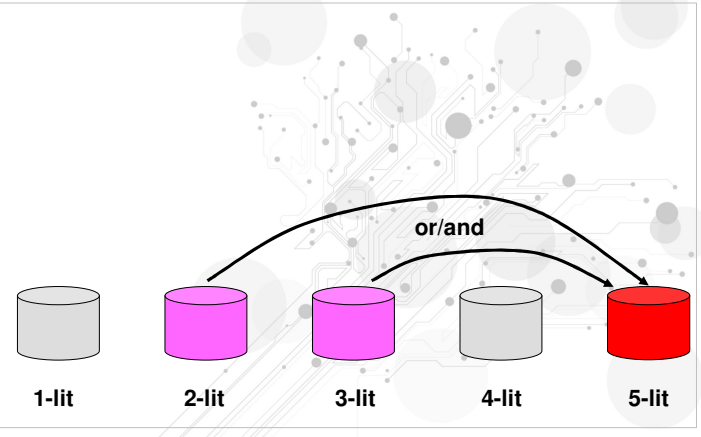
Fatoração - 5



Fatoração - 6



Fatoração - 7



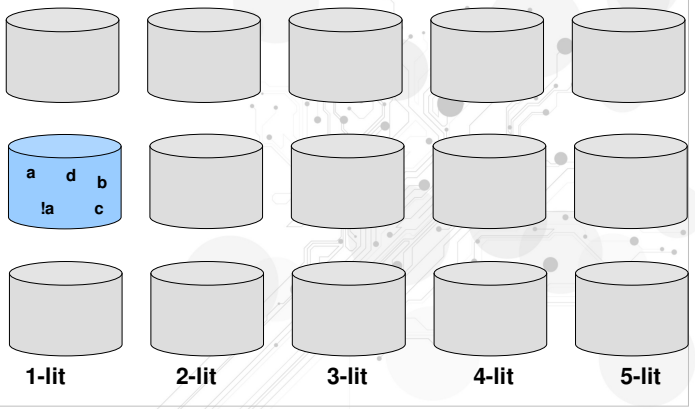
Fatoração

f = (a+b)*(c+!a*d)

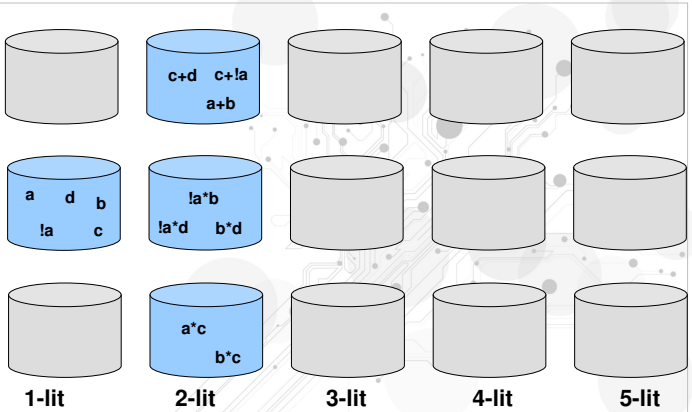
f(a=1) = c
f(a=0) = b*(c+d)
f(b=1) = c+!a*d
f(b=0) = a*c
f(c=1) = a+b
f(c=0) = b*!a*d
f(d=1) = (a+b)*(c+!a)
f(d=0) = (a+b)*c

f(a=0, b=1) = c+d
f(a=0, c=1) = b
f(a=0, c=0) = b*d
f(a=0, d=0) = b*c
f(b=1, c=0) =!a*d
f(b=0, c=1) = a
f(b=1, d=1) =c+!a
f(c=0, d=1) = b*!a
f(a=0, b=1, c=0) = d
f(b=1, c=0, d=1) = !a

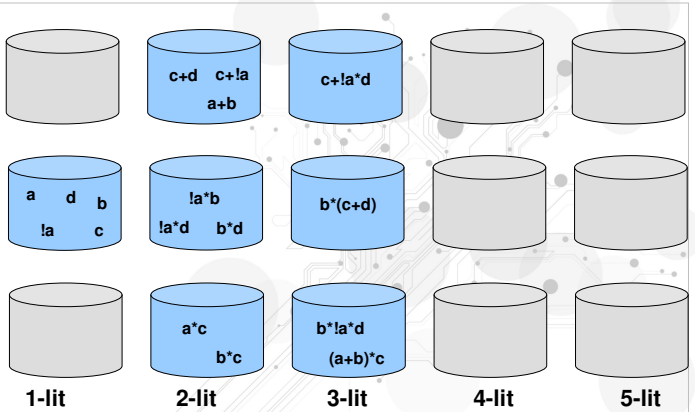
Fatoração – se1



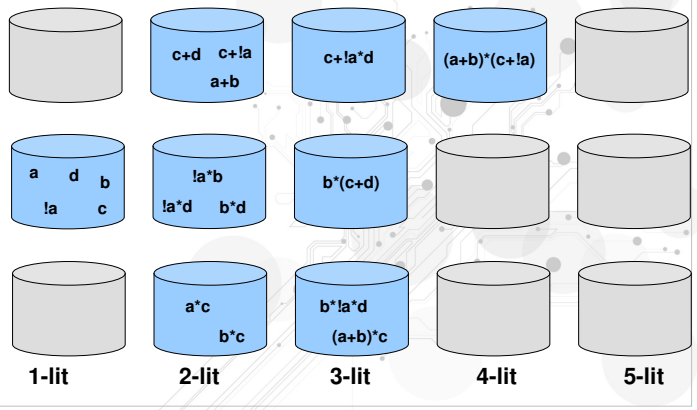
Fatoração – se2



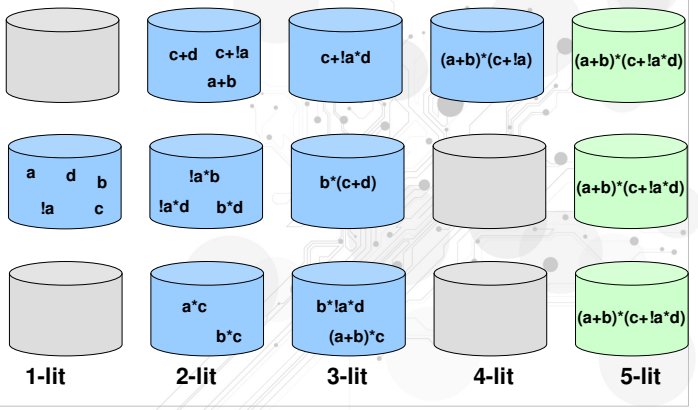
Fatoração – se3



Fatoração – se4



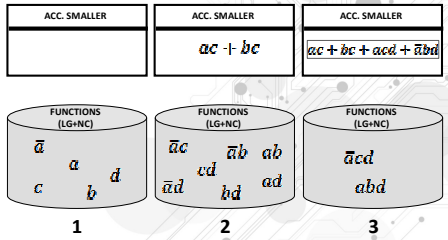
Fatoração – se5



Fatoração

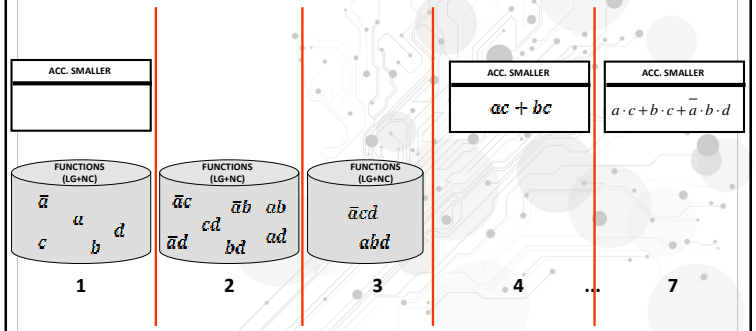
Composição Funcional

- Princípio aplicado a diferentes objetivos
- Neste caso, computo do MDC – Cadeia de decisão mínima



Composição Funcional

- Princípio aplicado a diferentes objetivos
- Neste caso, computo da SOP mínima



Composição Funcional

- Ordenamentos diferentes para SOP e MDC
  - **For MDC:**

$$f = \bar{a} \cdot \bar{b} \cdot \bar{d} + \bar{a} \cdot b \cdot \bar{c} + a \cdot \bar{d} \cdot \bar{e} + a \cdot c \cdot d + a \cdot \bar{d} \cdot e + a \cdot b \cdot c \quad \mathbf{3}$$

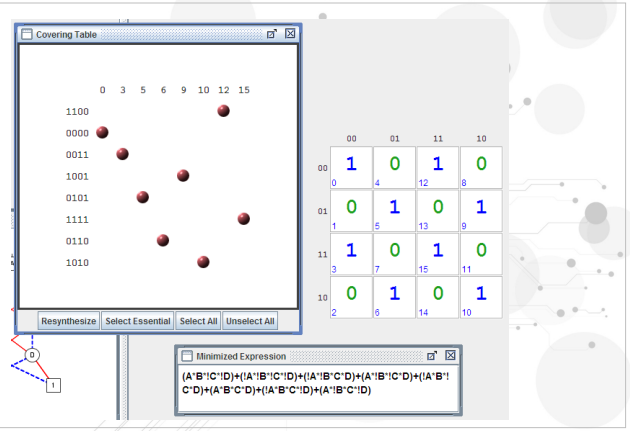
$$f = \bar{a} \cdot \bar{b} \cdot \bar{d} + \bar{a} \cdot b \cdot \bar{c} + a \cdot \bar{d} \cdot \bar{e} + a \cdot c \cdot d + b \cdot c \cdot \bar{d} \cdot e \quad \mathbf{4}$$

  - **For SOP**

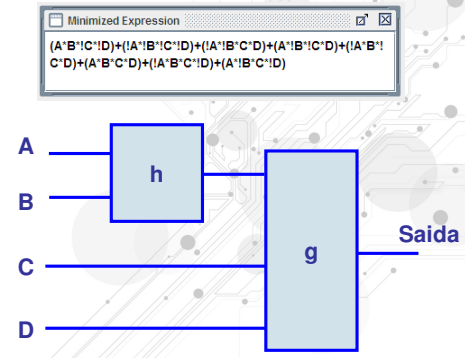
$$f = \bar{a} \cdot \bar{b} \cdot \bar{d} + \bar{a} \cdot b \cdot \bar{c} + a \cdot \bar{d} \cdot \bar{e} + a \cdot c \cdot d + b \cdot c \cdot \bar{d} \cdot e \quad \mathbf{16}$$

$$f = \bar{a} \cdot \bar{b} \cdot \bar{d} + \bar{a} \cdot b \cdot \bar{c} + a \cdot \bar{d} \cdot \bar{e} + a \cdot \bar{c} \cdot d + a \cdot \bar{d} \cdot e + a \cdot b \cdot c \quad \mathbf{18}$$

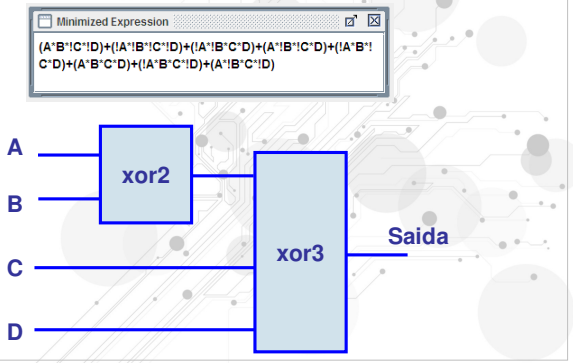
Decomposição disjunta



Decomposição disjunta

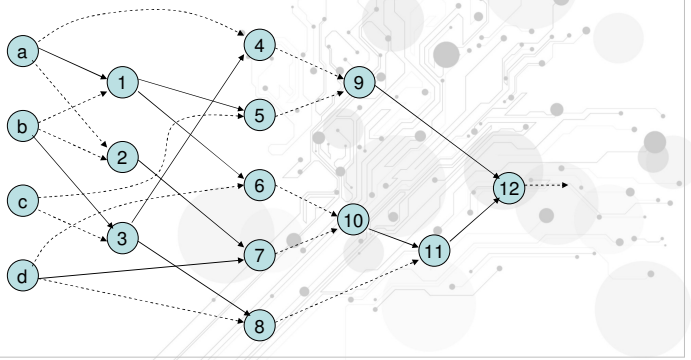


Decomposição disjunta

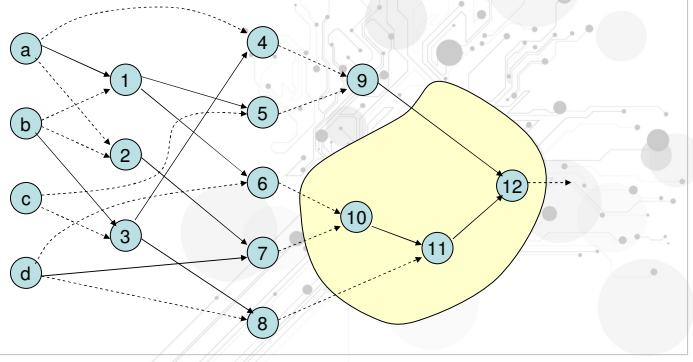


Cortes em AIGs

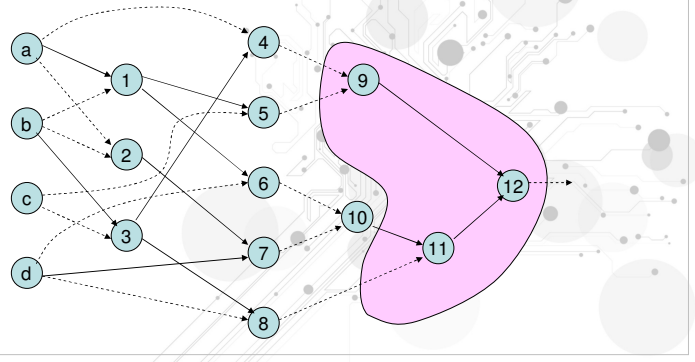
- Fazer cortes K



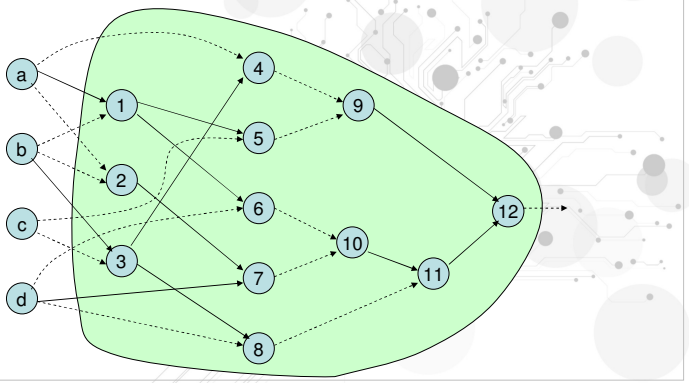
Cortes em AIGs



Cortes em AIGs

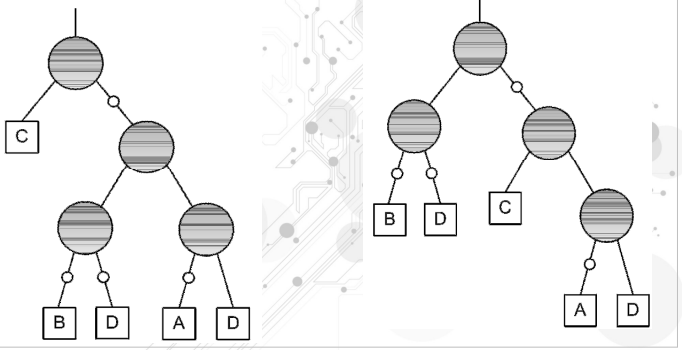


Cortes em AIGs

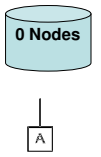


Reescrita de AIGs

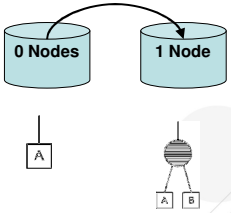
- Reescrever pequenas partes de um AIG
- Trocar por algo que se adapte melhor a otimização desejada



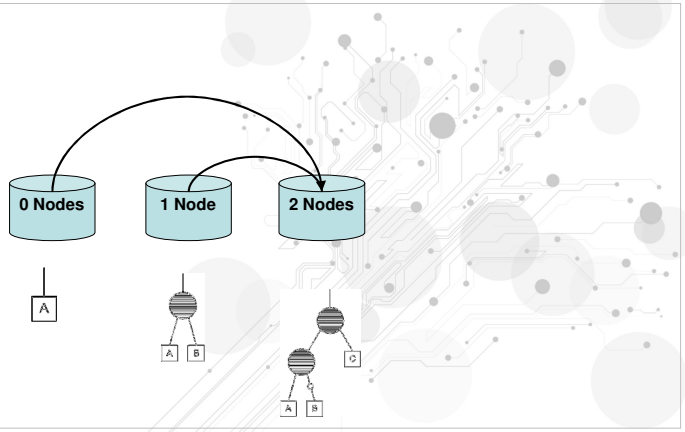
Reescrita de AIGs



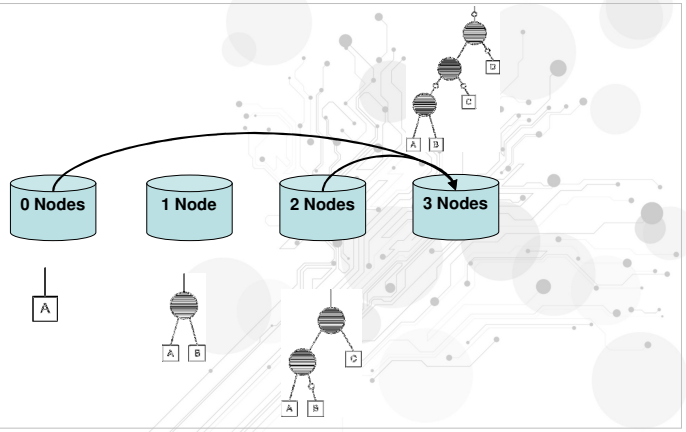
Reescrita de AIGs



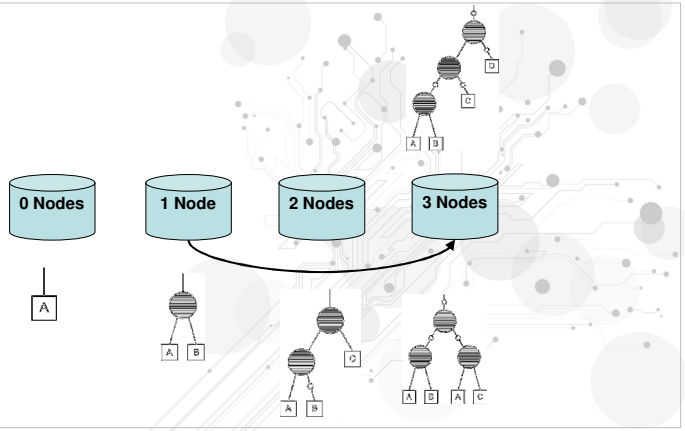
Reescrita de AIGs



Reescrita de AIGs



Reescrita de AIGs



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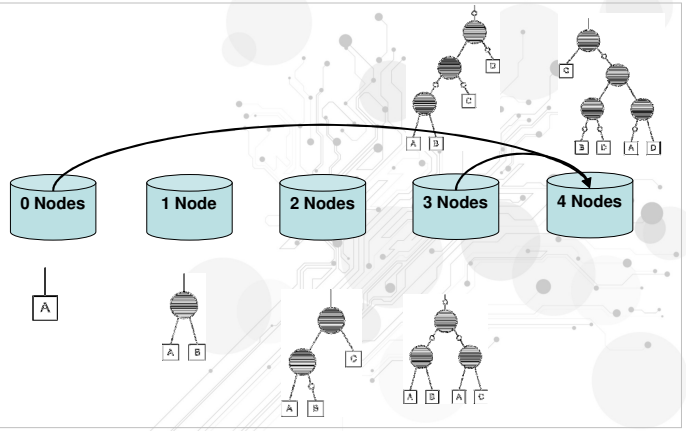
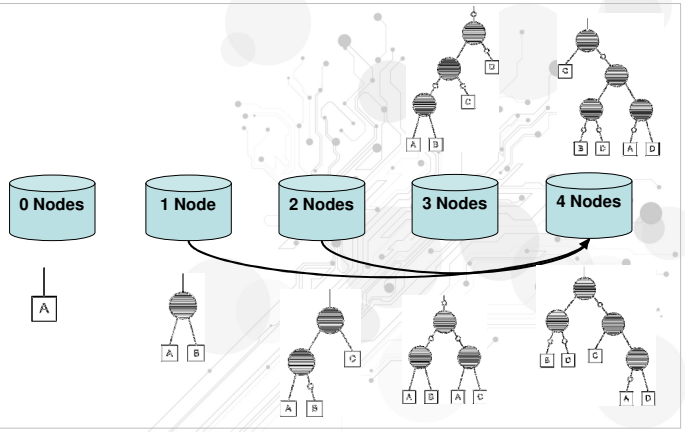
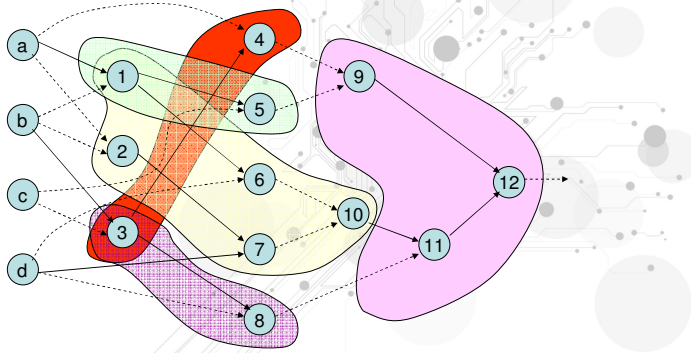


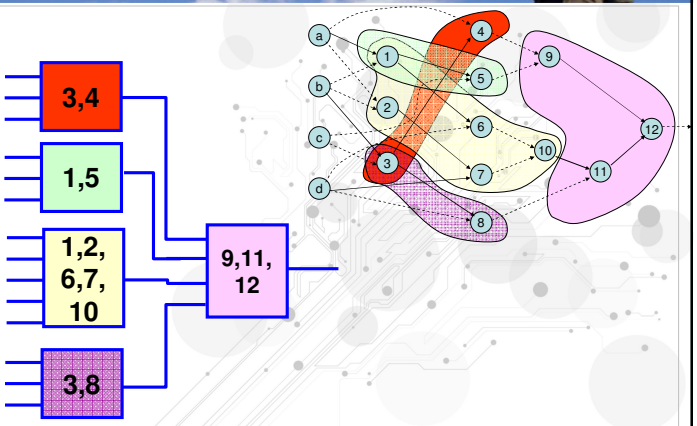
Reescrita de AIGs



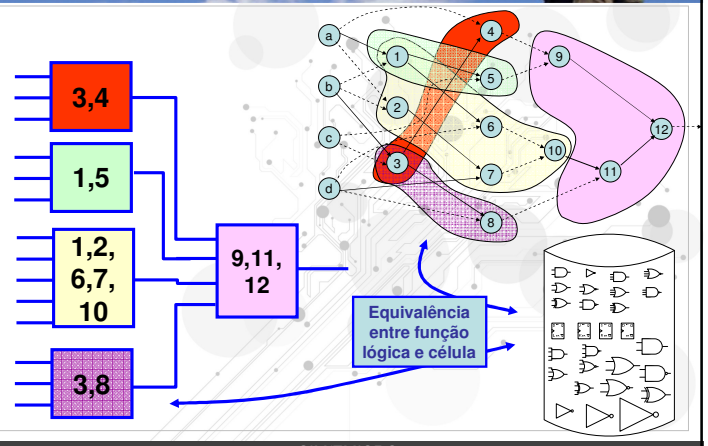
Cobertura de AIGs



Mapeamento tecnológico

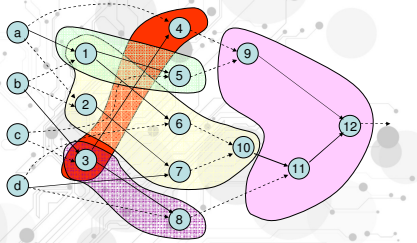


Matching



Matching

- !(!i4*!i5*i10*!i8) equivalente a célula a+b+c+!d
- Sob o assinalamento
  - i4 ↔ a
  - i5 ↔ b
  - i10 ↔ d
  - i8 ↔ c



É função da etapa de matching identificar esta equivalência

Síntese Lógica dentro de células

- Síntese lógica pode ser multi-objetivo
- Dentro das células conta o número de transistores em série e em paralelo

Eq#	Equation	L	S	P
(3)	$f = b \cdot (\overline{d} + c) + (\overline{a} + d + c) \cdot (a + \overline{b} \cdot \overline{c})$	9	3	5
(4)	$f = c \cdot (b + a) + \overline{c} \cdot (\overline{a} \cdot \overline{d} + (d + b) \cdot (\overline{b} + a))$	10	3	5
(5)	$f = (\overline{c} + b + a) \cdot (c + \overline{a} \cdot \overline{d} + (d + b) \cdot (\overline{b} + a))$	10	3	4
(6)	$f = b \cdot (\overline{d} + c + a) + \overline{b} \cdot (\overline{c} + a) \cdot (\overline{a} + d + c)$	10	3	6

Uma ferramenta mínima

- AIG
- Cortes
- Reescrita dos cortes

Conclusão

- Síntese lógica é uma área vasta
- Ficamos sem falar de coisas importantes
  - BDDs – Diagramas de Decisão Binária
  - Representação de funções com inteiros