EMICRO/SIM 2013
XV Escola de Microeletrônica Sul / 28° Simpósio Sul de Microeletrônica
Porto Alegre, 29 de abril a 3 de maio de 2013

Transistor MOS

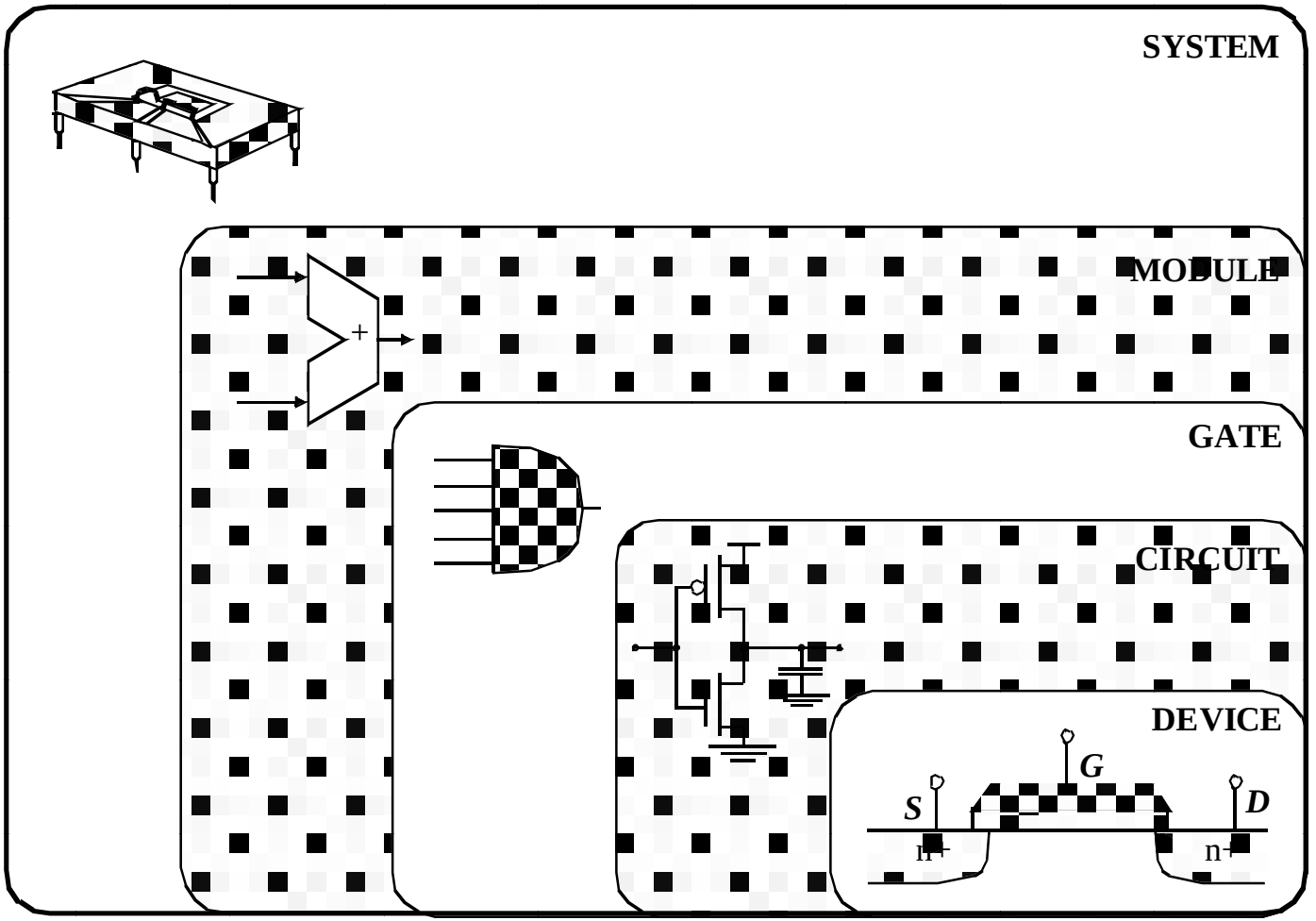
Gilson Wirth
Eng Elétrica - UFRGS

Organização
Promoção
Apoio

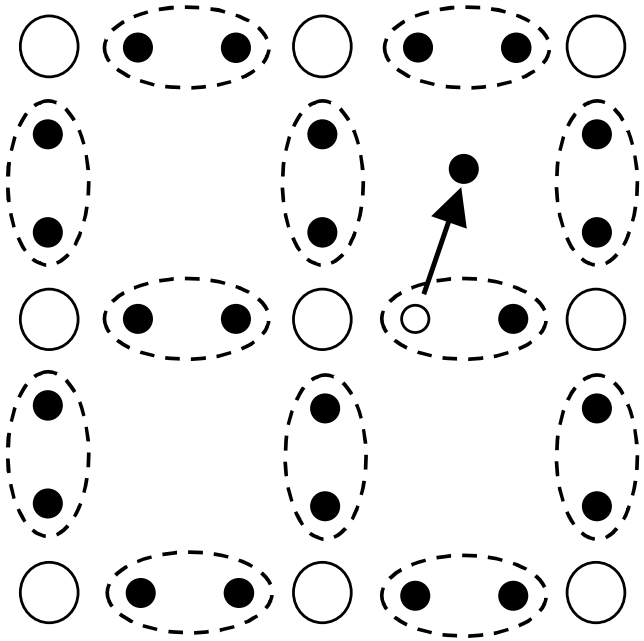
Conteúdo

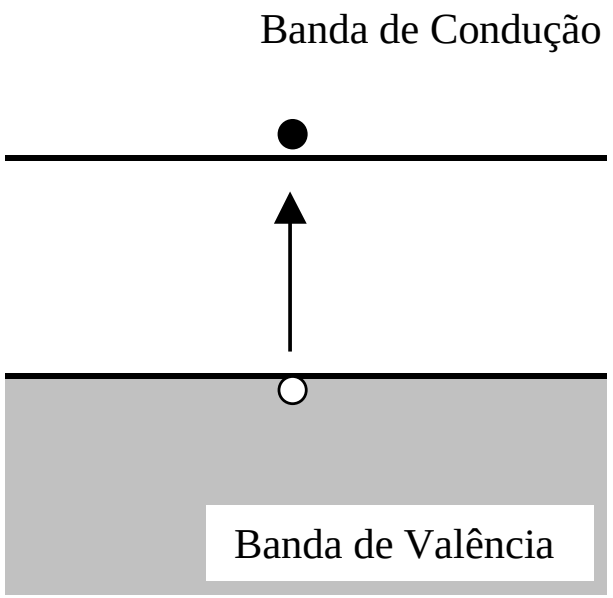
- Semicondutor
- Junção PN
- Capacitor MOS
- Transistor MOS
- Modelos Elétricos

Níveis de Abstração



Elétrons e Lacunas

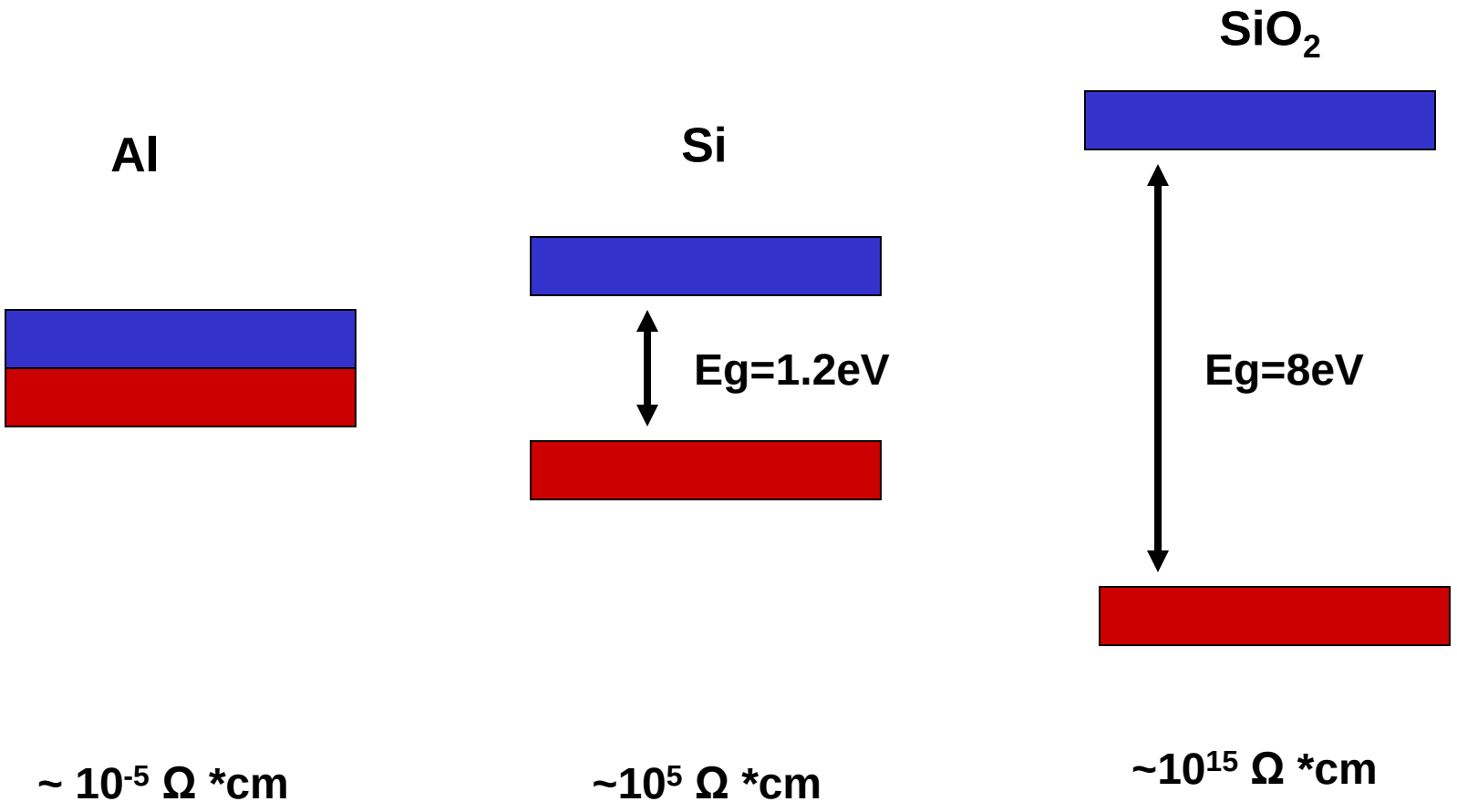




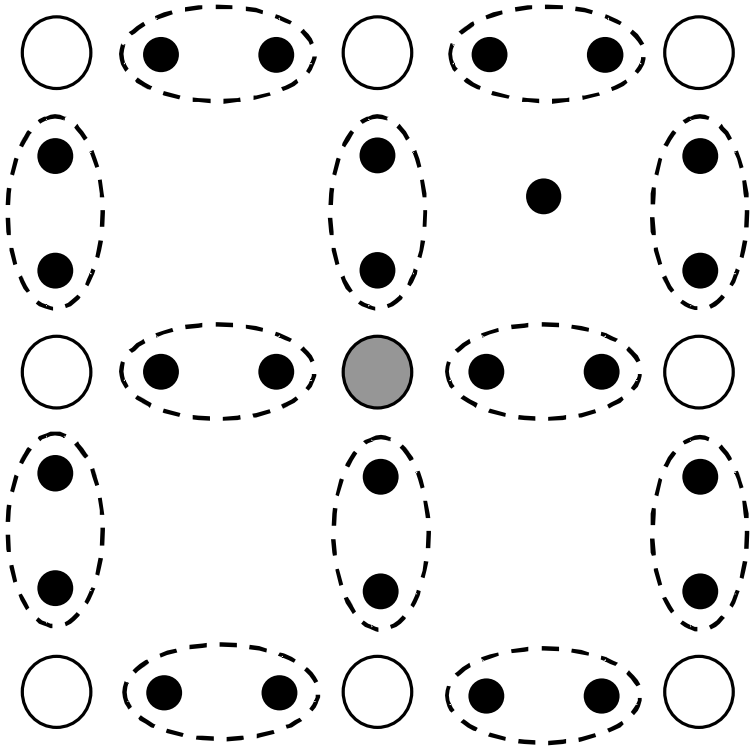
$$p.n = n_i^2$$

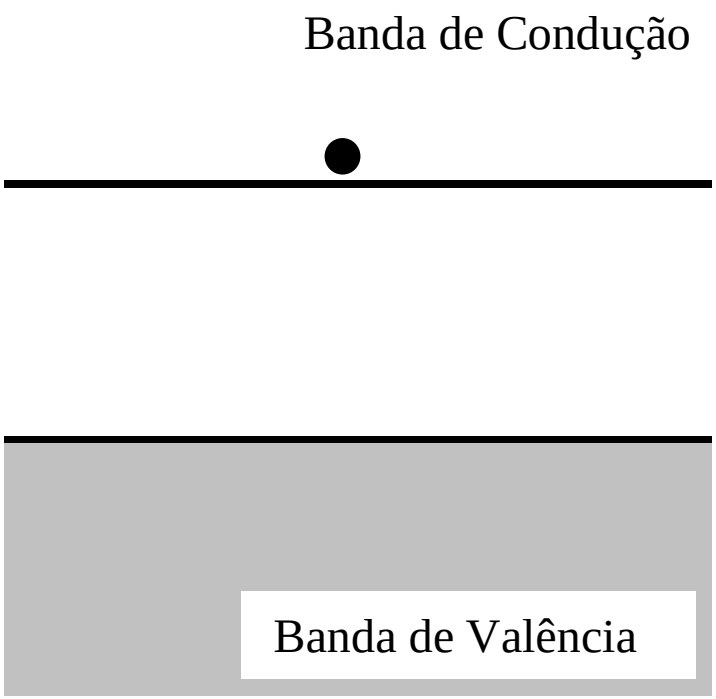
$$p_i = n_i = 1.45*10^{10}/cm^3 \text{ @ } 27\ C$$

Condutor, Semicondutor e Isolante

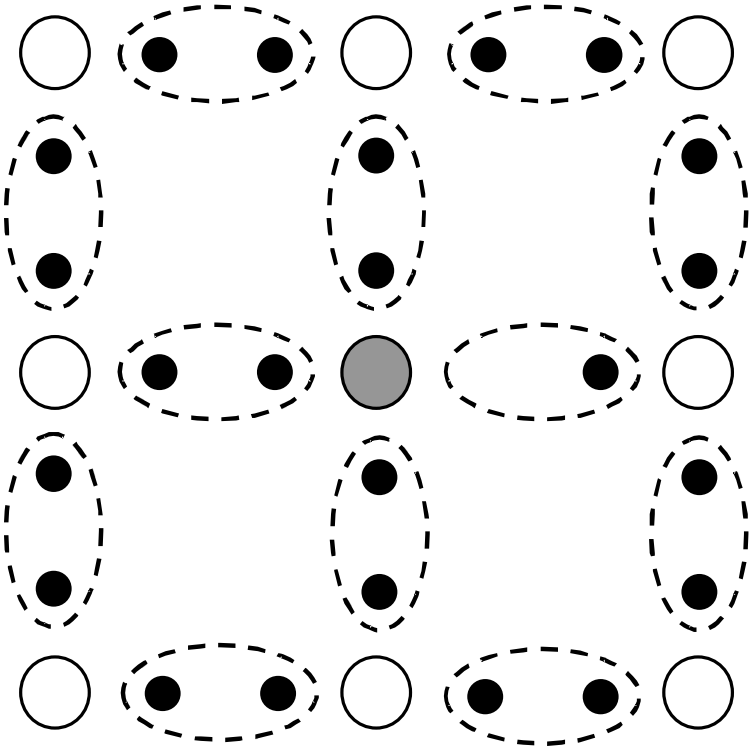


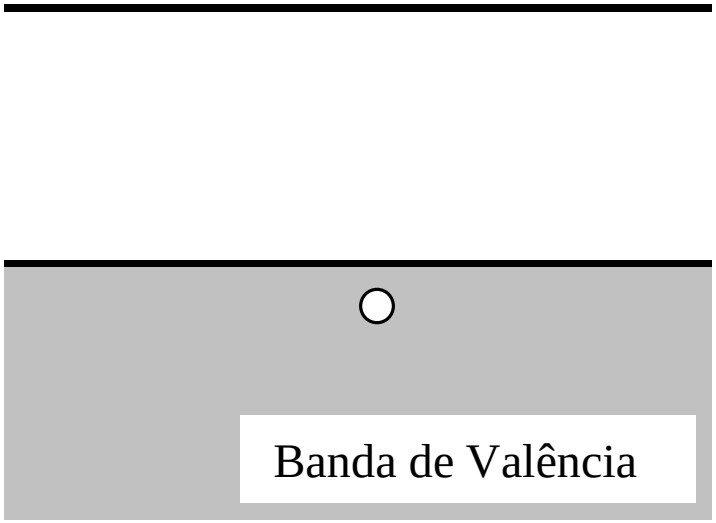
Material tipo n





Material tipo p





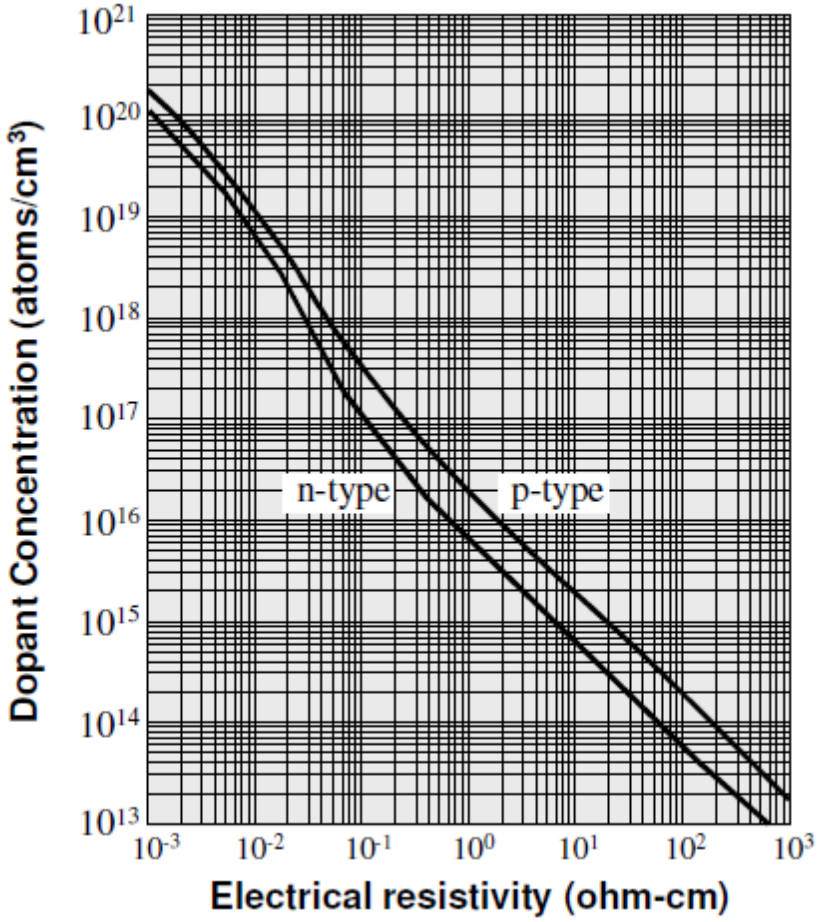
Elétrons e Lacunas: Condutividade do Material

Condutividade: $\sigma = q * (m_n*n + m_p*p)$ (S/cm)

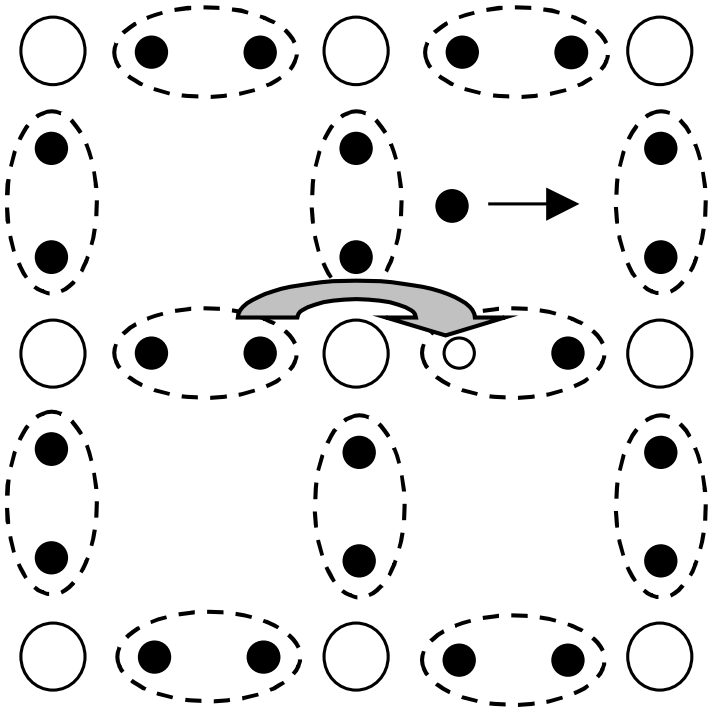
Resistividade: $\rho = 1/\sigma$ (Ω*cm)

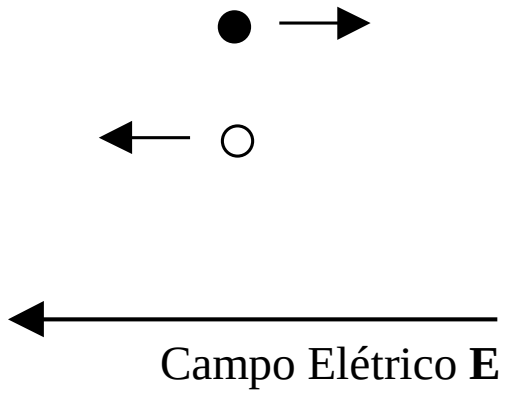
Onde
q = carga do elétron
m_n = mobilidade do elétron (~ 1500 cm^2/V para Si)
m_n = mobilidade da lacuna (~ 500 cm^2/V para Si)
n = concentração de elétrons
p = concentração de lacunas

Dopagem


Dopant Concentration (atoms/cm³)
10²¹
10²⁰
10¹⁹
10¹⁸
10¹⁷
10¹⁶
10¹⁵
10¹⁴
10¹³
n-type
p-type
10⁻³
10⁻²
10⁻¹
10⁰
10¹
10²
10³
Electrical resistivity (ohm-cm)

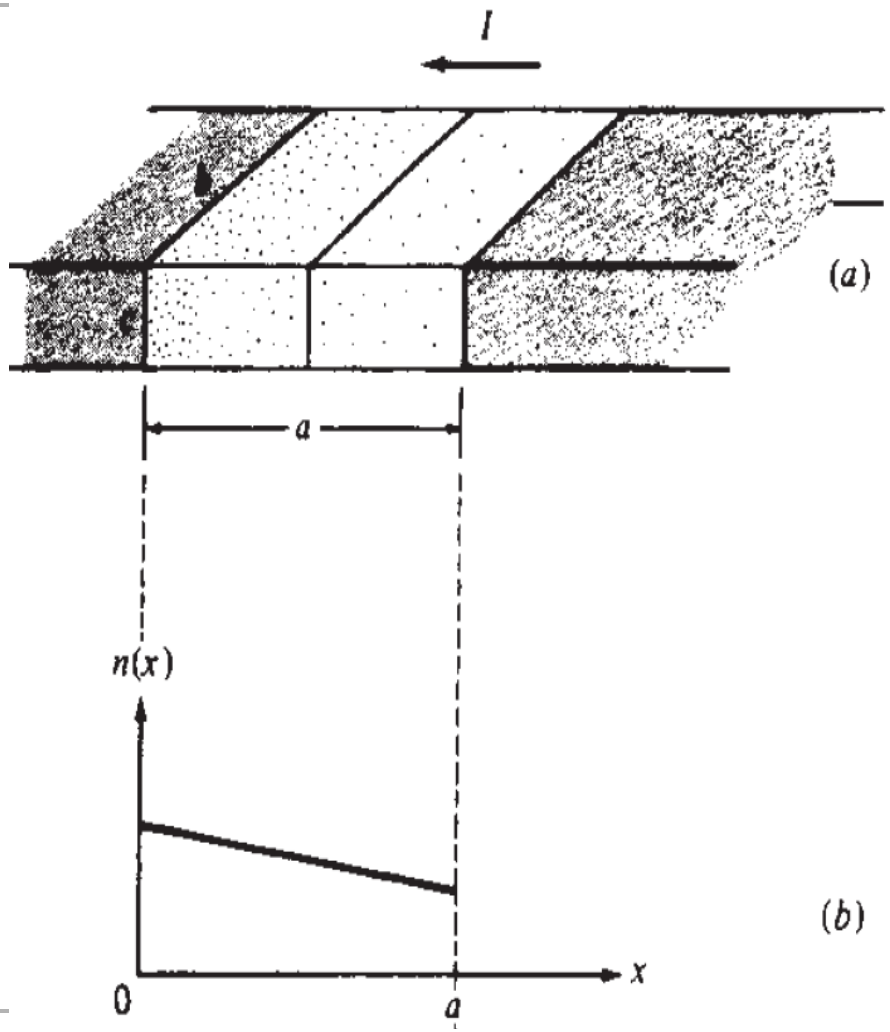
Elétrons e Lacunas, Campo Elétrico, Drift Current





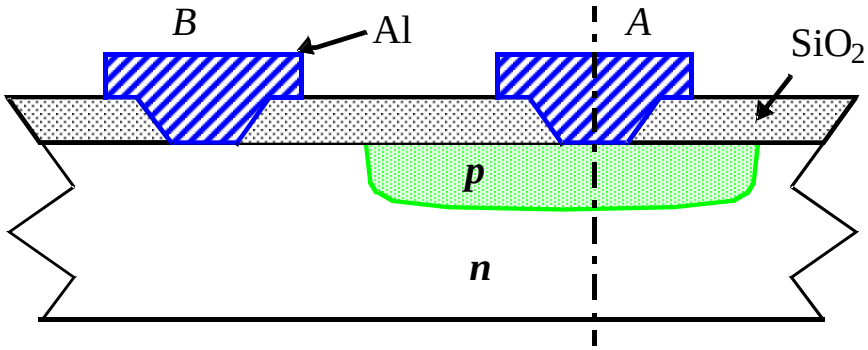
$F \approx E \quad \rightarrow \quad I \approx \mu * V$

Diffusion

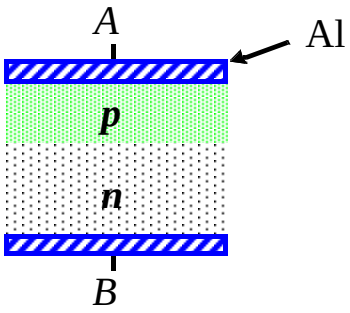


$$J_n = qD_n \frac{dn}{dx}$$

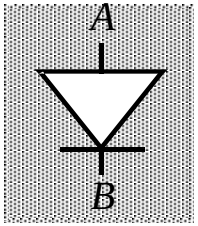
PN-Junction



Cross-section of *pn*-junction in an IC process

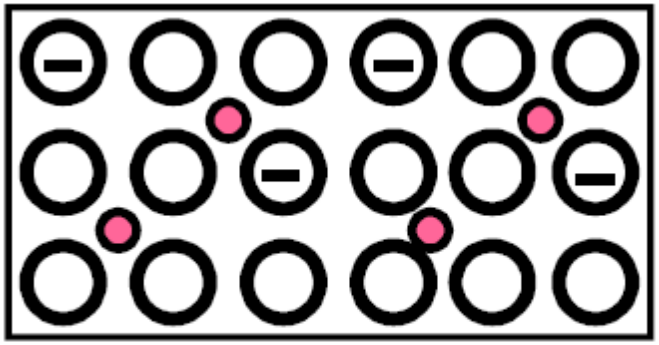


One-dimensional representation

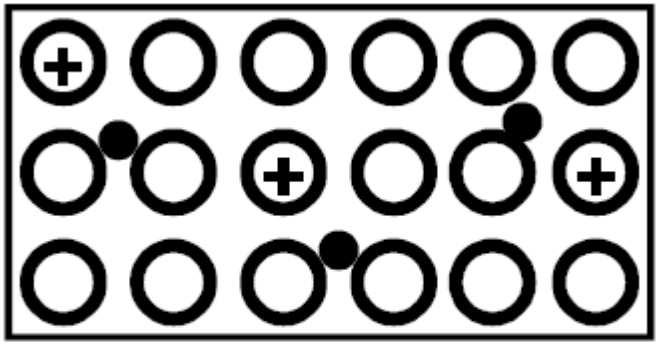


diode symbol

PN-Junction

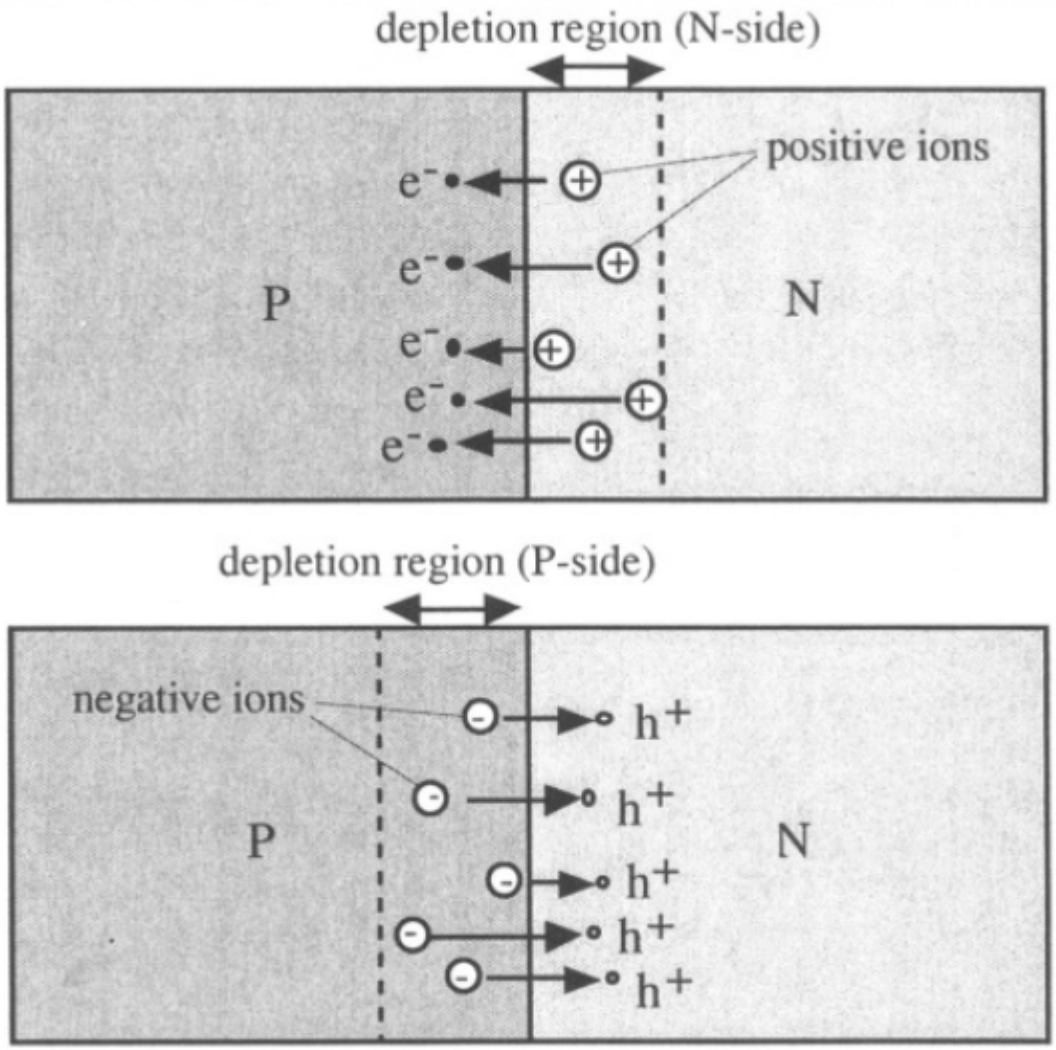


P-type material

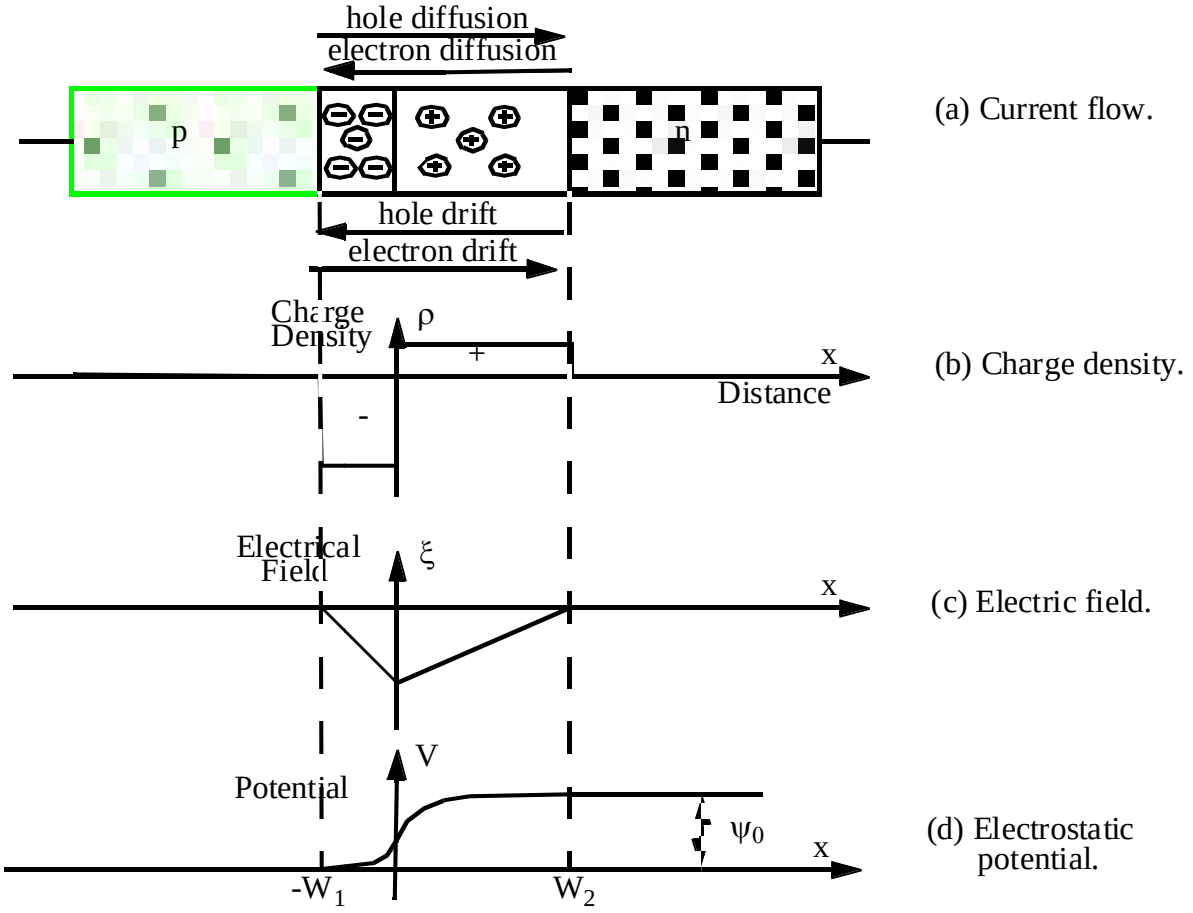


N-type material

Creation of Depletion Regions in Unbiased Junction



Diode



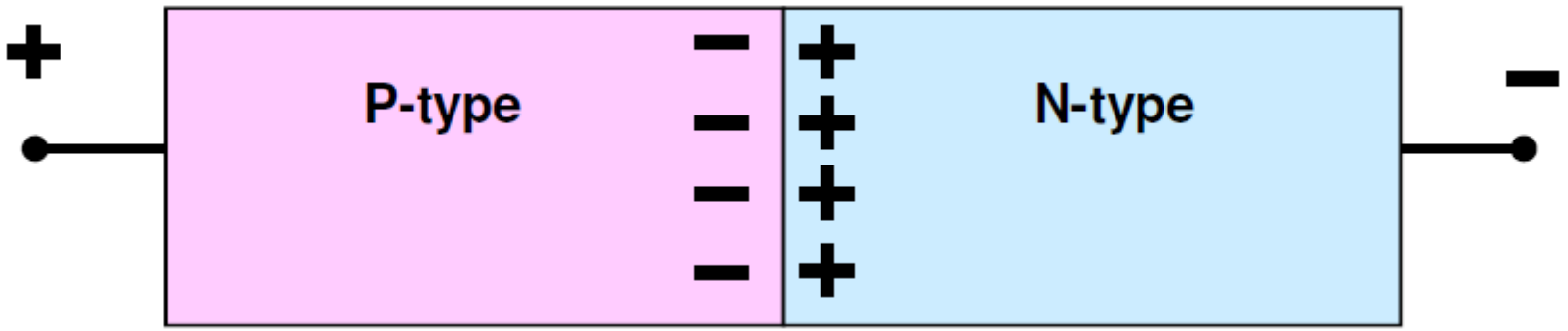
(a) Current flow.

(b) Charge density.

(c) Electric field.

(d) Electrostatic potential.

PN-Junction: Forward Bias



Diode: Forward Bias

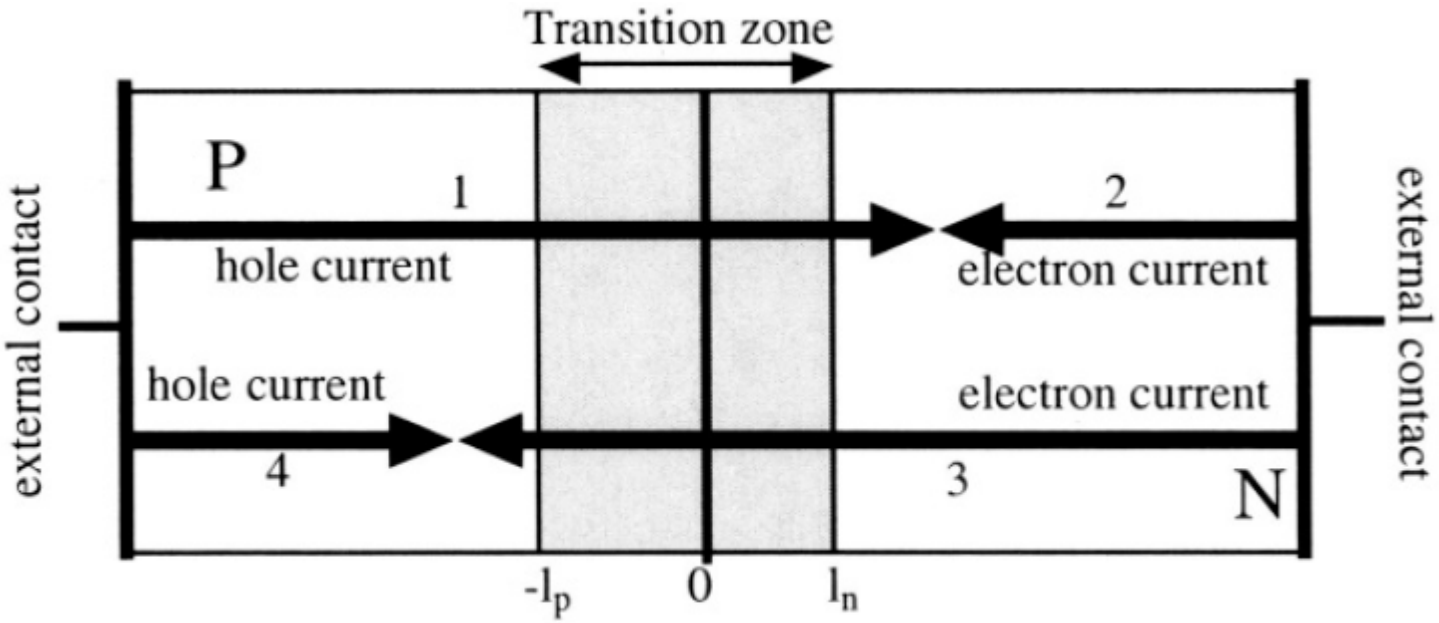
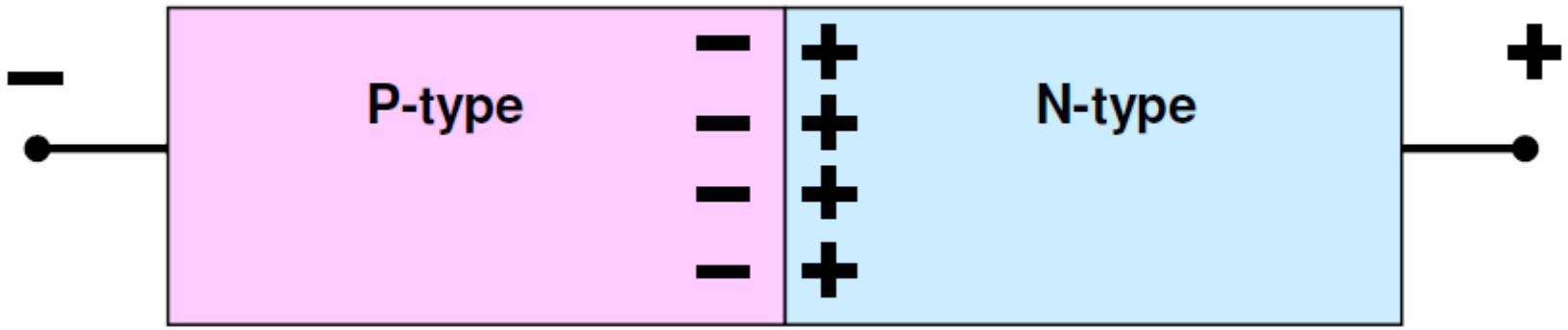


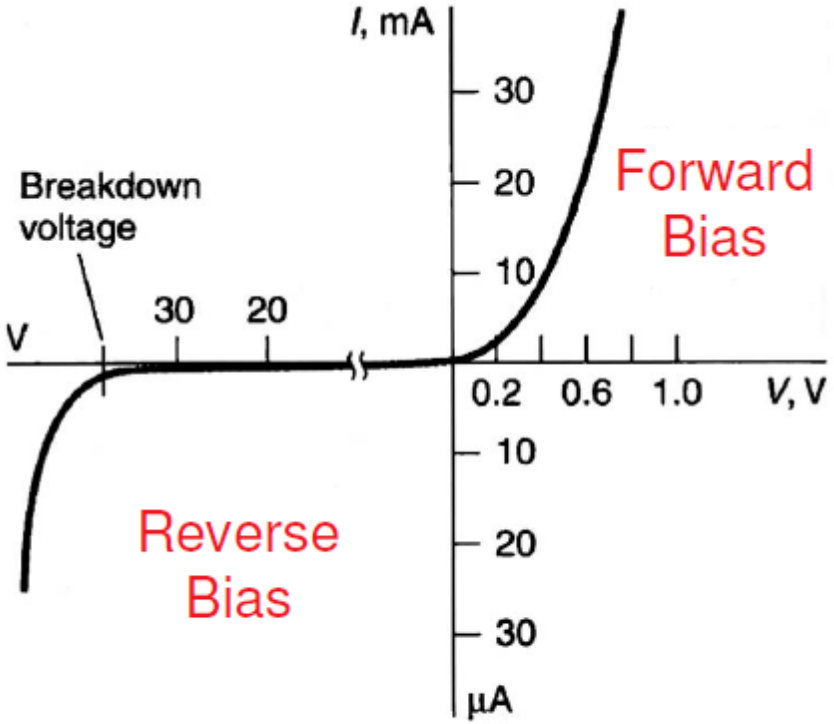
Figure 4.9: Forward-biased PN junction; 1: holes injected from the P-type region into the N-type region; 2: electrons recombining with the holes injected in the N-type region; 3: electrons injected from the N-type region into the P-type region; 4: holes recombining with the electrons injected in the N-type region.

PN-Junction: Reverse Bias



PN-Junction: I x V

$$I = I_s\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$



Forward bias: Current exponentially increases.

Reverse bias: Low-leakage current equal to ~0.

Rectifying pn junction: Passes current in only one direction!

DC (Quasi Static, Large Signal) Models

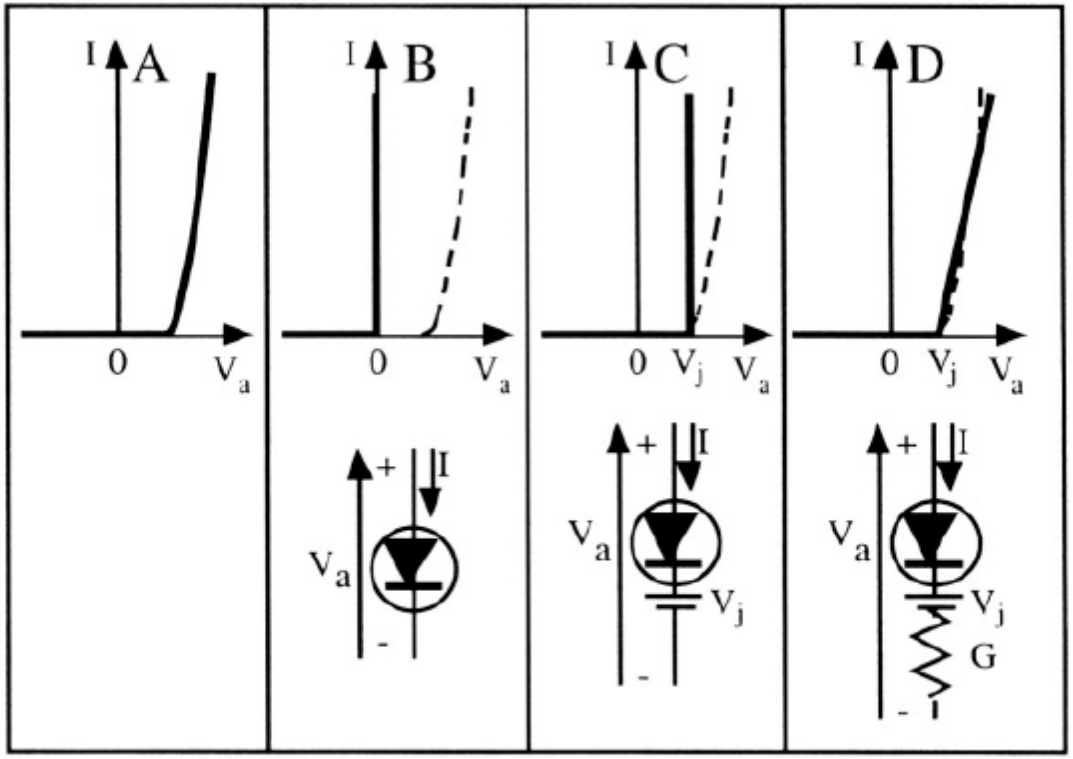
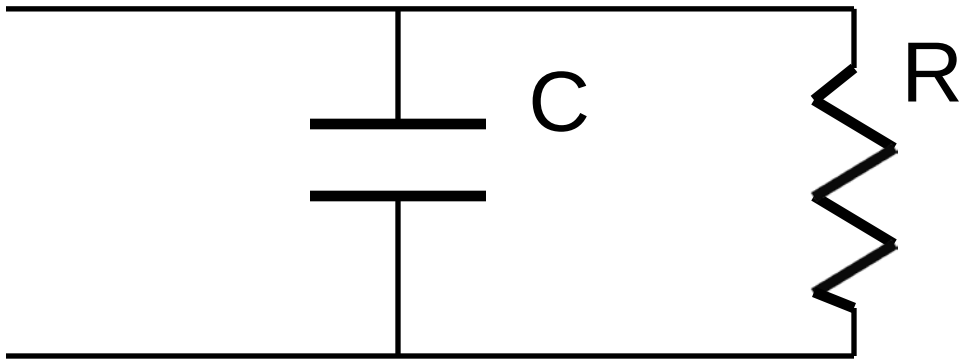
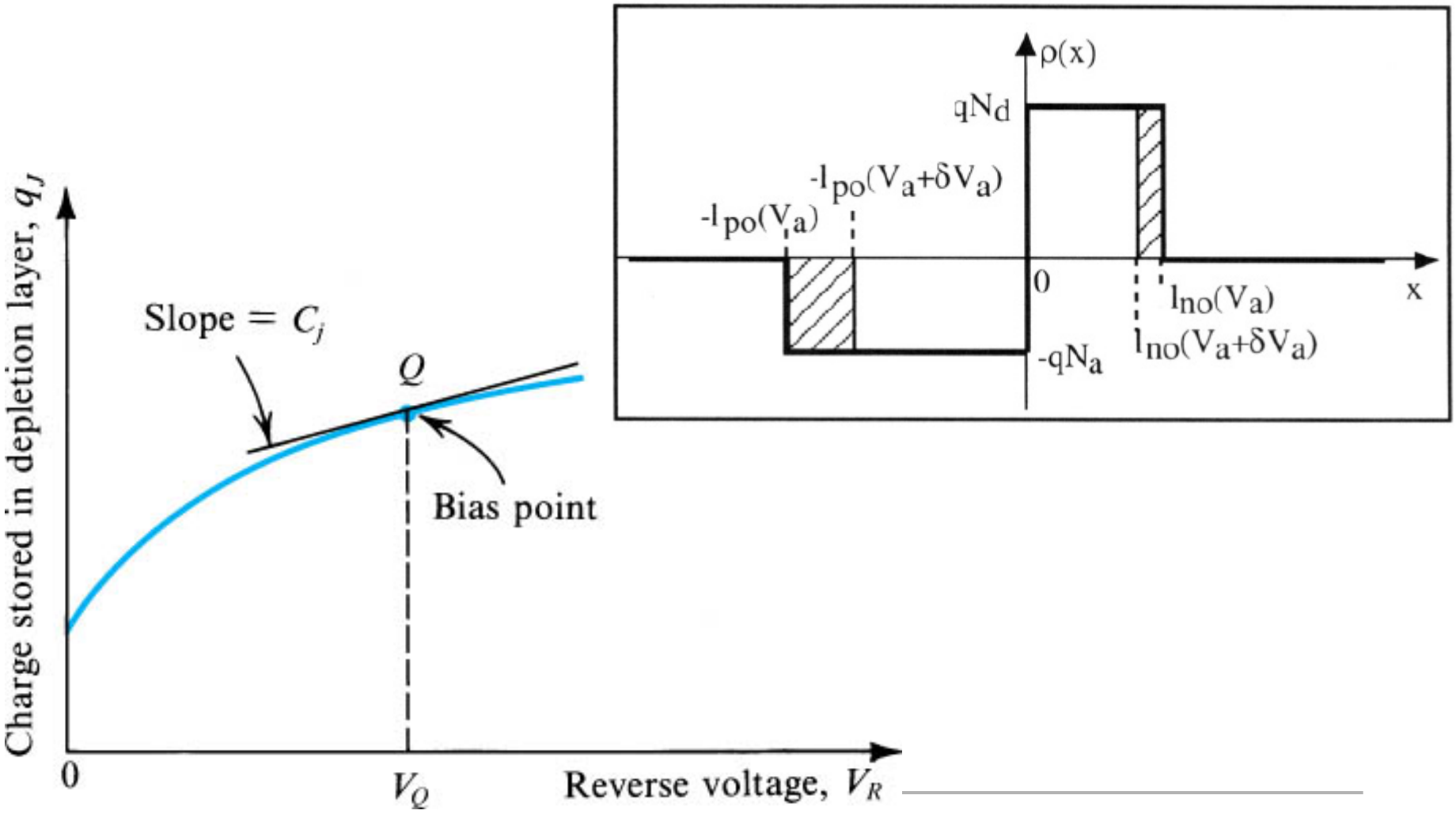


Figure 4.19: A: actual I-V characteristics, B: idealized diode, C: idealized diode + voltage source, D: idealized diode + voltage source + conductance.

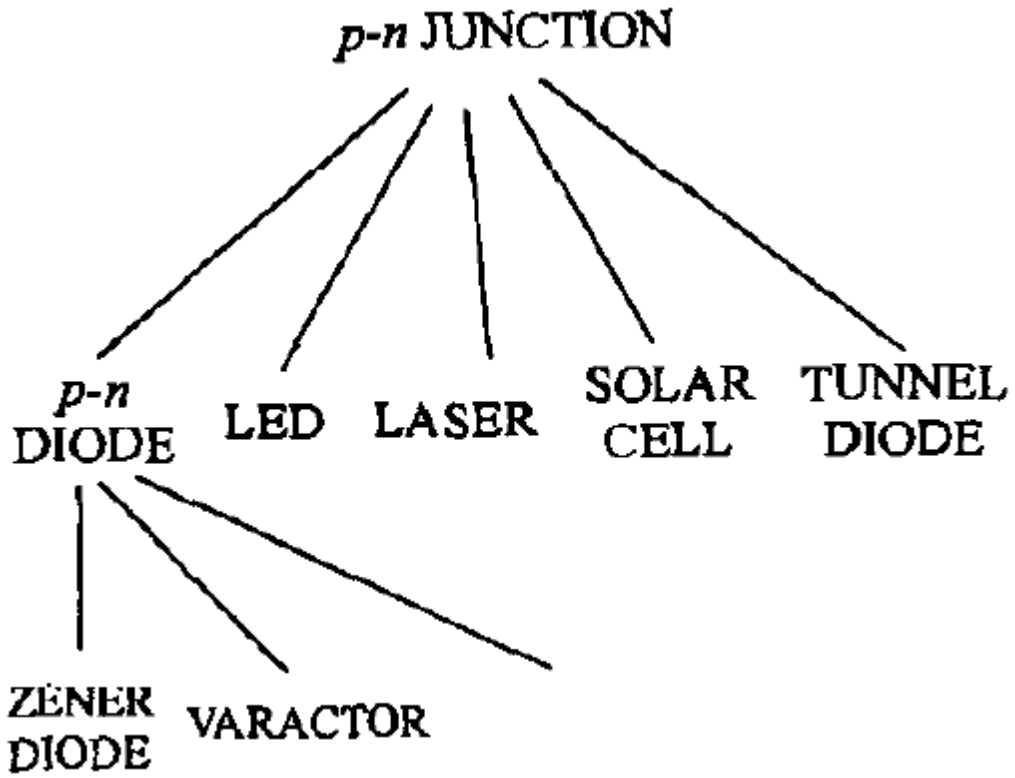
AC (Small Signal, High-Frequency) Model



Diode: Junction Capacitance

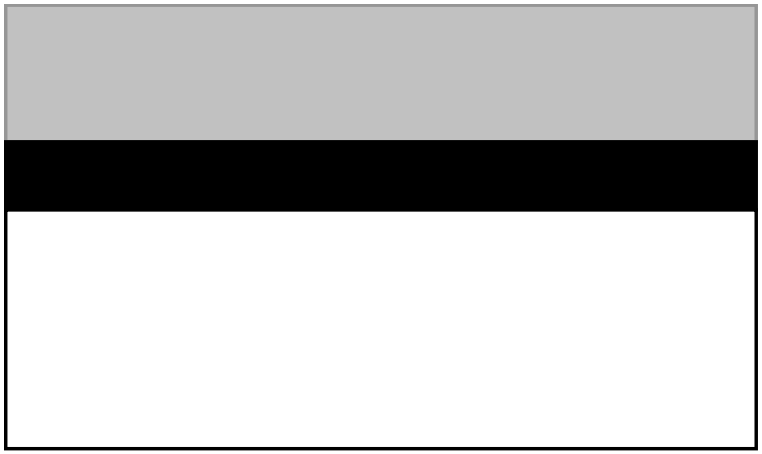


pn - Junction


p-n JUNCTION
p-n DIODE
LED
LASER
SOLAR CELL
TUNNEL DIODE
ZENER DIODE
VARACTOR

Capacitor MOS

Capacitor MOS

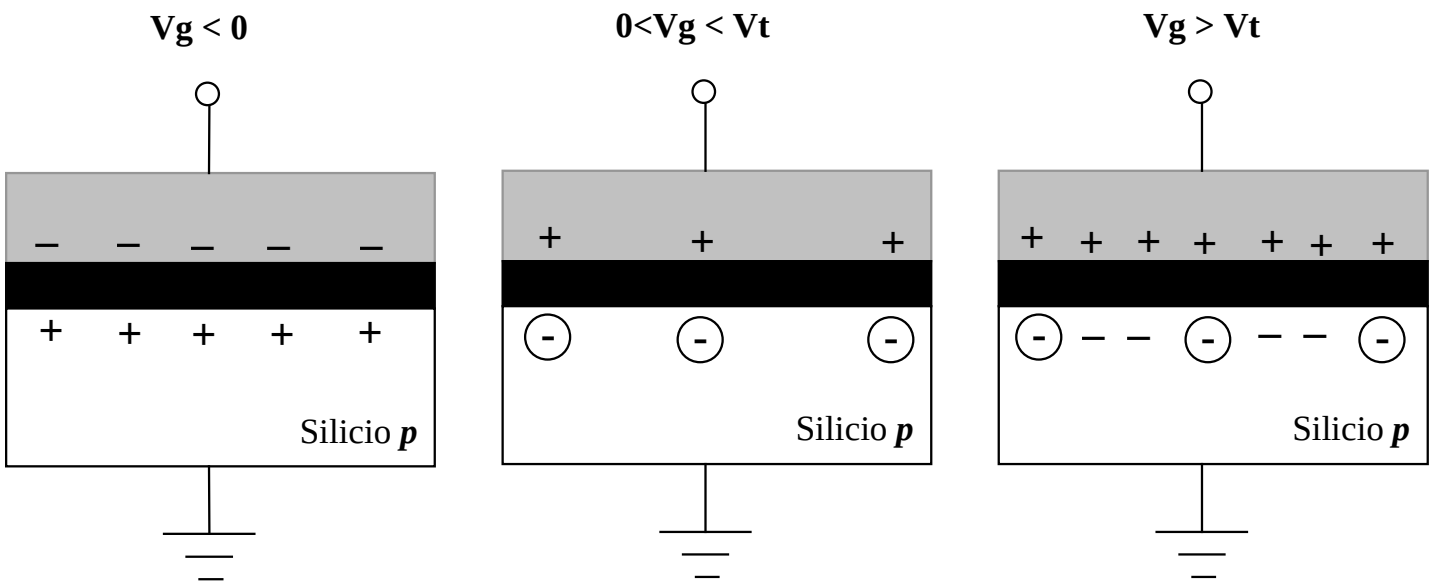


Porta de Poly ou Metal

Isolante (SiO2)

Substrato (Silício-*p*)

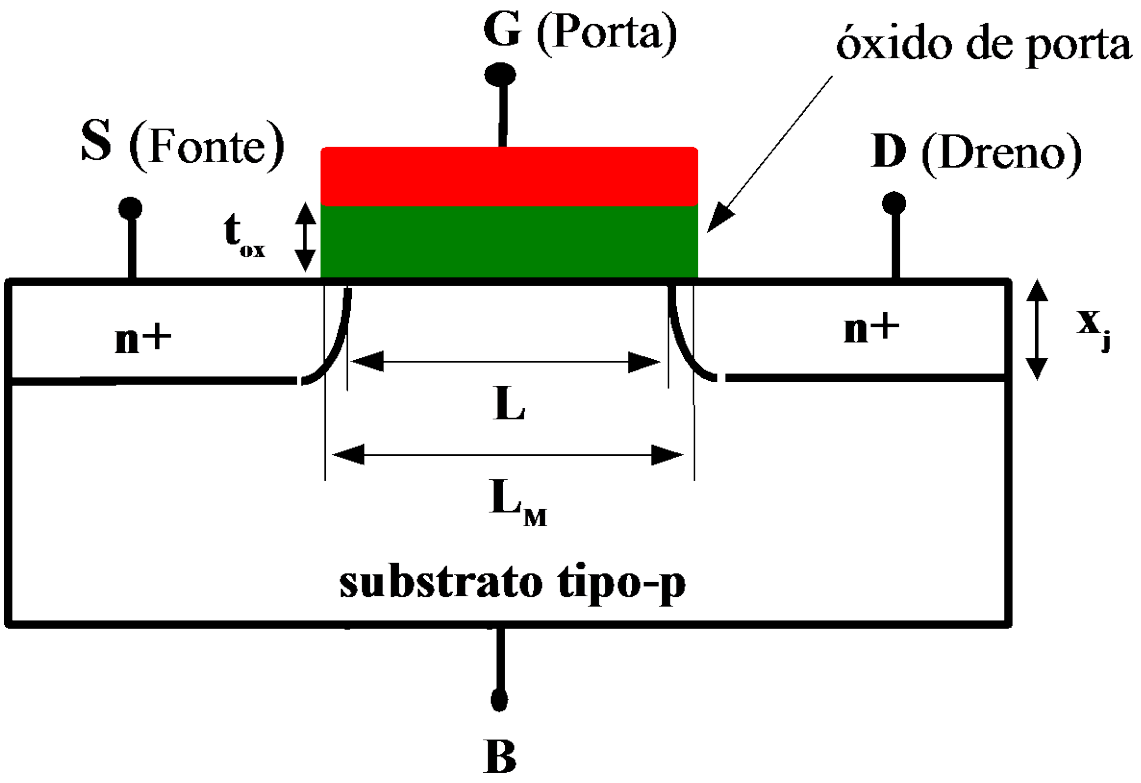
Capacitor MOS

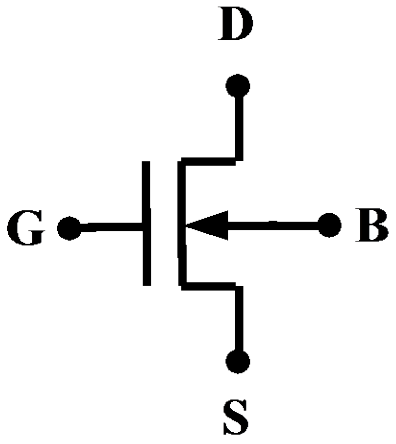


Legenda: (-) Aceitador Ionizado - Elétron Livre + Lacuna (móvel)

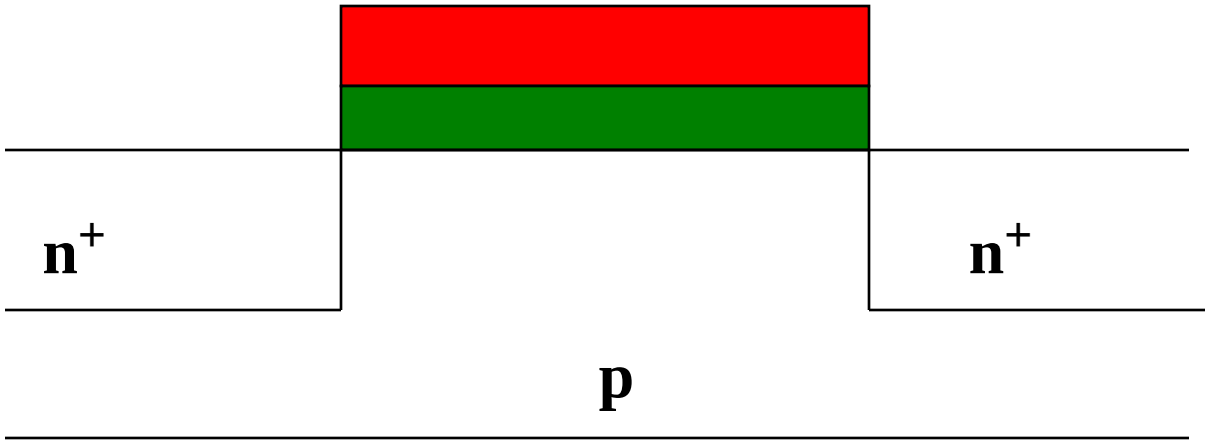
MOSFET

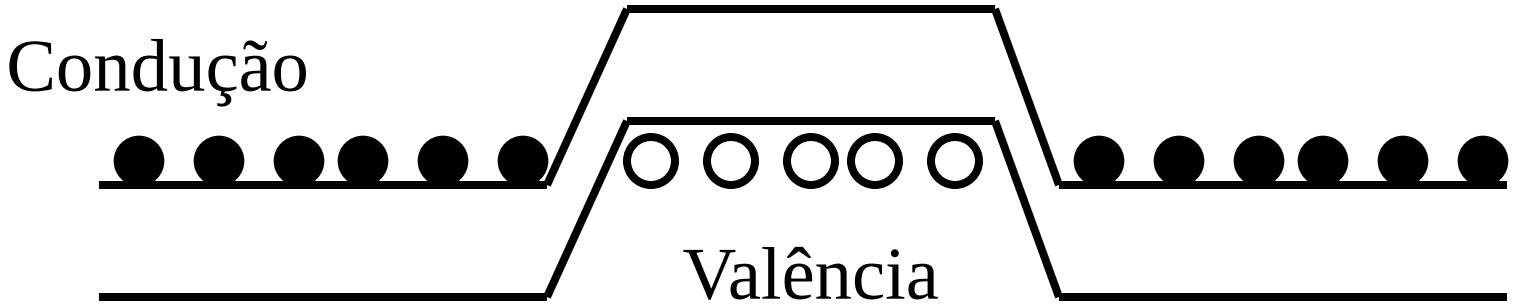
MOSFET


G (Porta)
óxido de porta
S (Fonte)
D (Dreno)
t_{ox}
n+
n+
x_j
L
L_M
substrato tipo-p
B

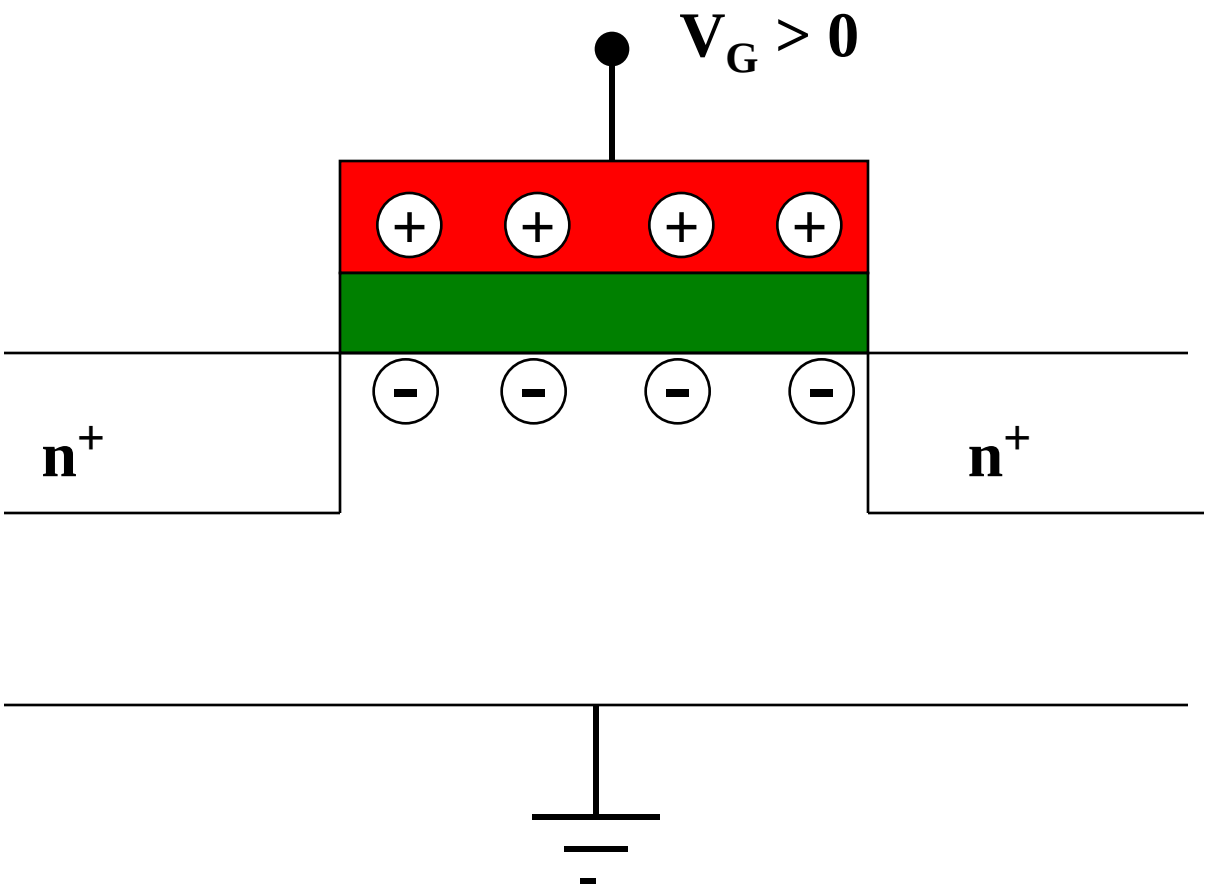

D
G
B
S

MOSFET

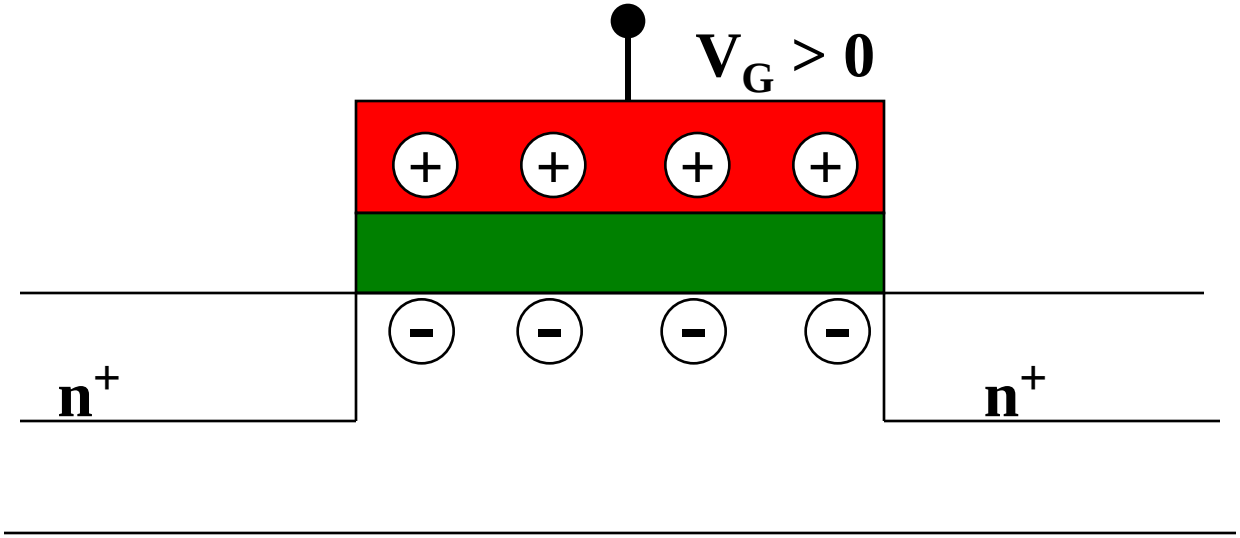


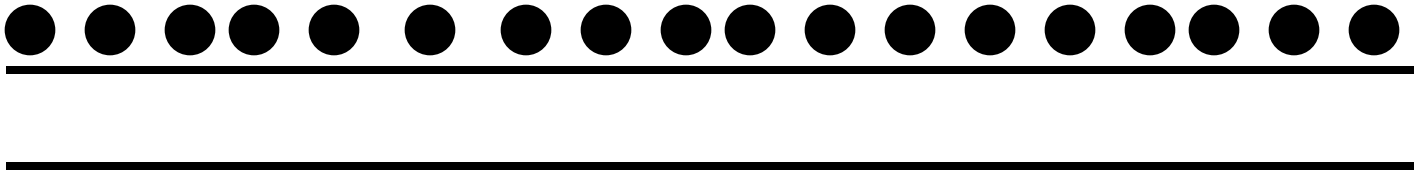


MOSFET

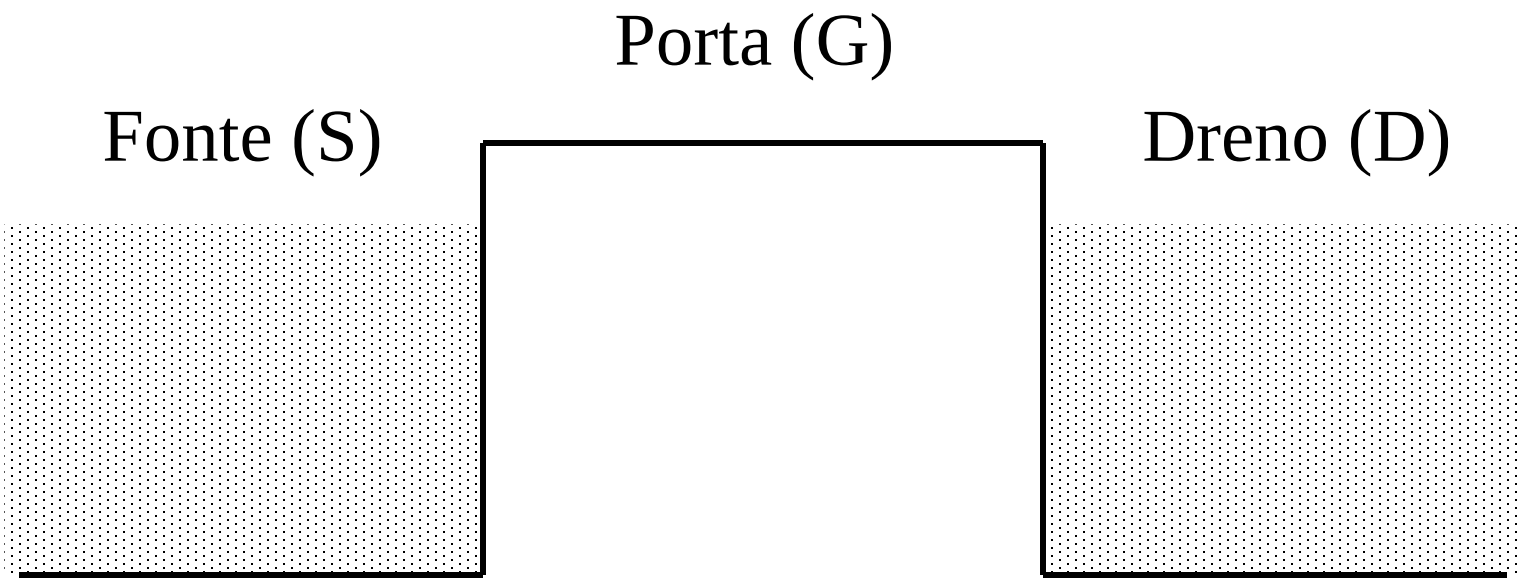


MOSFET



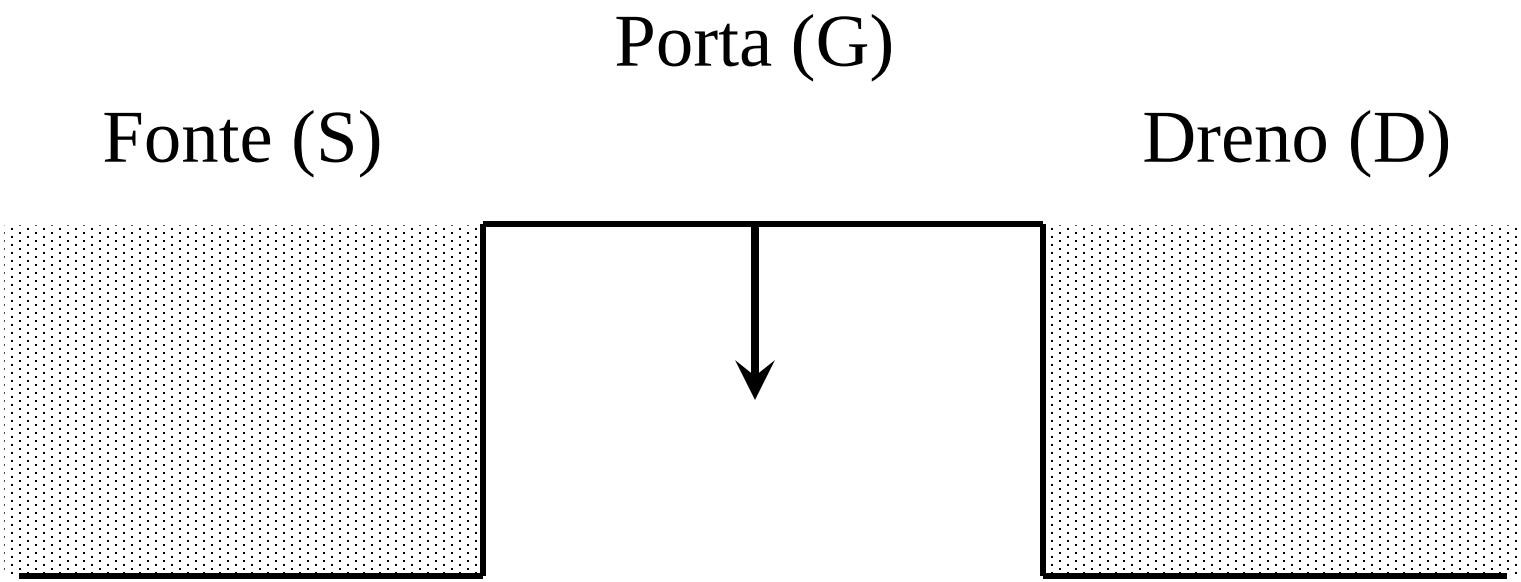


MOSFET



$V_S = 0$ $V_G = 0$ $V_D = 0$

MOSFET



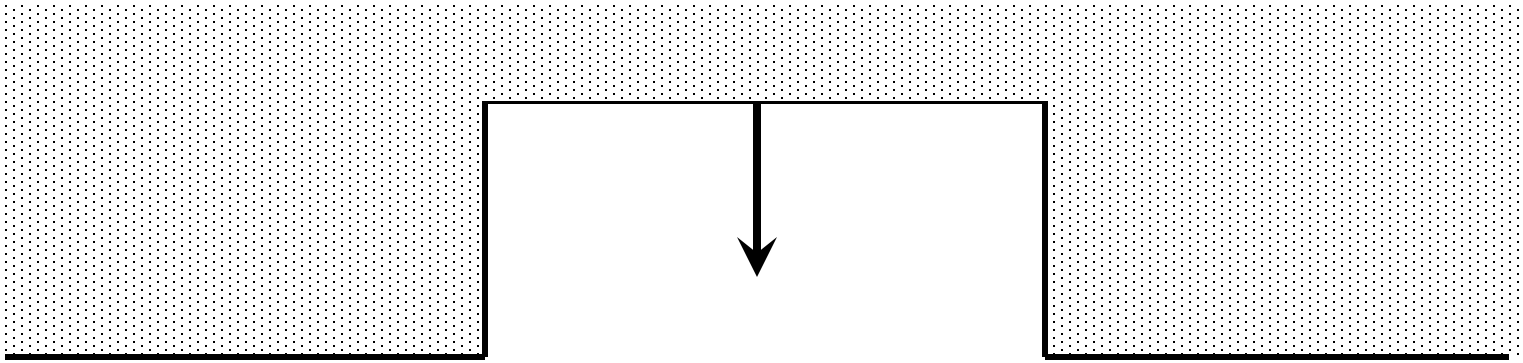
$V_S = 0$ $V_G = V_T$ $V_D = 0$

MOSFET

Porta (G)

Fonte (S)

Dreno (D)

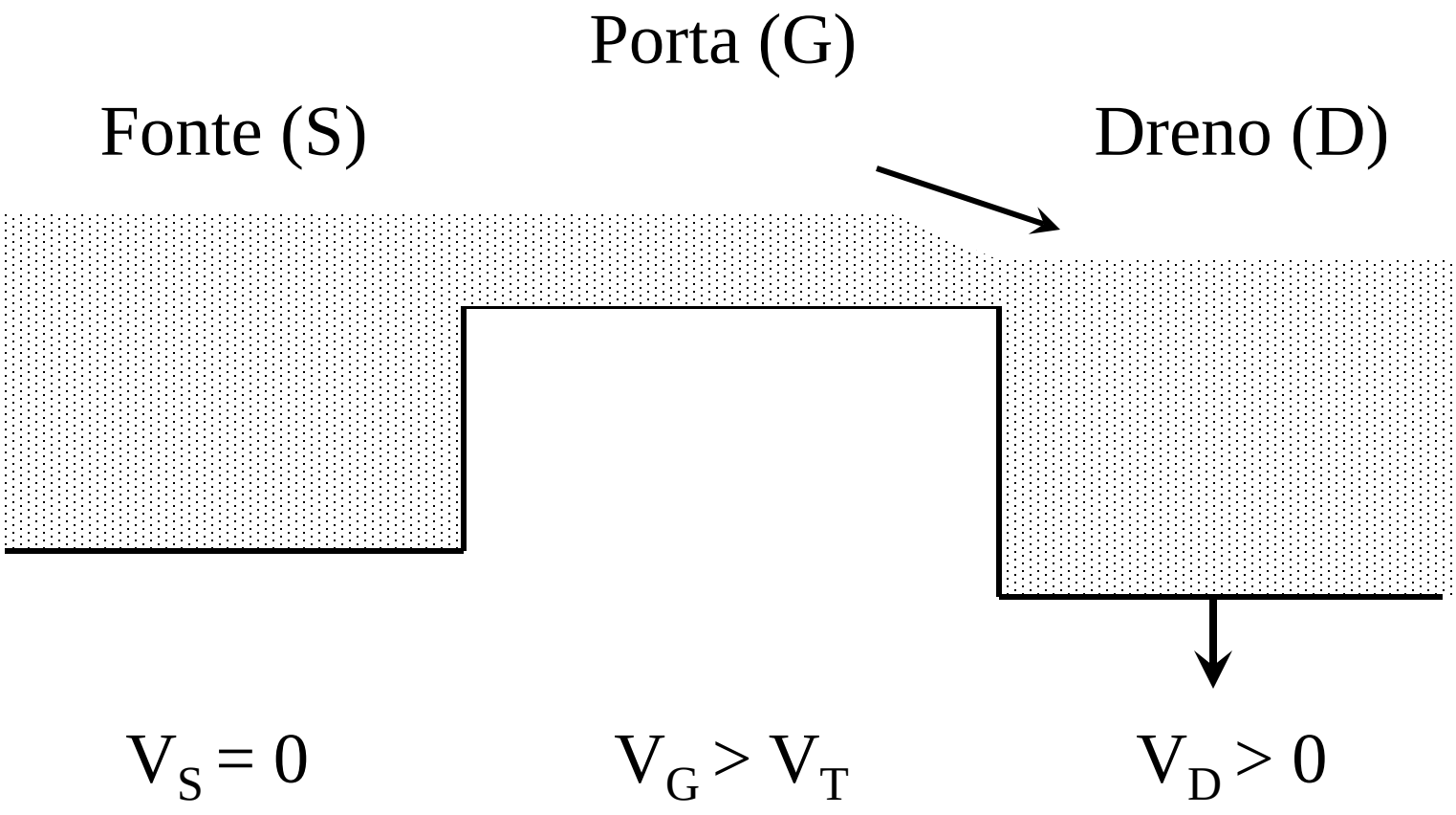


$V_S = 0$

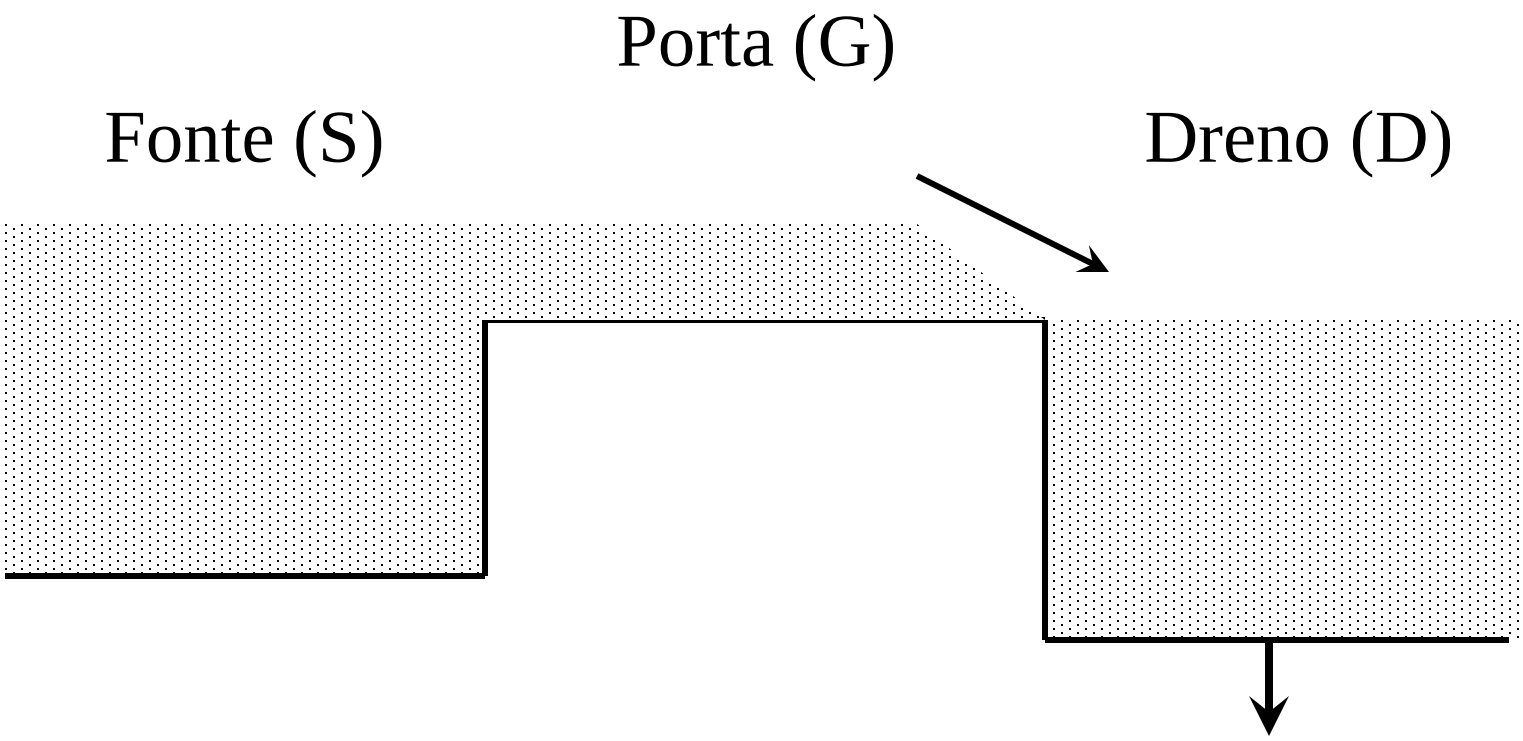
$V_G > V_T$

$V_D = 0$

MOSFET

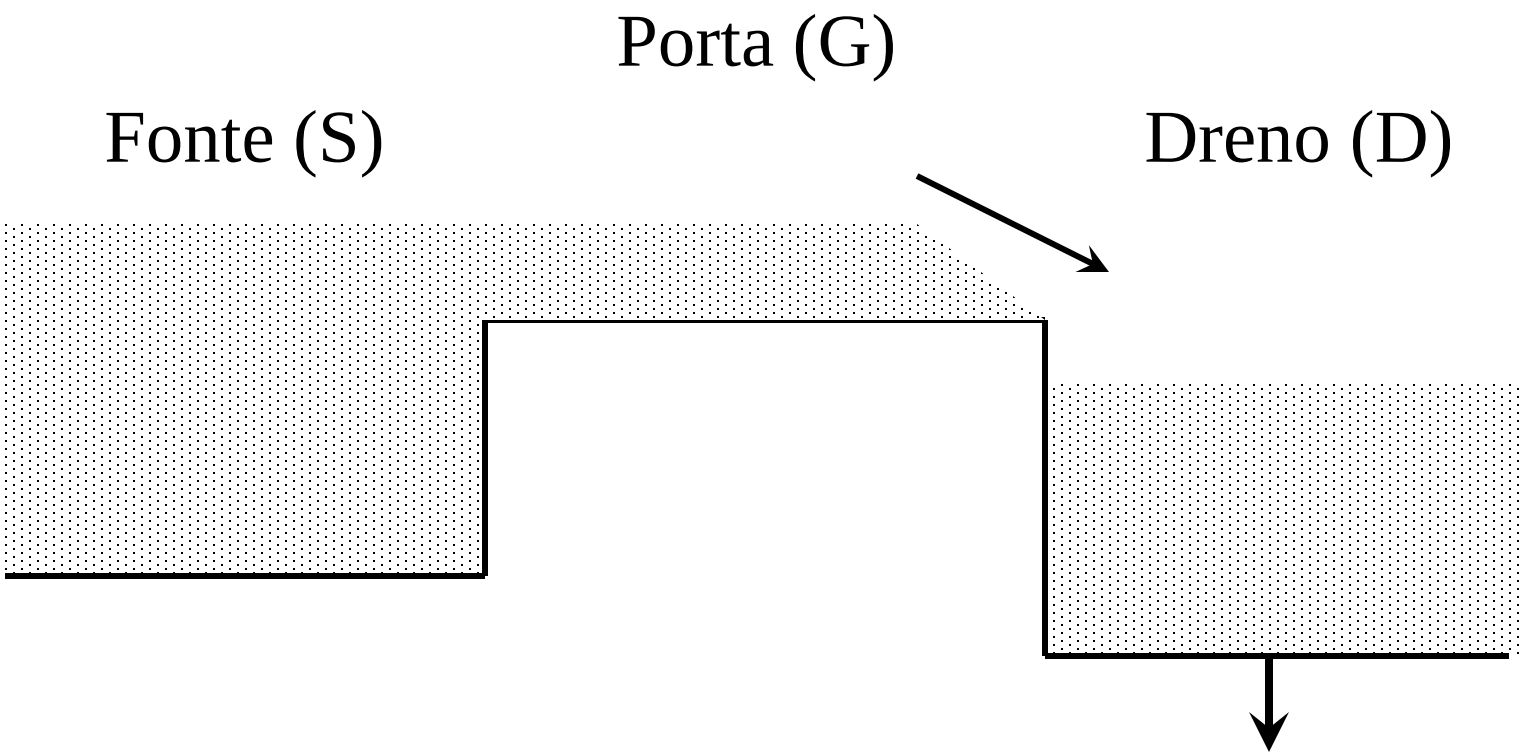


MOSFET

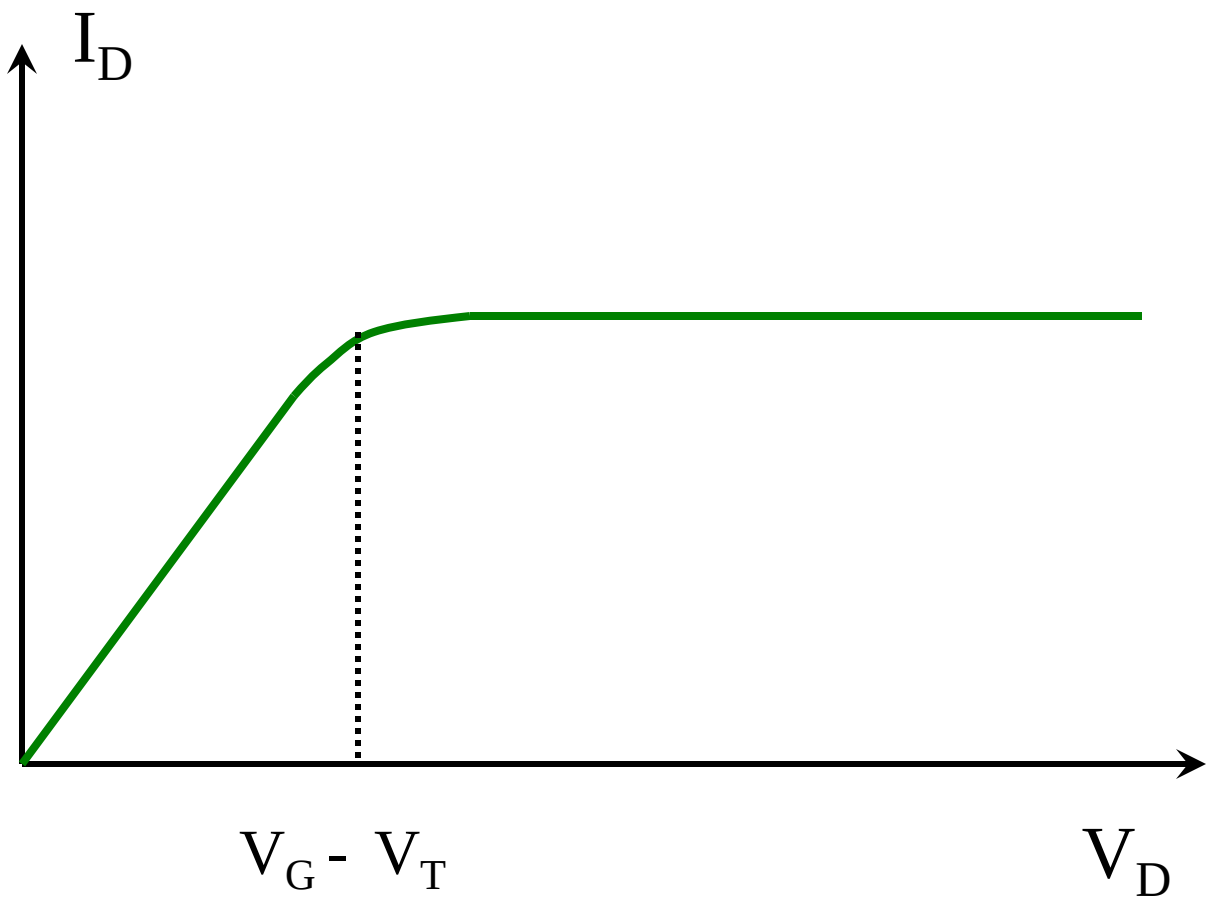


$V_S = 0$ $V_G > V_T$ $V_D = (V_G - V_T)$

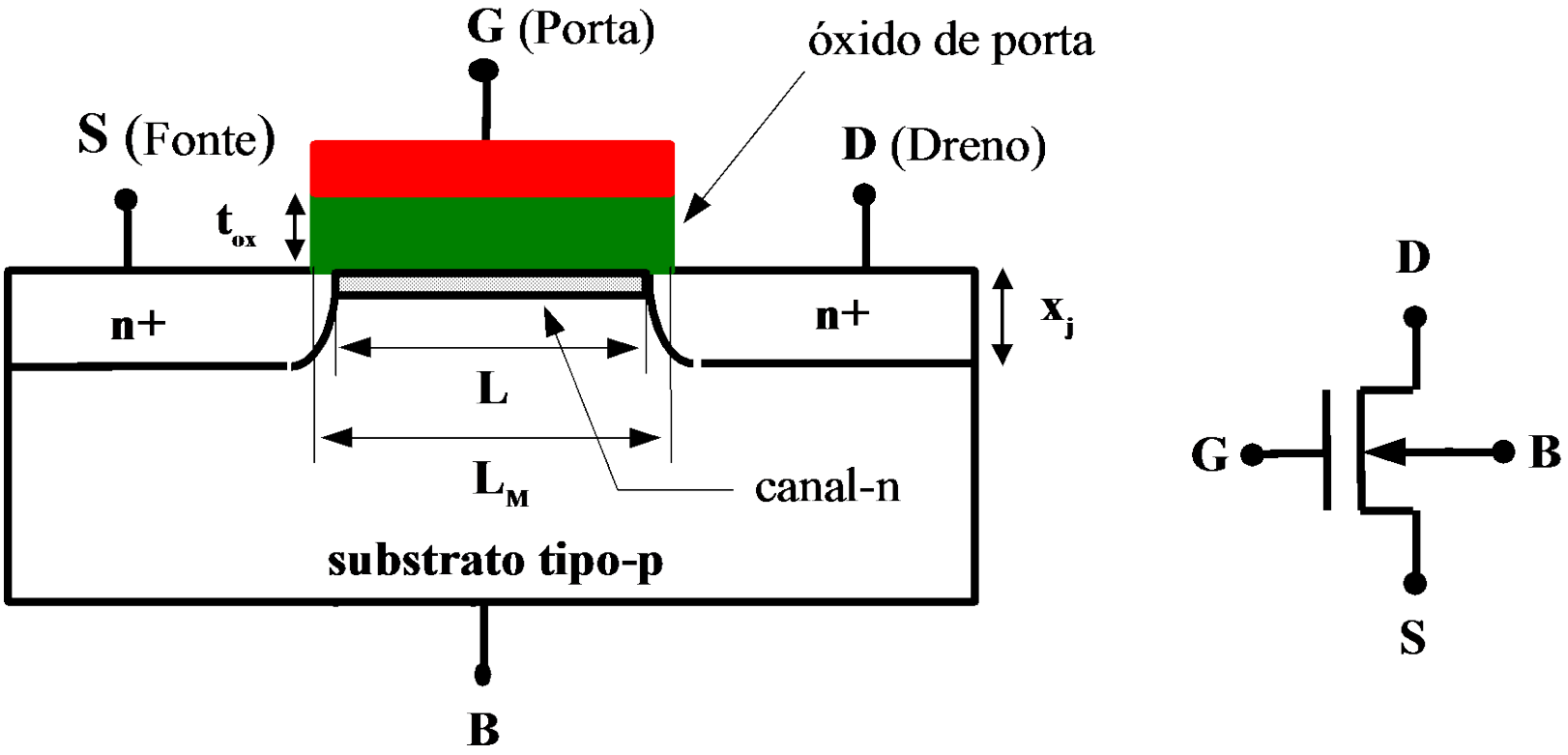
MOSFET



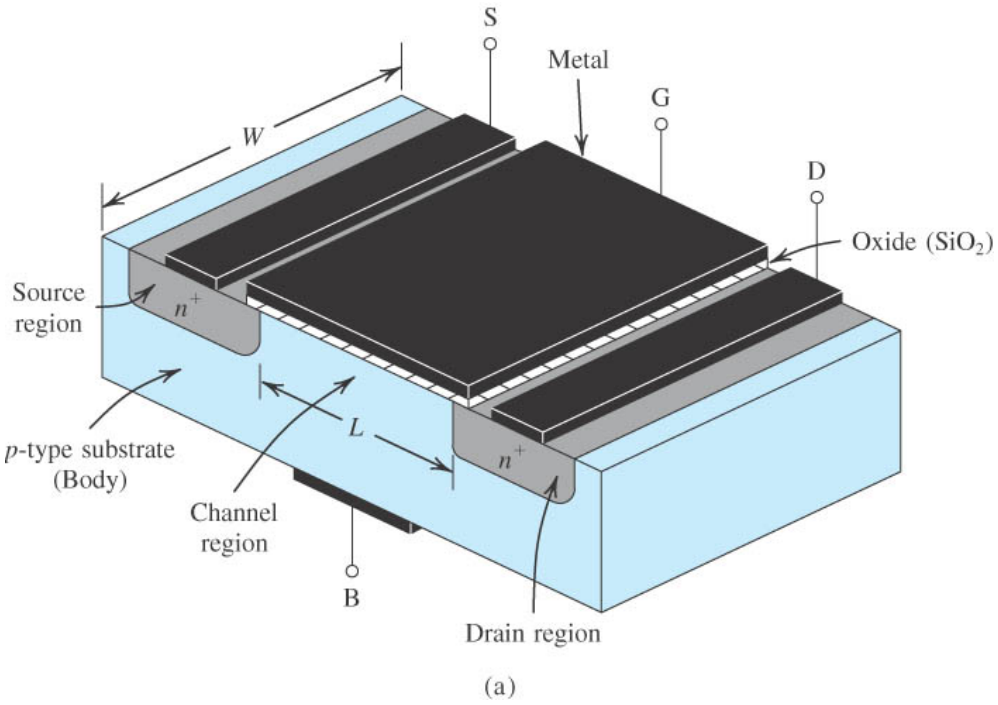
MOSFET: Curva I_D x V_D



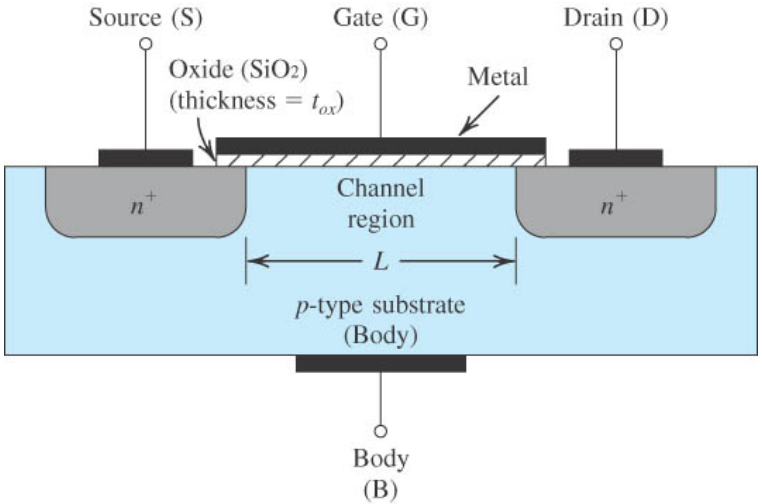
MOSFET


G (Porta)
óxido de porta
S (Fonte)
D (Dreno)
t_{ox}
n+
n+
x_j
L
L_M
canal-n
substrato tipo-p
B
D
G
B
S

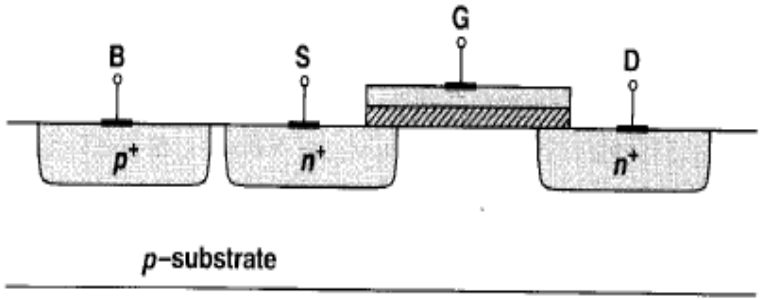
MOSFET


S
Metal
G
W
D
Oxide (SiO_2)
Source region
n^+
p-type substrate (Body)
L
Channel region
n^+
B
Drain region

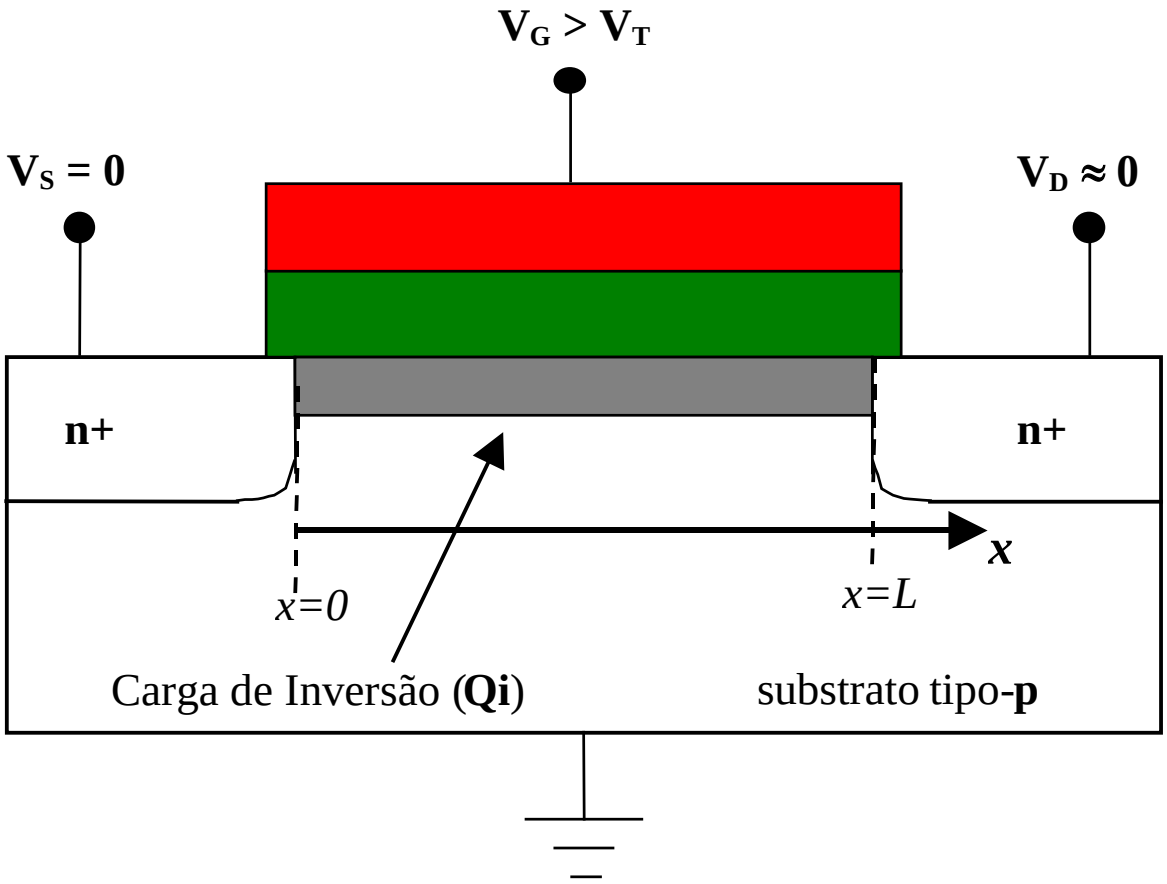
(a)


Source (S)
Gate (G)
Drain (D)
Oxide (SiO_2) (thickness = t_{ox})
Metal
n^+
Channel region
n^+
L
p-type substrate (Body)
Body (B)

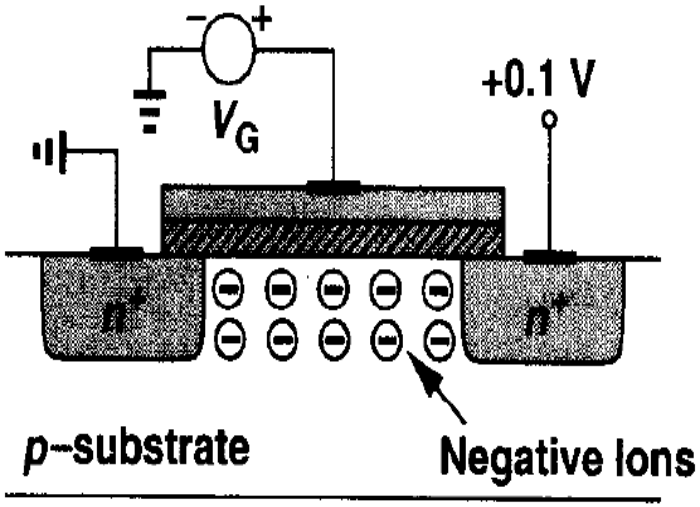
(b)

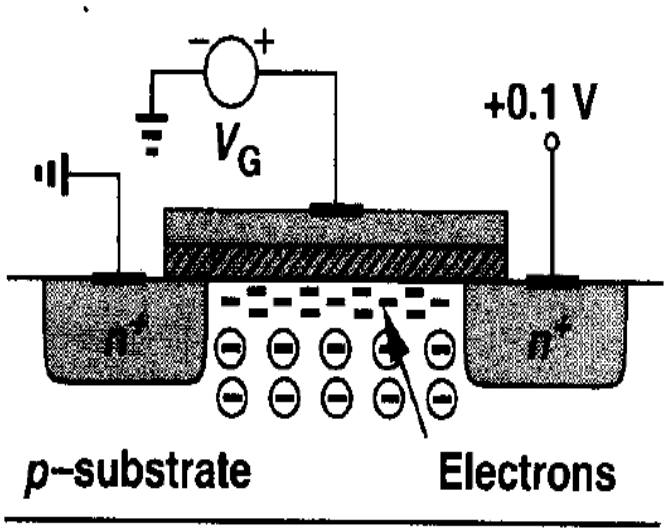

B
S
G
D
p^+
n^+
n^+
p–substrate

MOSFET


$V_G > V_T$
$V_S = 0$
$V_D \approx 0$
n+
n+
x
x=0
x=L
Carga de Inversão (Qi)
substrato tipo-p

MOSFET – Threshold Voltage

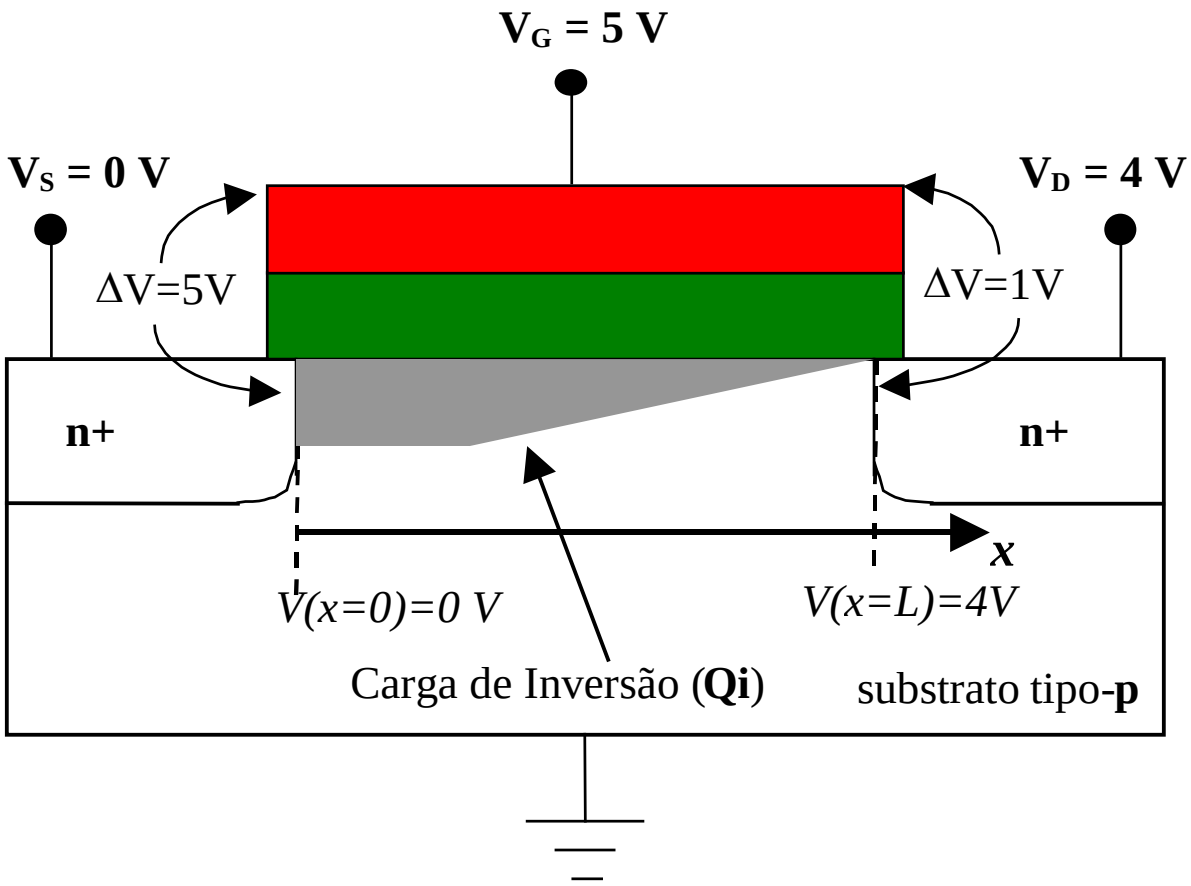




usually defined as the gate voltage for which the interface is "as much n-type as the substrate is p-type." It can be proved [1] that[3]

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

MOSFET


V_G = 5 V
V_S = 0 V
V_D = 4 V
ΔV=5V
ΔV=1V
n+
n+
x
V(x=0)=0 V
V(x=L)=4V
Carga de Inversão (Qi)
substrato tipo-p

Modelo I-V quadrático básico

- **Carga de inversão (densidade)**

$$Q_i(x) \cong C_{ox}\left(V_{GS} - V_T - V(x)\right)$$

$$Q_I' = -C_{ox}'\left(V_G - V_{FB} - \phi_s - \gamma\sqrt{\phi_s - \phi_t}\right)$$

Modelo I-V quadrático básico

- **Corrente total no canal**

$$I_{DS} = \mu W Q_i(x) \frac{dV(x)}{dx}$$

$$I_{DS} = \mu C_{ox} W \left(V_{GS} - V_T - V(x) \right) \frac{dV(x)}{dx}$$

Modelo I-V quadrático básico

- **Corrente total no canal e “beta”**

$$I_{DS}\int_0^L dx = \mu C_{ox} W \int_0^{V_{DS}} \left(V_{GS} - V_T - V(x)\right) dV$$

$$I_{DS} = \beta.\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$\beta \equiv \mu C_{ox} \frac{W}{L}$$

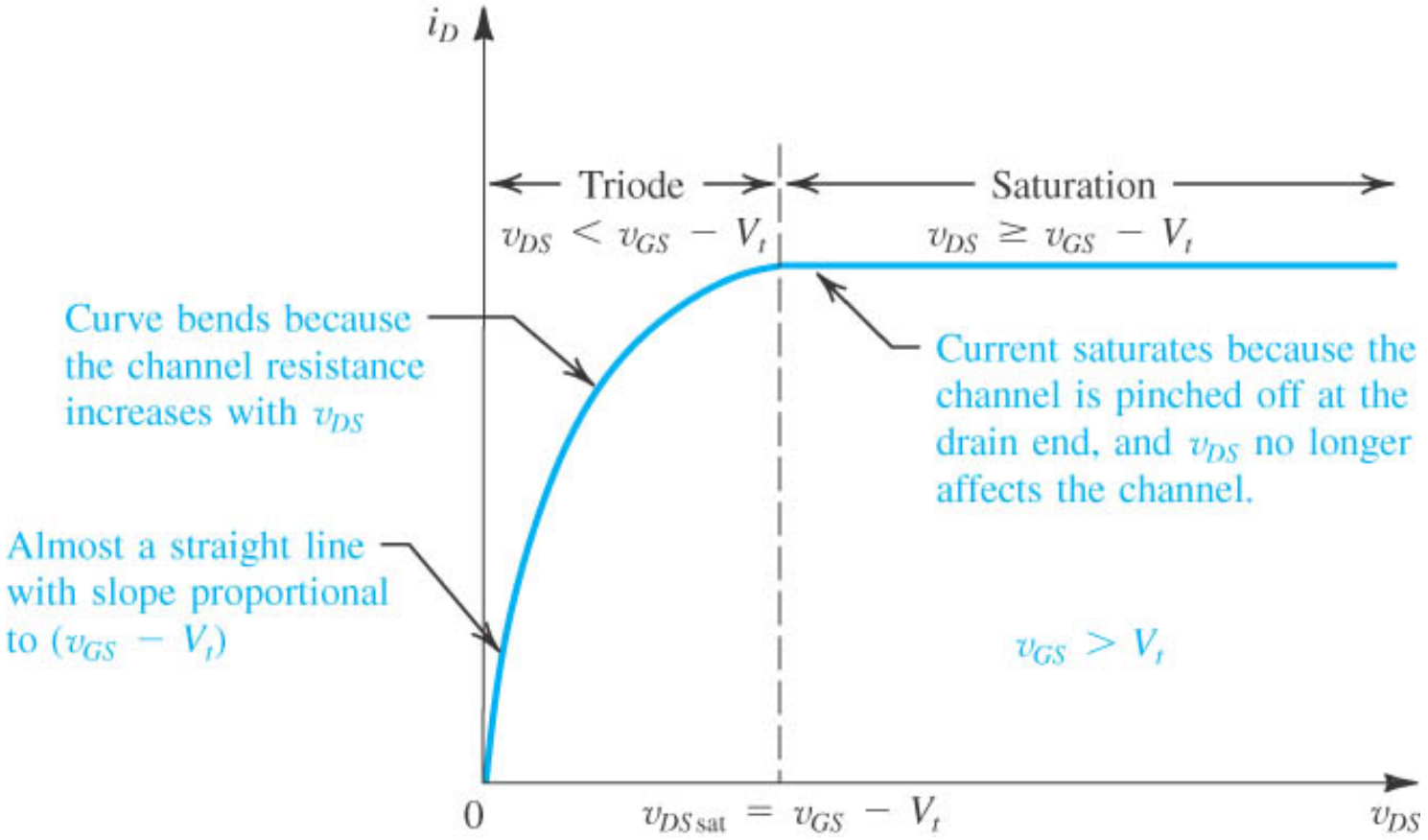
Corrente I_D MOSFET

$$I_{DS} = \beta.\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Zona Linear (Triodo) $I_{DS} = \beta.\left[(V_{GS} - V_T)V_{DS}\right]$

Zona de Saturação $I_{DS} = \frac{\beta}{2}.(V_{GS} - V_T)^2$

Características Transistor MOS



Zona de saturação

- **Parâmetro “lambda”**

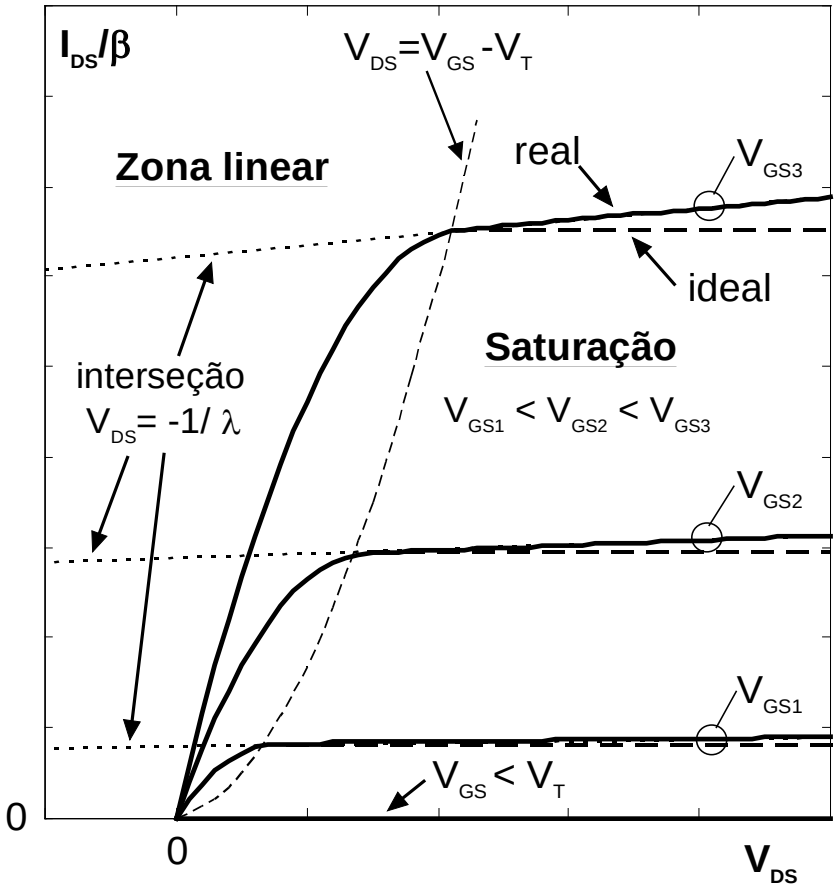
Para

$V_{GS} >= V_T$

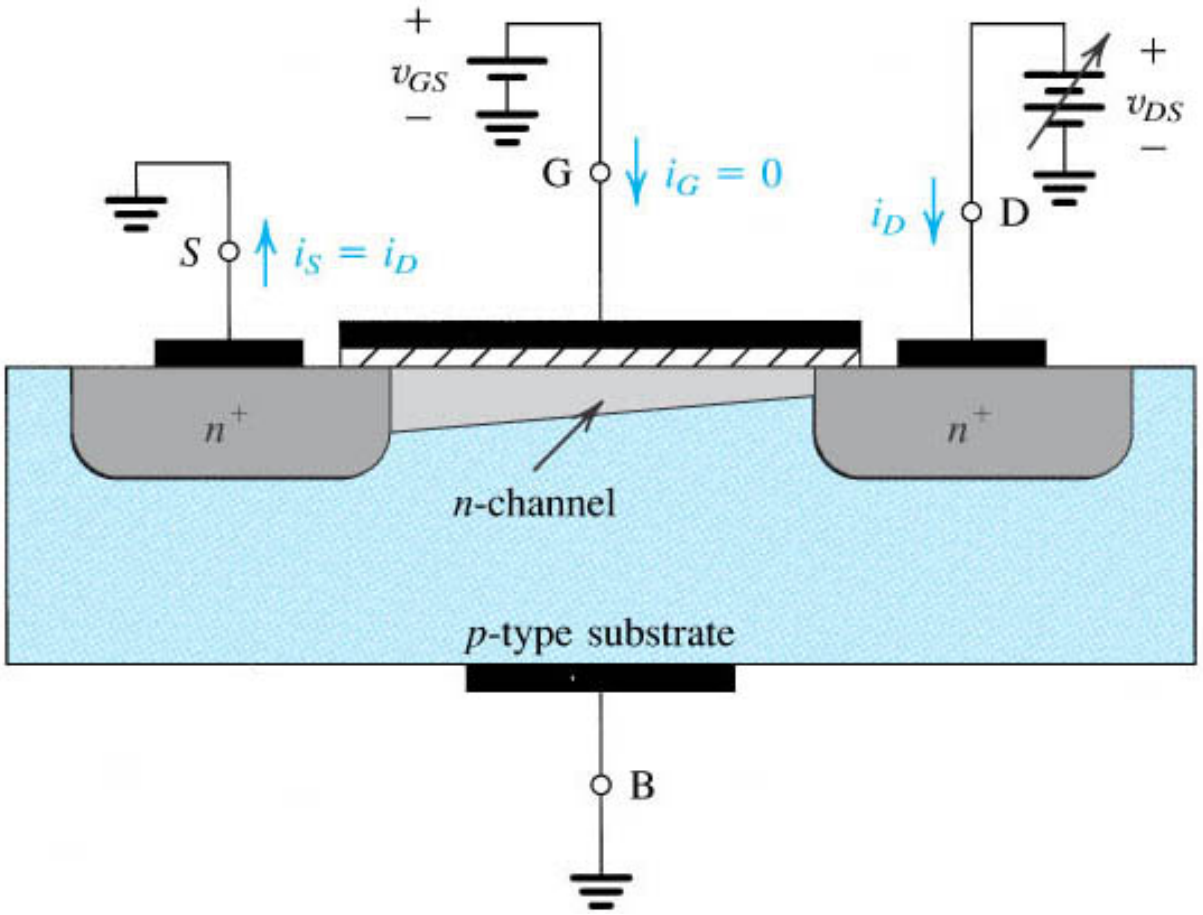
$V_{DS} >= V_{GS} - V_T$

$$I_{DS} = \frac{\beta}{2}.\left(V_{GS} - V_T\right)^2$$

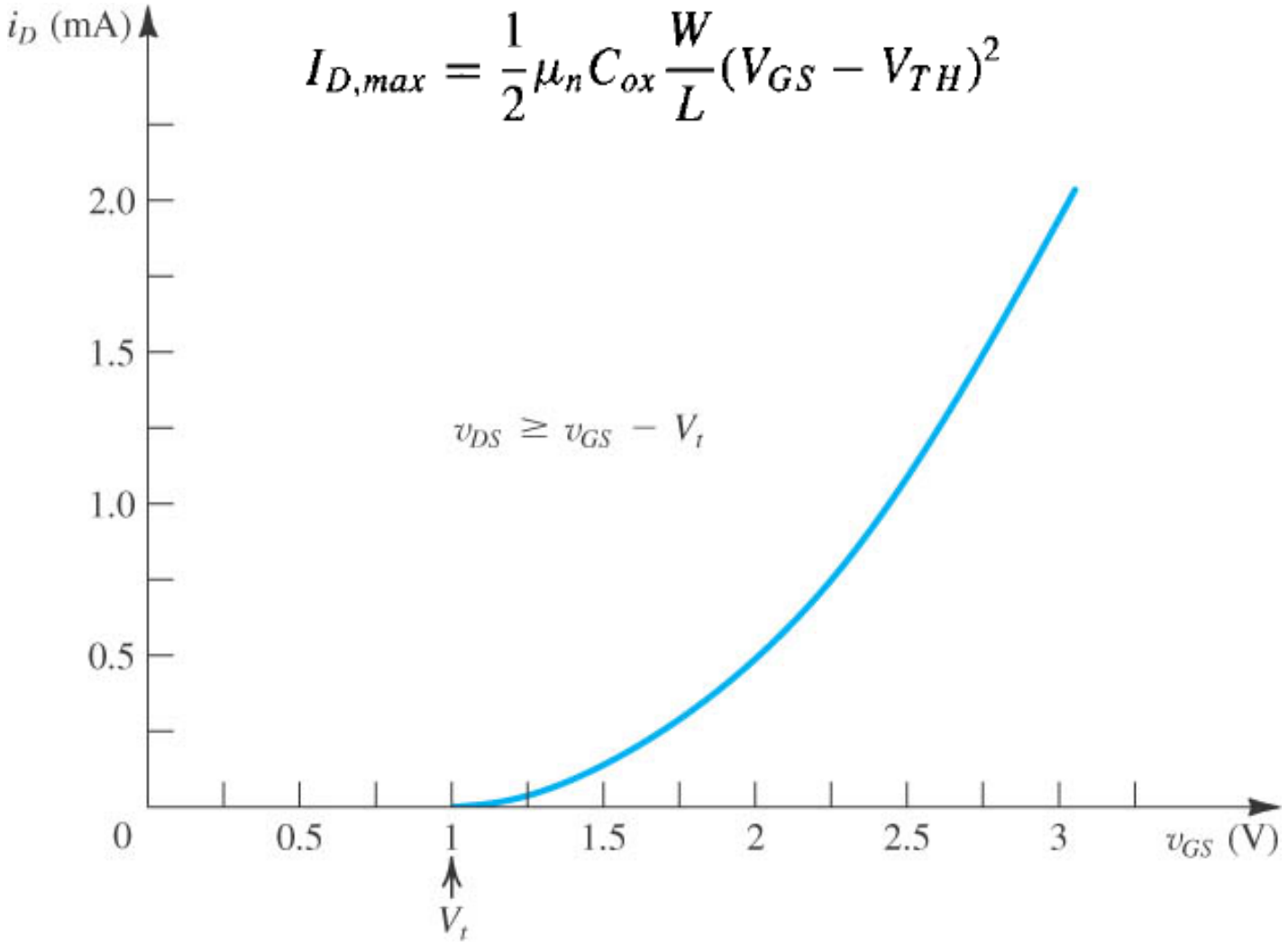
$$I_{DS} = \frac{\beta}{2}.\left(V_{GS} - V_T\right)^2.(1 + \lambda V_{DS})$$



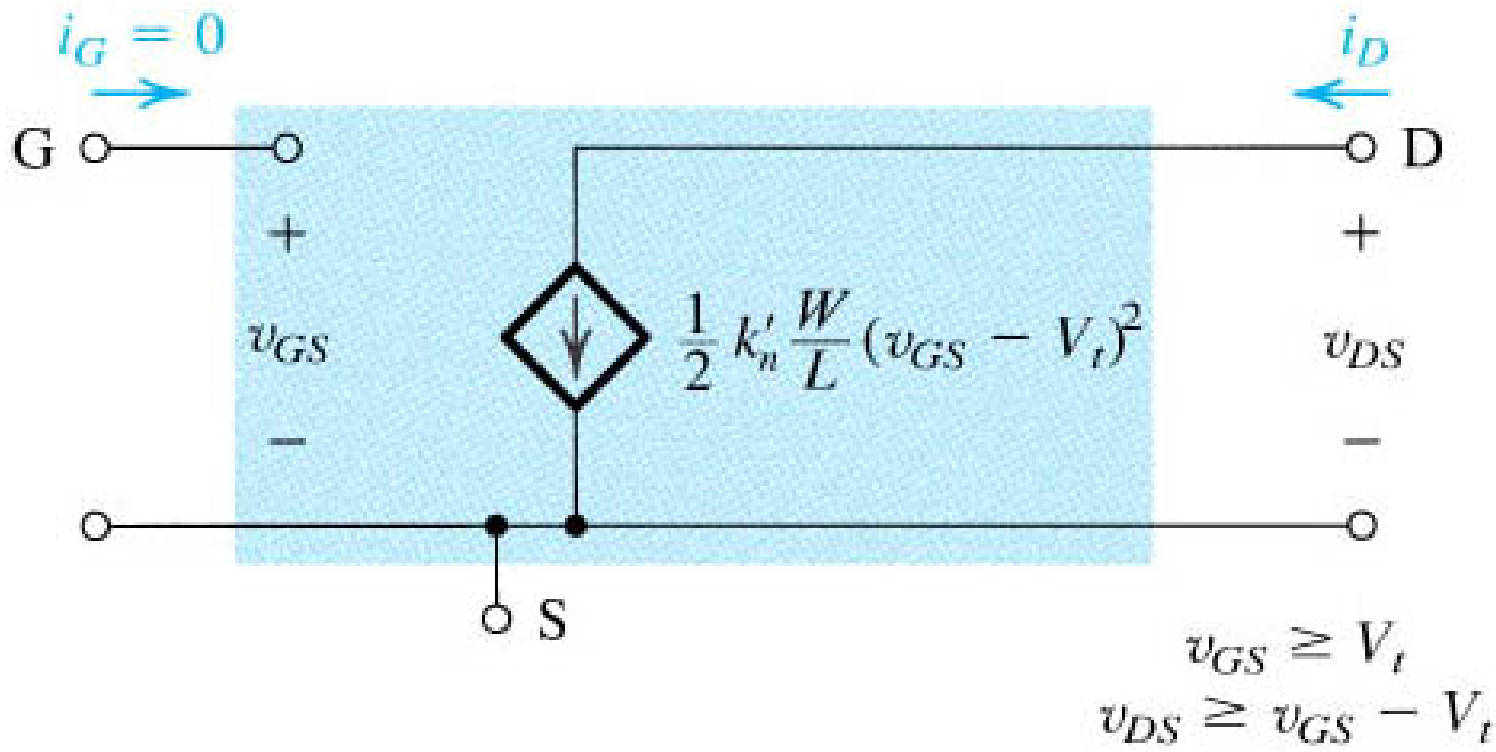
Características Transistor MOS



Características Transistor MOS: Saturação

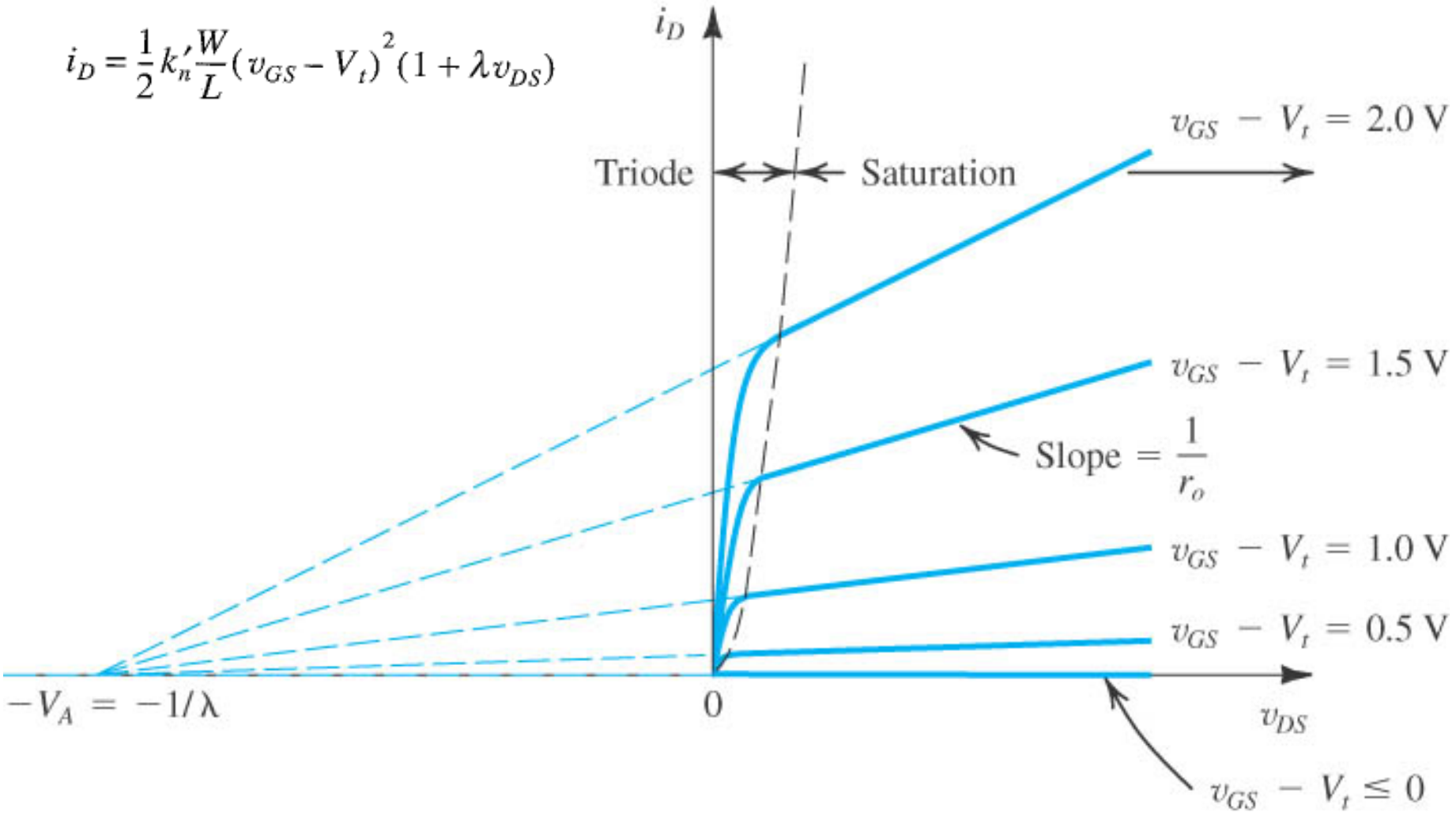


Características Transistor MOS: Saturação

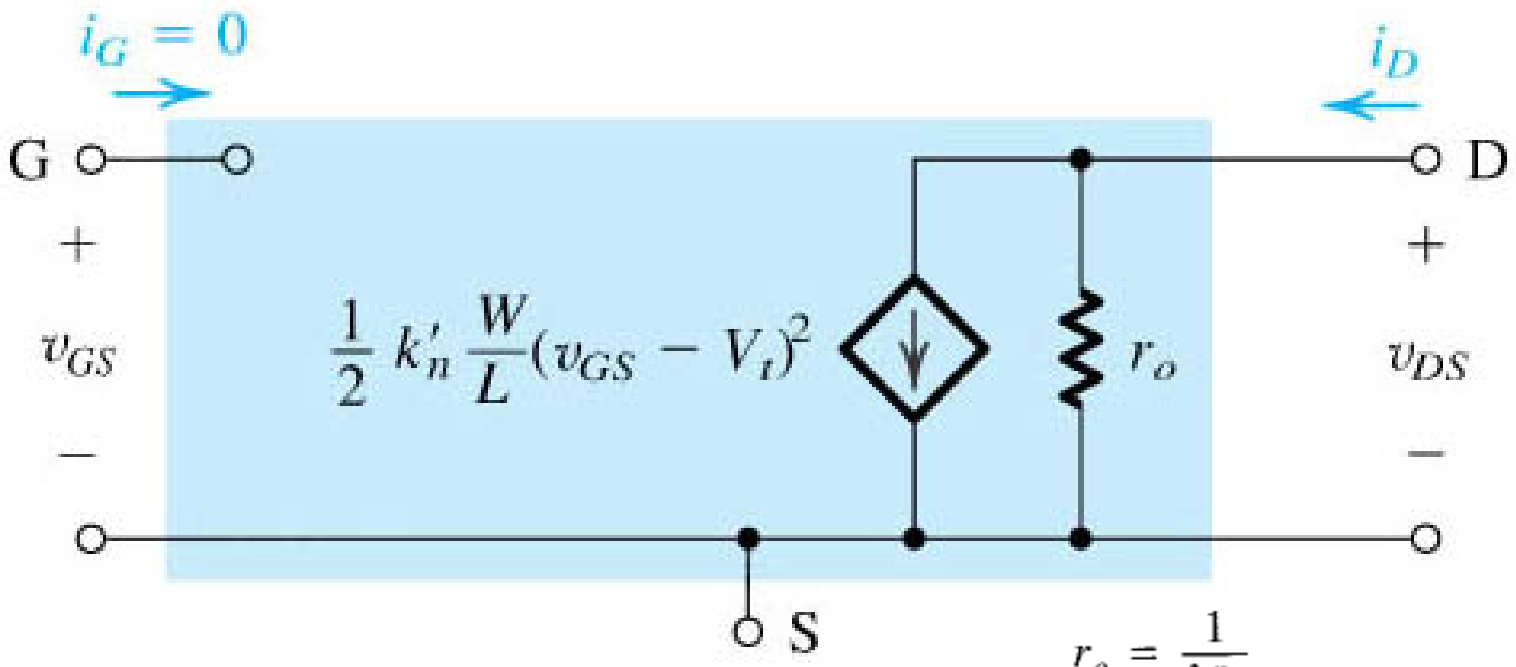


Características Transistor MOS: Saturação

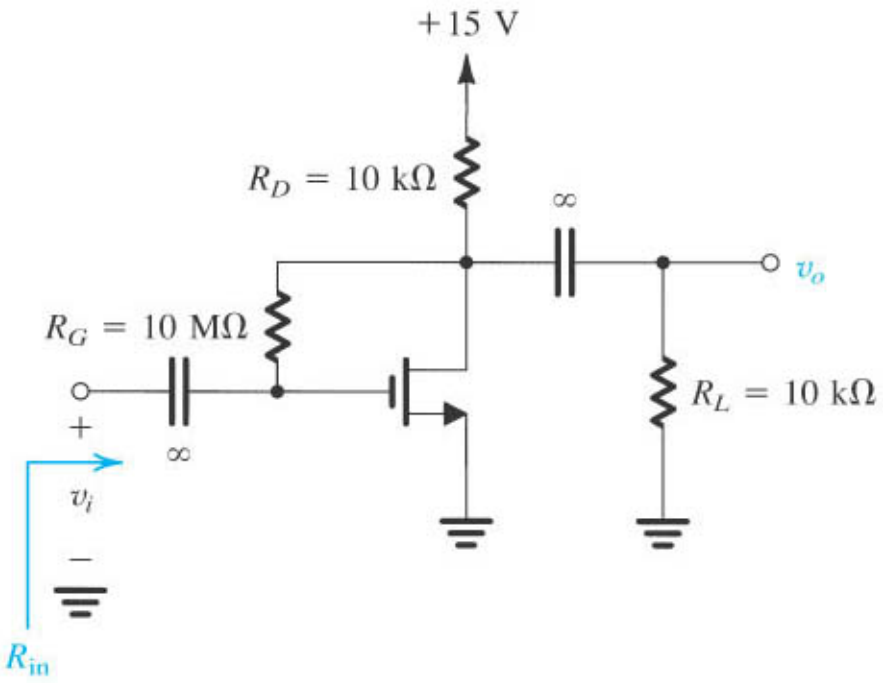
$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$



Características Transistor MOS: Saturação

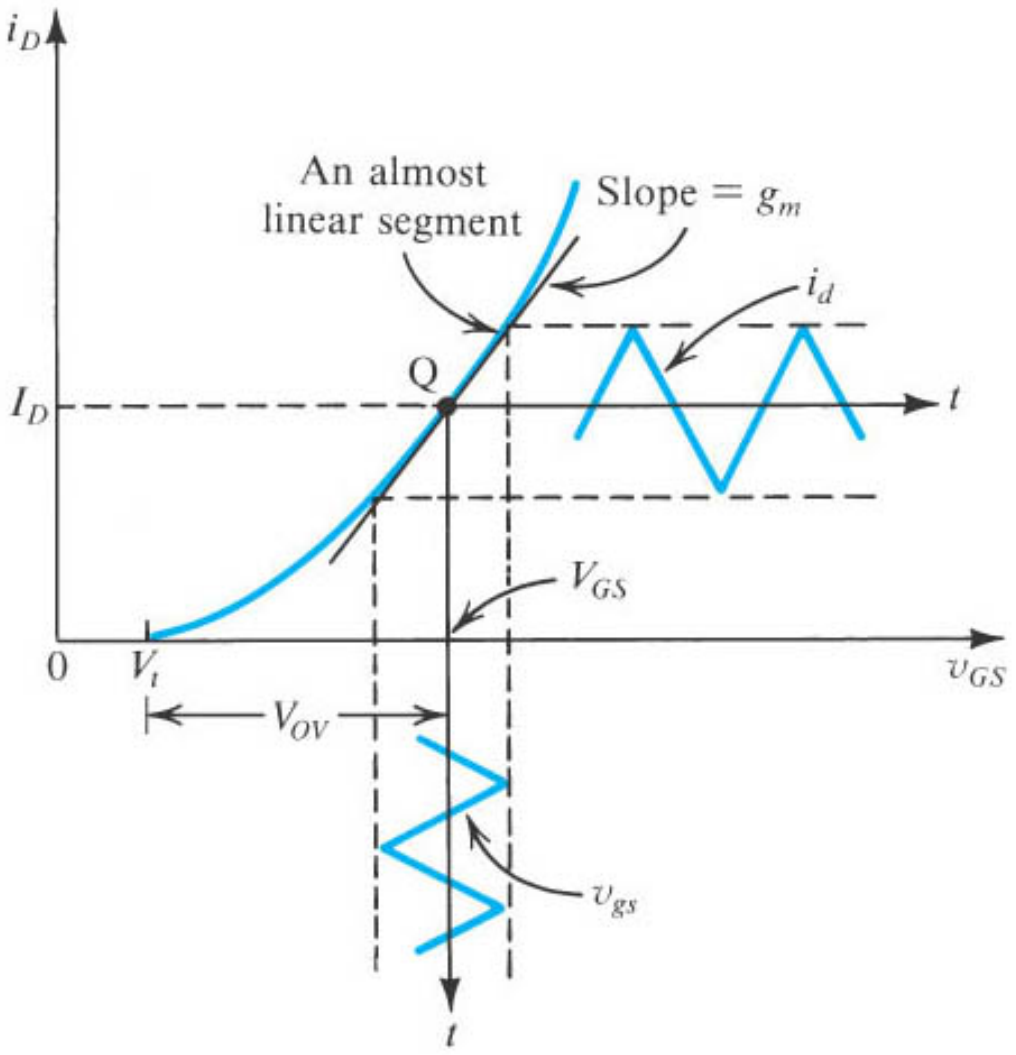


Características Transistor MOS: **Pequenos Sinais**

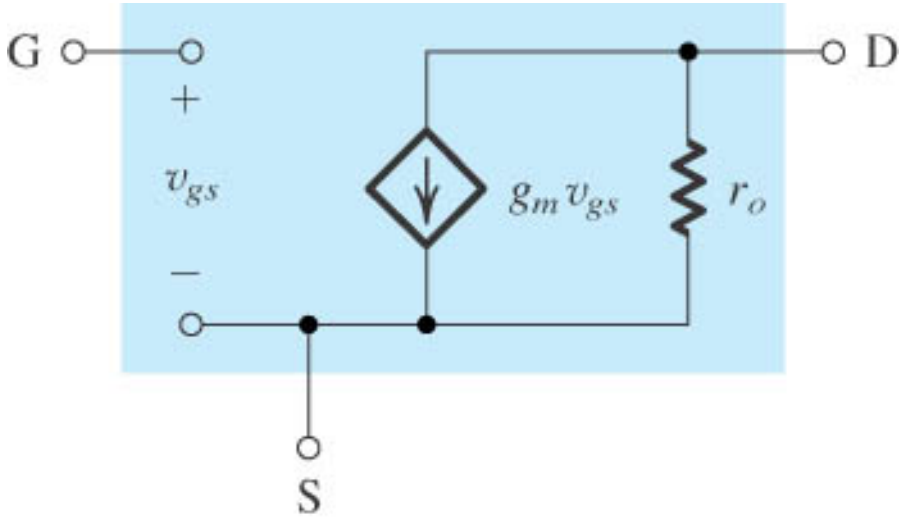


(a)

Características Transistor MOS: **Pequenos Sinais**



Características Transistor MOS: **Pequenos Sinais**



(b)

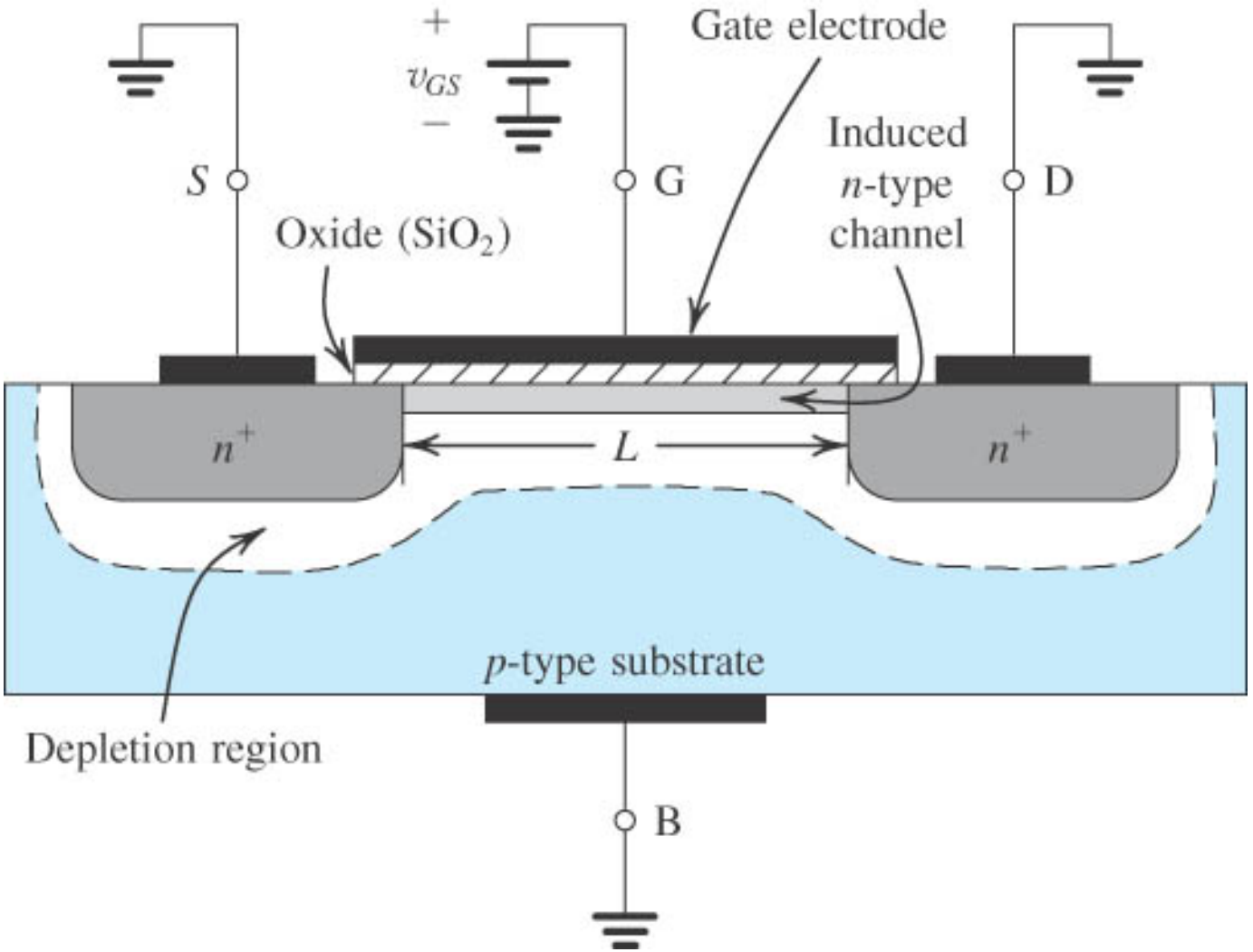
$$r_o = \frac{1}{\lambda I_D}$$

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V DS,\text{const.}}$$

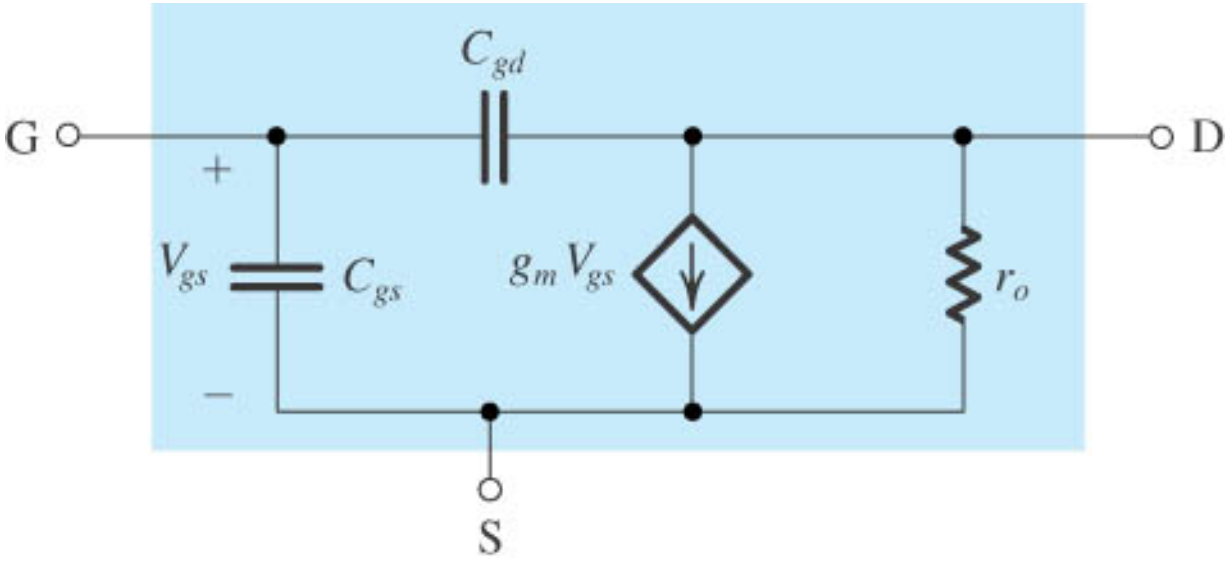
$$= \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}).$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

Características Transistor MOS: Alta Freq

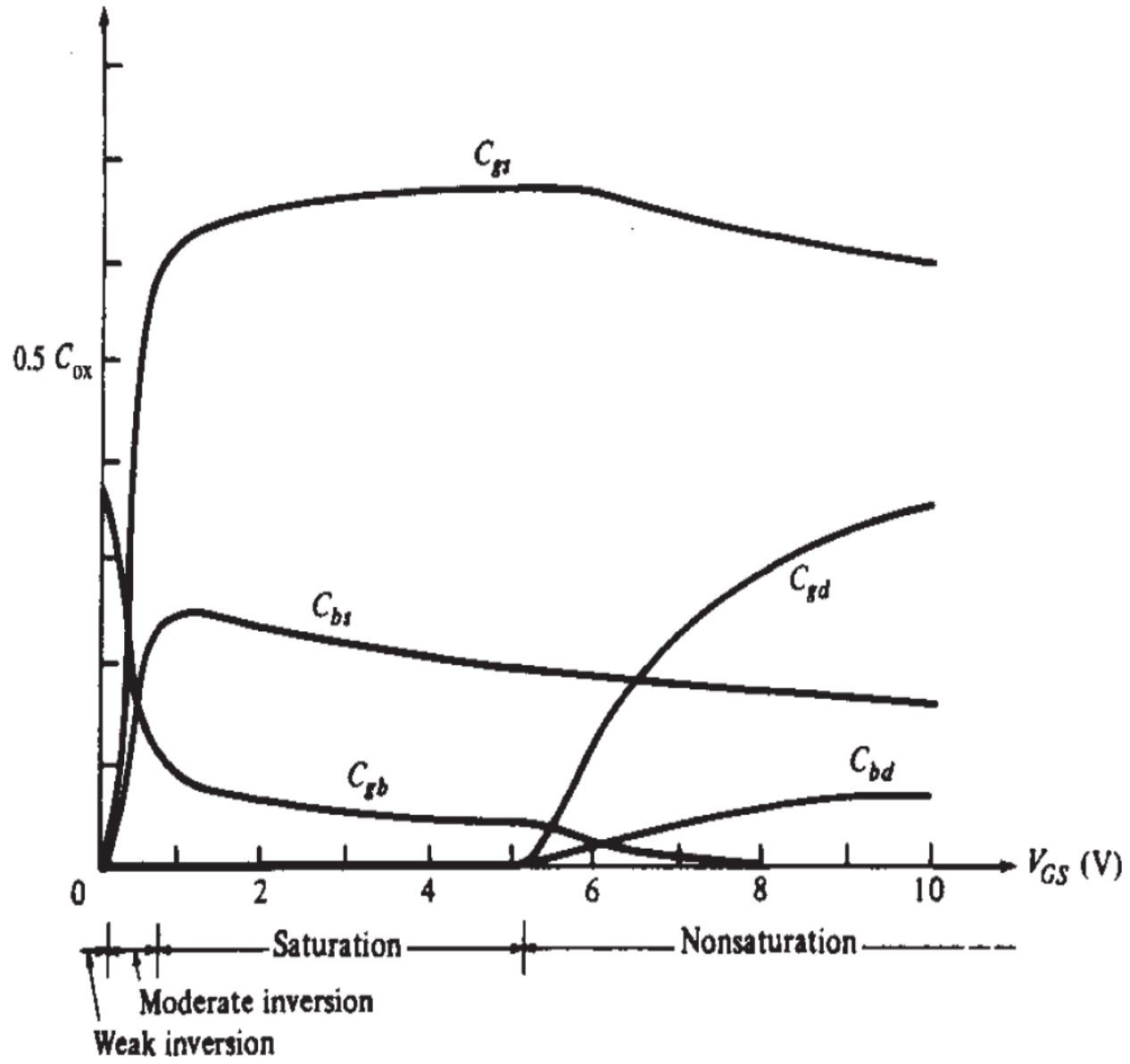


Características Transistor MOS: Alta Freq

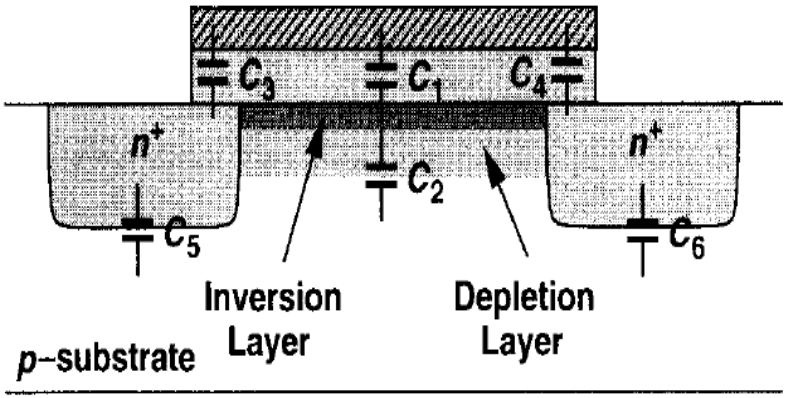


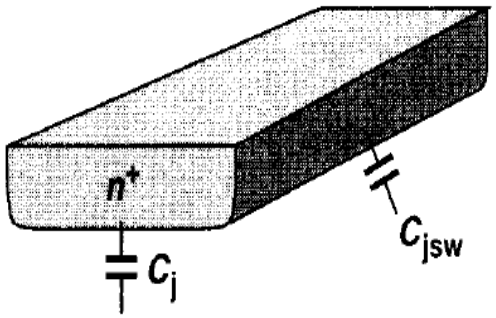
(c)

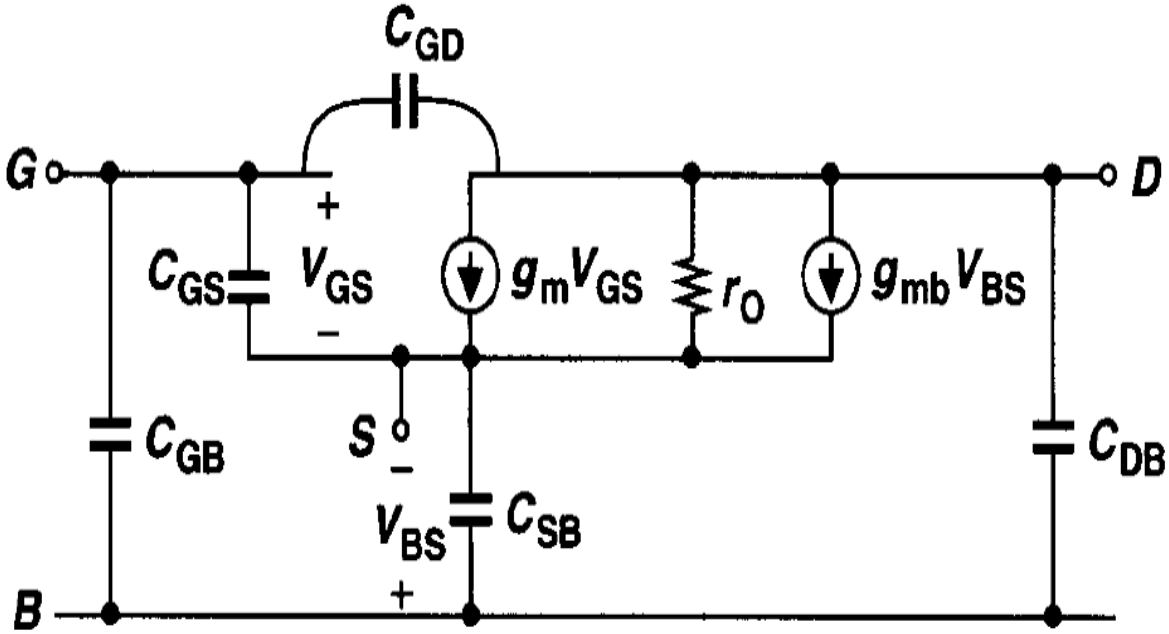
Características Transistor MOS: Alta Freq

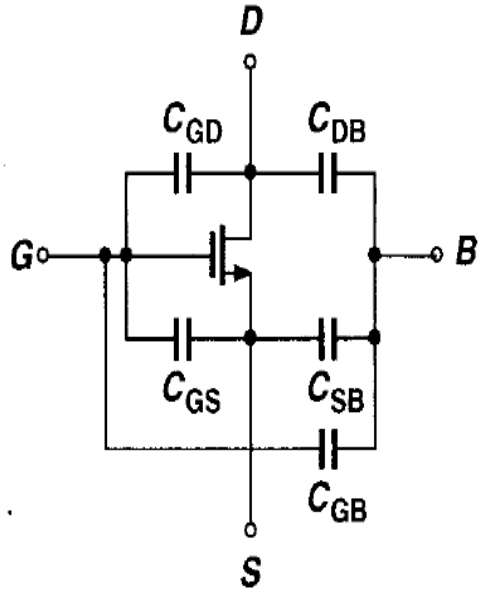


Características Transistor MOS: Alta Freq

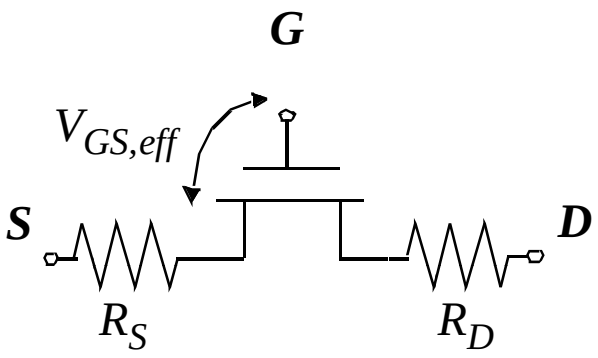


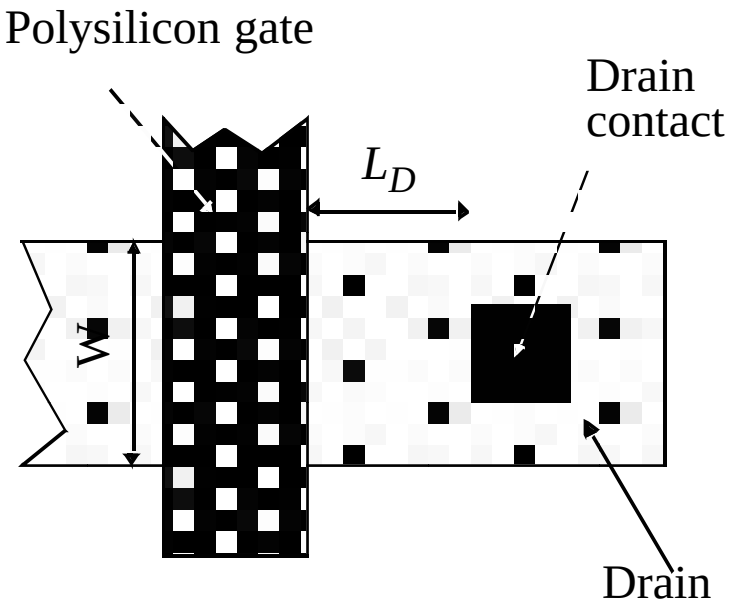






Resistência Parasita





MOSFET: SPICE Simulation

Forma Geral:

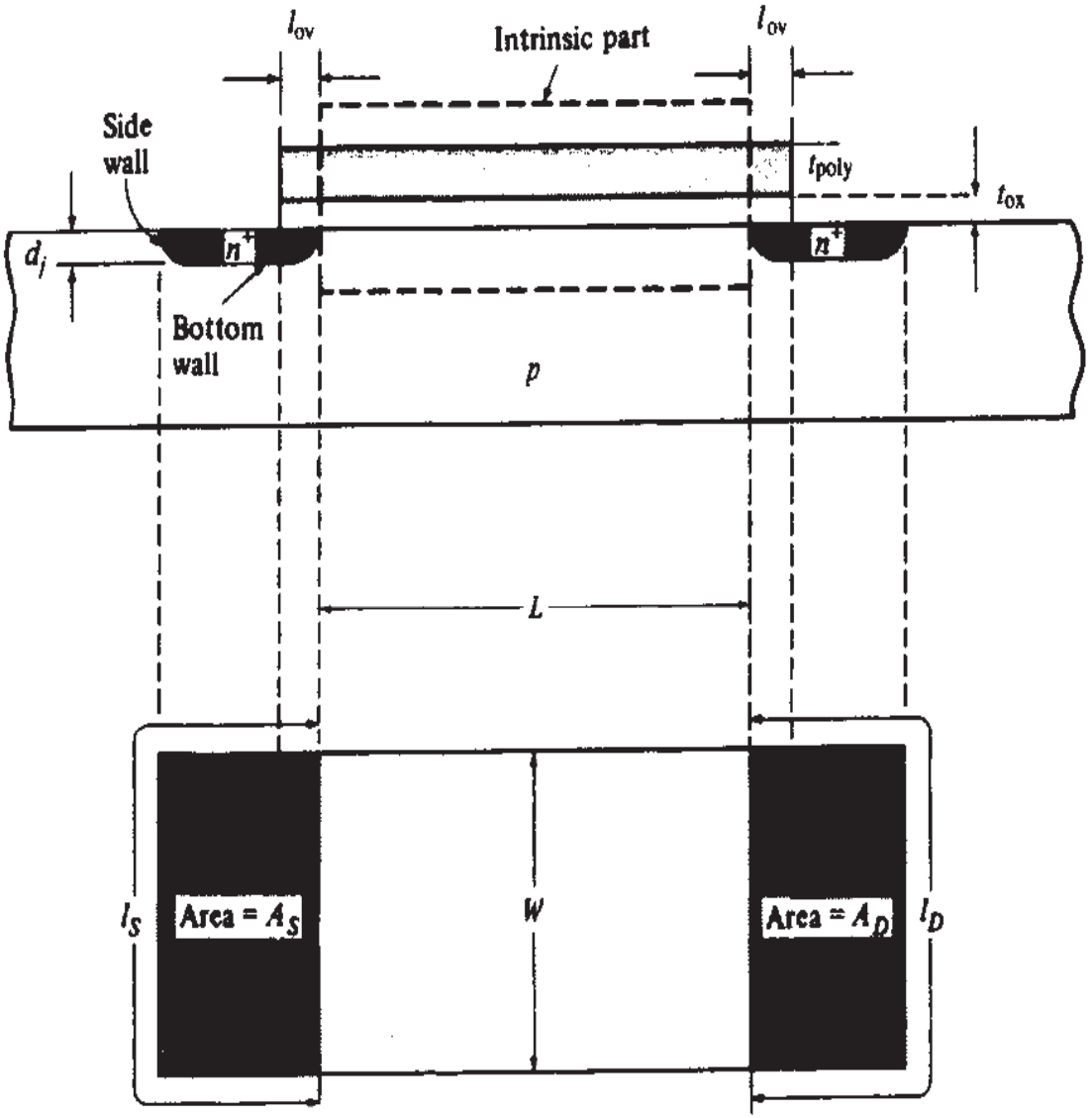
```
MXXXXXXX ND NG NS NB MNAME <L=VAL> <W=VAL> <AD=VAL> <AS=VAL>
+ <PD=VAL> <PS=VAL> <NRD=VAL> <NRS=VAL> <OFF>
+ <IC=VDS, VGS, VBS> <TEMP=T>
```

Exemplo:

```
M1 2 9 3 0 MOD1 L=10U W=5U AD=100P AS=100P PD=40U PS=40U
```

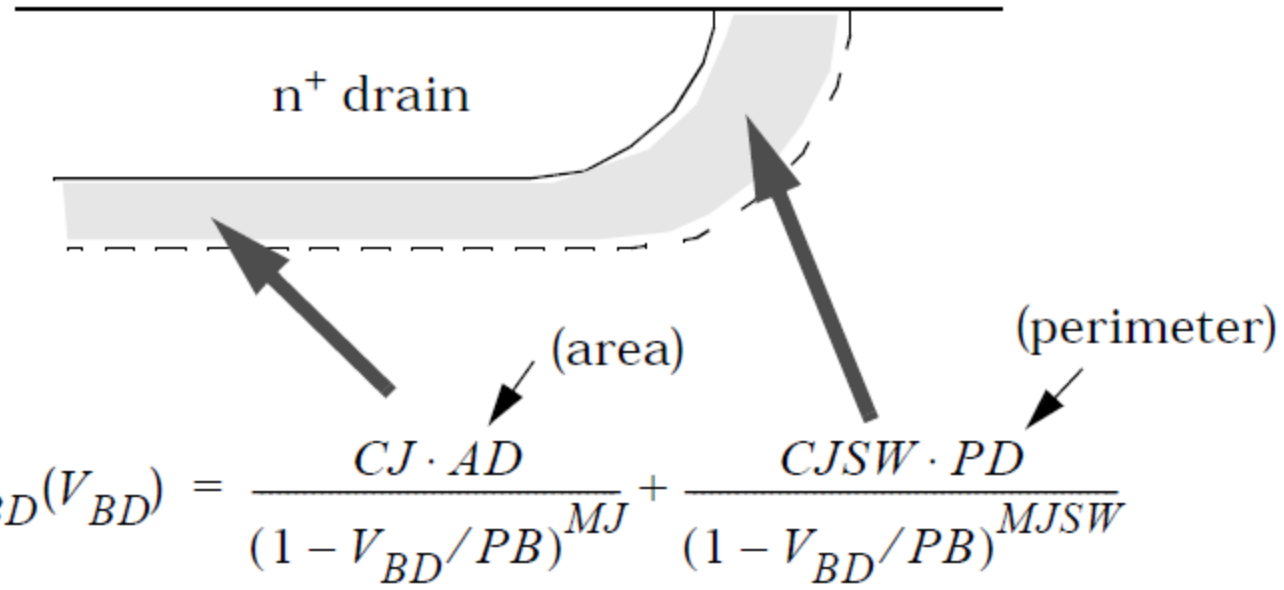
ND, NG, NS, and NB are the drain, gate, source, and bulk (substrate) nodes, respectively. MNAME is the model name. L and W are the channel length and width, in meters. AD and AS are the areas of the drain and source diffusions, in meters^2. Note that the suffix U specifies microns (1e-6 m) and P sq-microns (1e-12 m^2). If any of L, W, AD, or AS are not specified, default values are used. The use of defaults simplifies input file preparation, as well as the editing required if device geometries are to be changed. PD and PS are the perimeters of the drain and source junctions, in meters. NRD and NRS designate the equivalent number of squares of the drain and source diffusions; these values multiply the sheet resistance RSH specified on the .MODEL control line for an accurate representation of the parasitic series drain and source resistance of each transistor. PD and PS default to 0.0 while NRD and NRS to 1.0. OFF indicates an (optional) initial condition on the device for dc analysis. The (optional) initial condition specification using IC=VDS, VGS, VBS is intended for use with the UIC option on the .TRAN control line, when a transient

MOSFET: SPICE Simulation

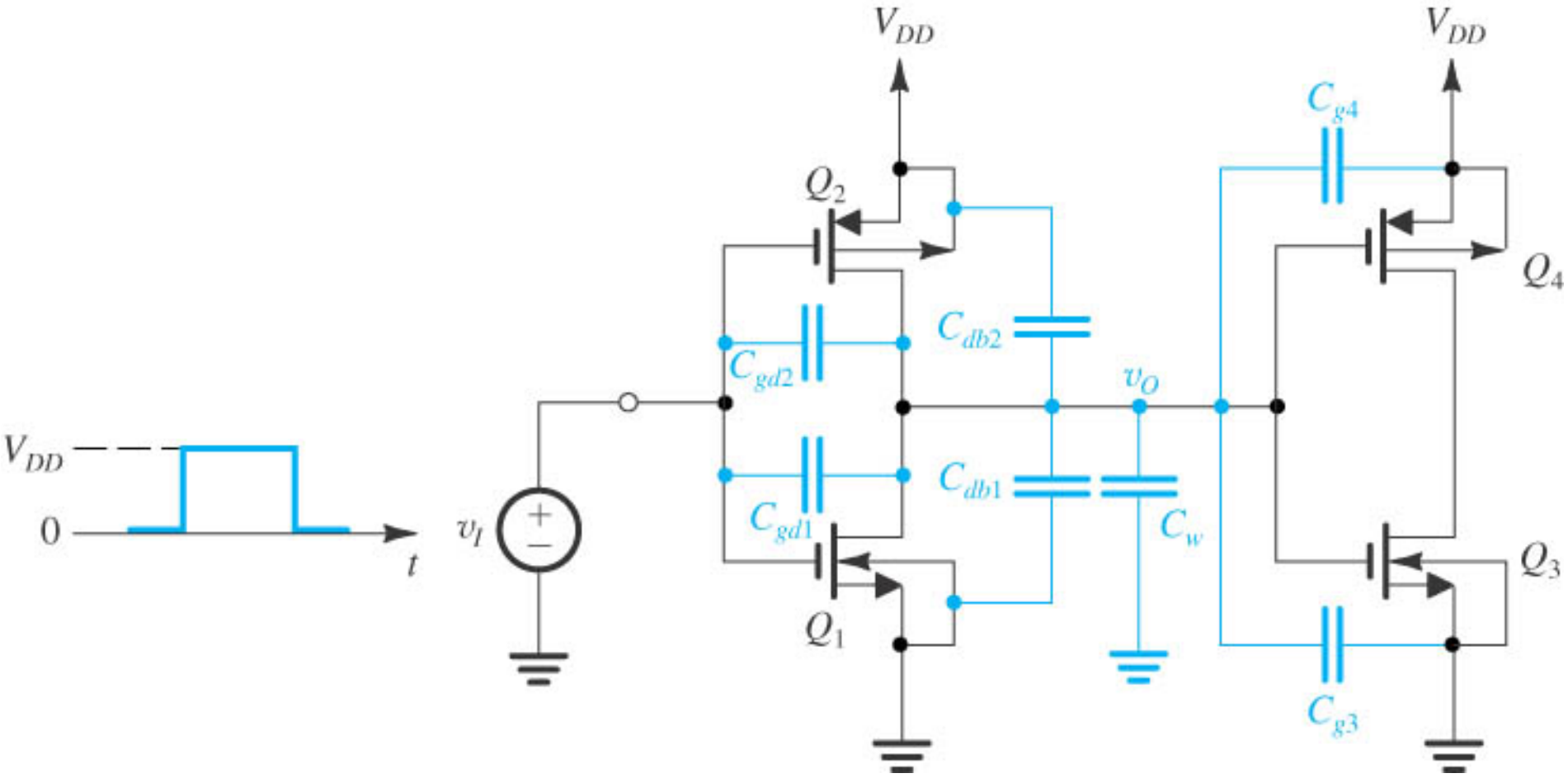


MOSFET: SPICE Simulation

As Capacitâncias de Junção são Independentes da Tensão de Operação?

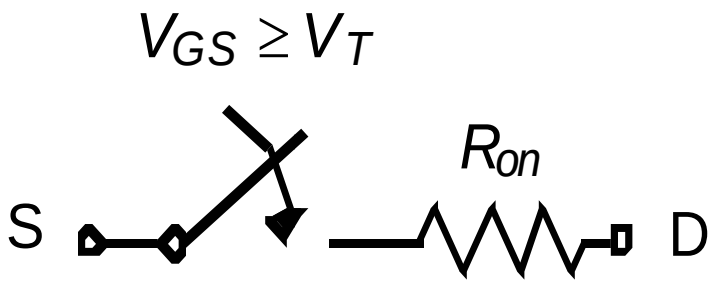


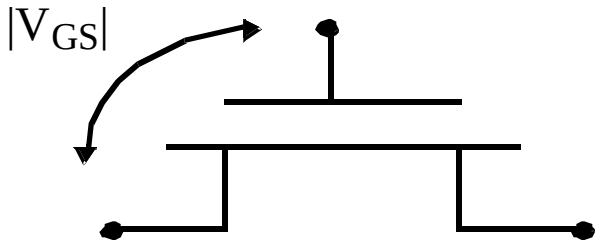
Digital MOSFET Circuits



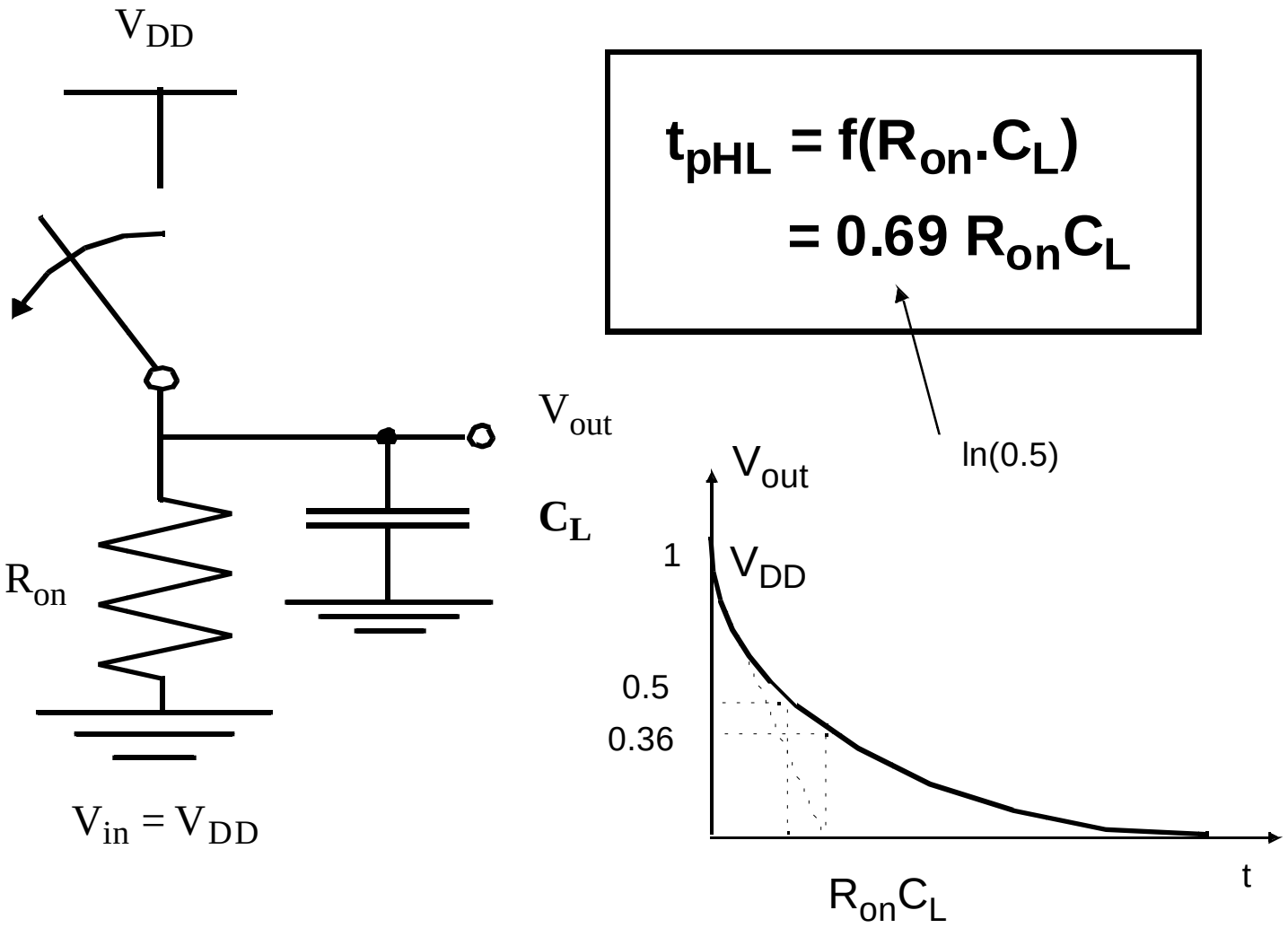
Digital MOSFET Circuits

A Switch! ⟷ An MOS Transistor

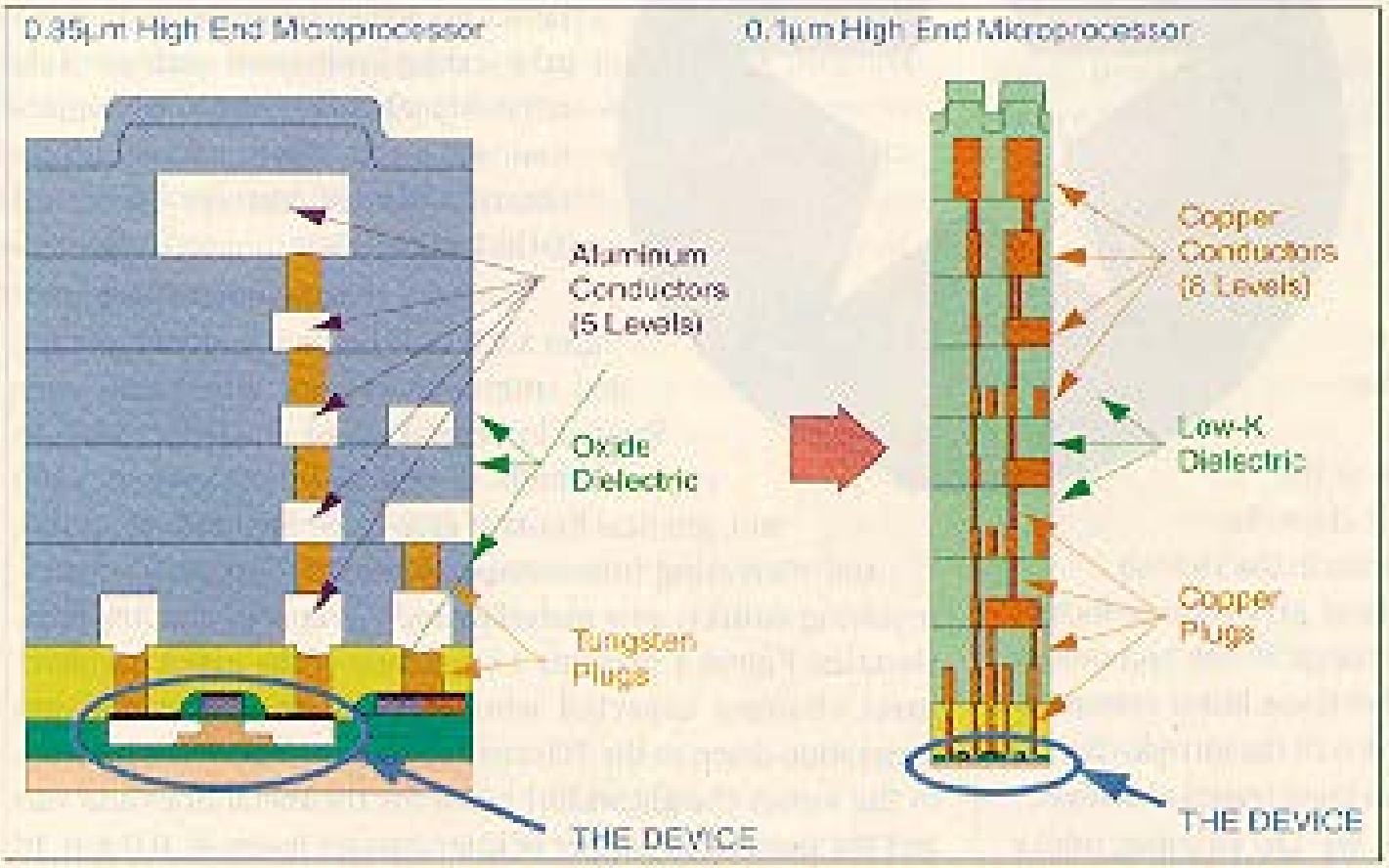




Digital MOSFET Circuits

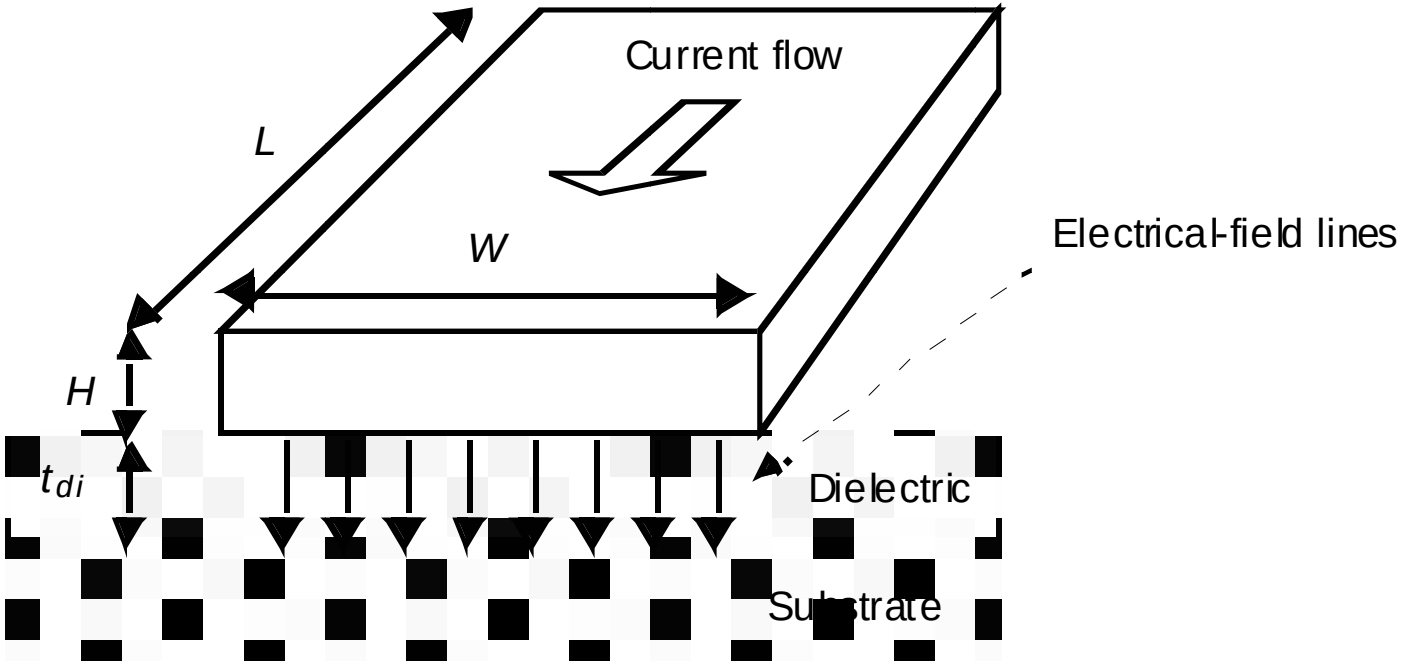


Interconexão



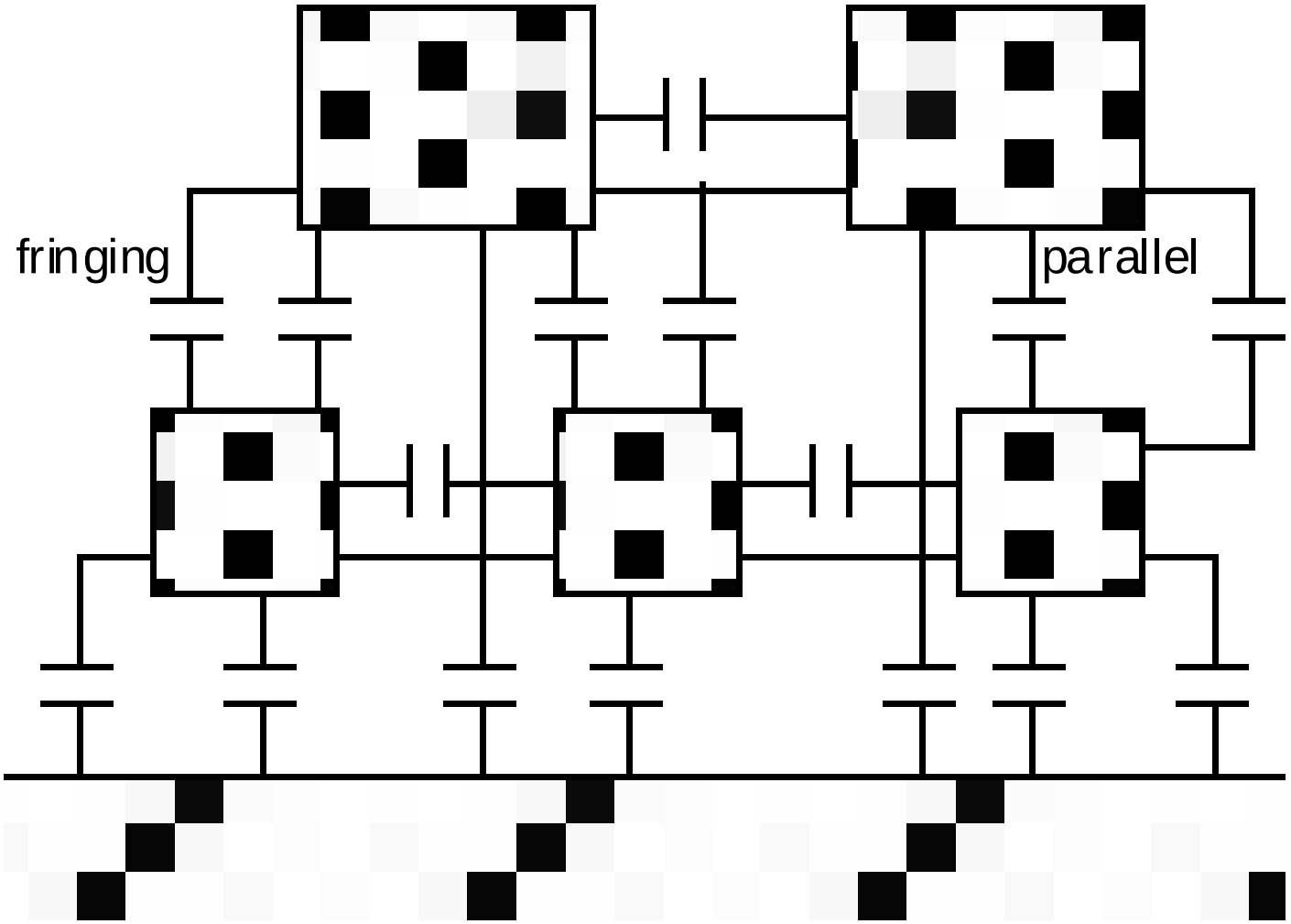
1. Process architecture challenge.

Interconexão: Capacitância

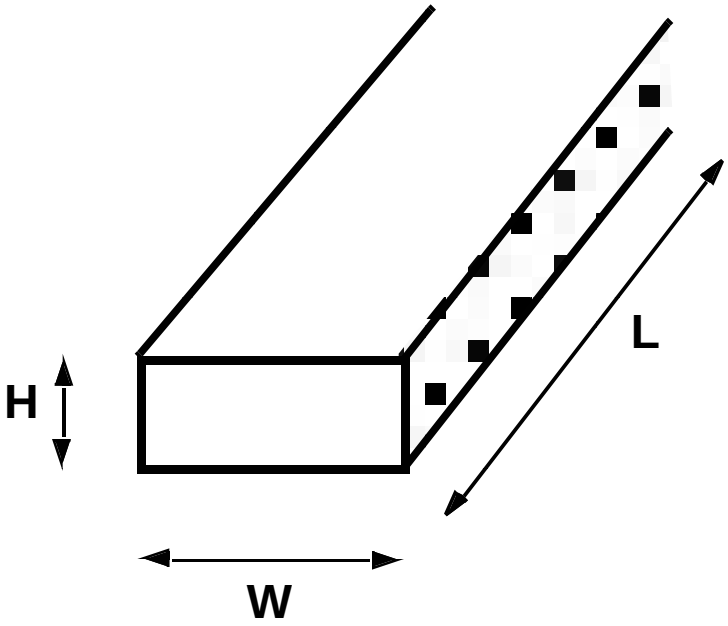


$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

Interconexão: Capacitância



Interconexão: Resistência

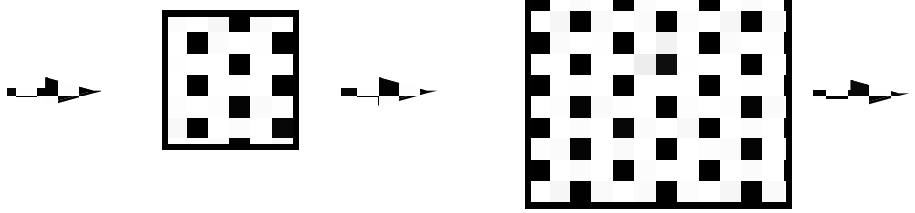


$$R = \rho \frac{L}{H\,W}$$

Sheet Resistance

R_o

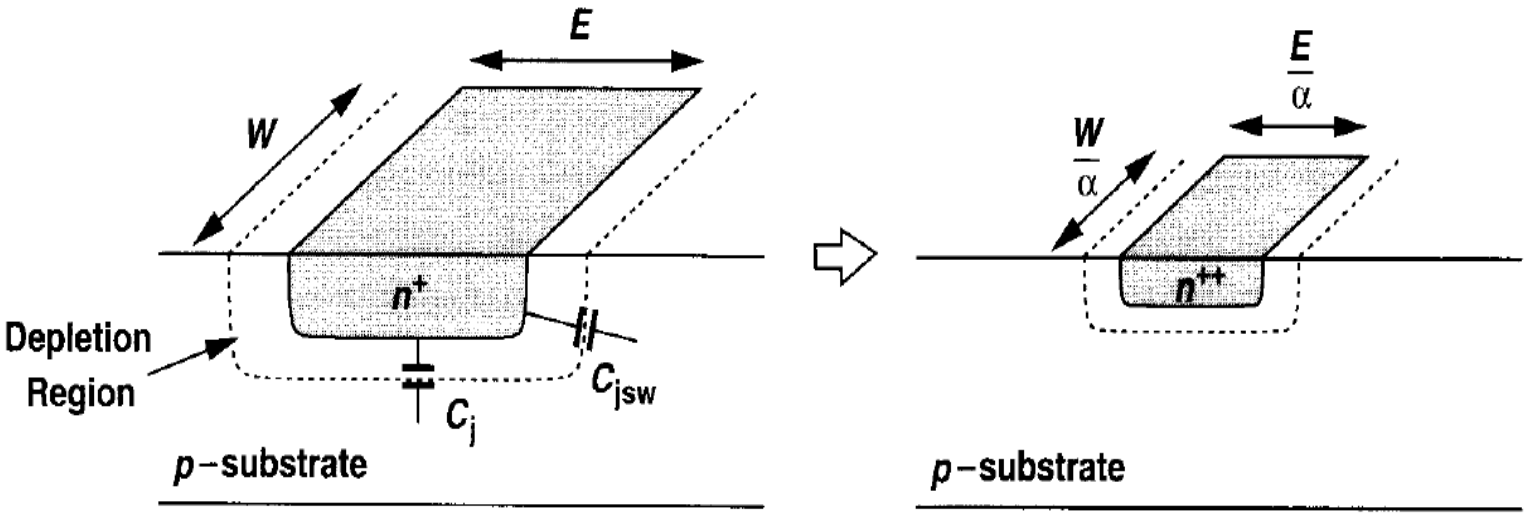
$R_1 \equiv R_2$



Interconexão: Resistência

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Scaling



- W e L decrease by a factor α
- Depletion Width decreases by a factor α

→ **All capacitances decreases by a factor α**

Razavi, pp. 581

Scaling

$$g_{m,scaled} = \mu(\alpha C_{ox})\frac{W/\alpha}{L/\alpha}\frac{V_{GS} - V_{TH}}{\alpha}$$

$$= \mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH}),$$

- t_{ox} decreases by a factor α → C_{ox} decreases by a factor α

- W and L decrease by a factor α

- Supply voltage and VTH are decreased by a factor α

→ **Transconductance remains constant**

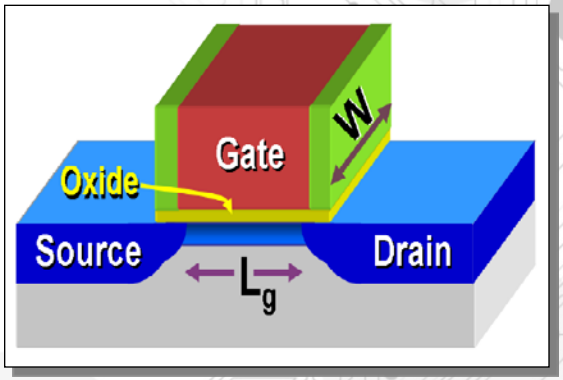
Obs.: If doping scales, output resistance r_0 is kept constant
However, dynamic range decreases.

Traditional Scaling

$$I_{Dsat} \approx \tfrac{1}{2} C_{ox} \mu (W/L_g)(V_G - V_T)^2$$

$= \varepsilon_o \varepsilon_s / T_{ox}$

- Reduce Gate Oxide Thickness

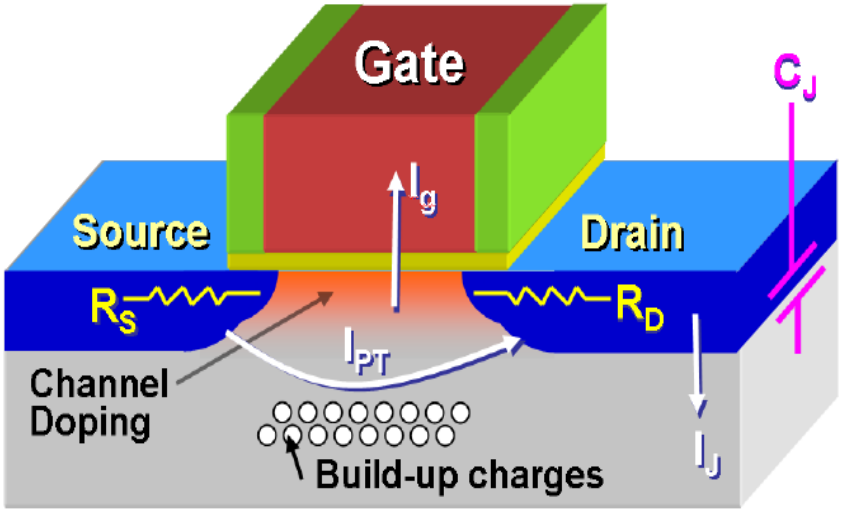


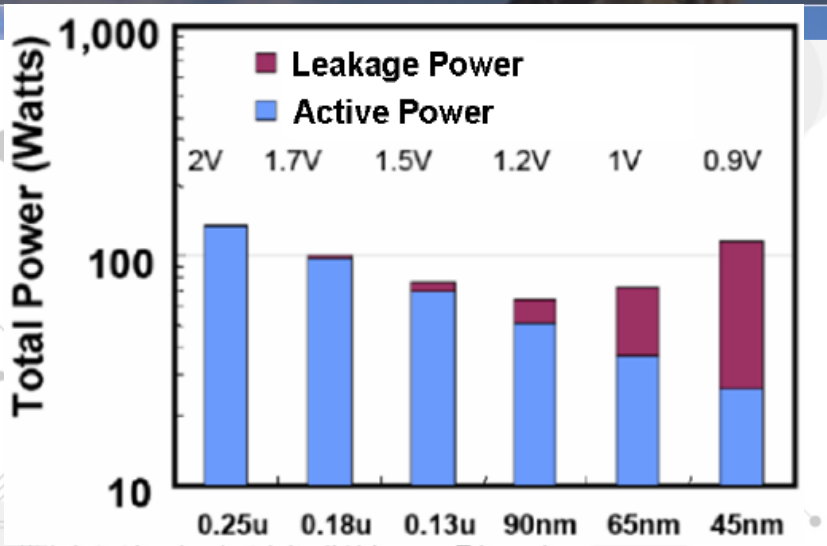
- Reduce Physical Gate Length (L_g)
- Reduce Threshold Voltage (V_T)
- Reduce Operating Voltage (V_{dd})

$$F_{max} = I_{DSAT} / (V_{DD} C_{ox})$$

$$Power = (V_{dd})^2 C_{ox} F_{max}$$

MOS: Traditional Scaling Limitations





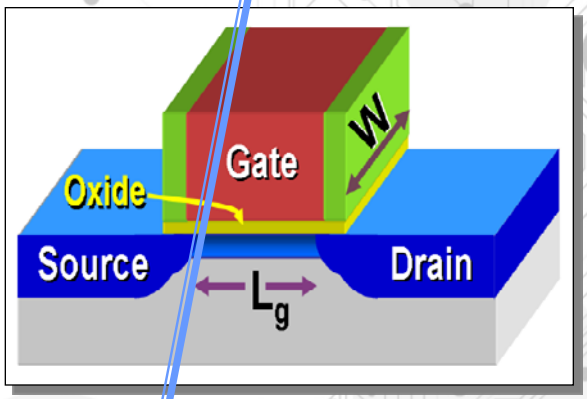
- **Leakage current:** Increasing off-state leakage I_g, I_{PT}, I_J (increases stand-by power)
- **Floating body:** Increasing body-factor due to charge build-up (V_T instability)
- **Parasitic:** Increasing junction resistance and capacitance (decreases performance)
- **Mobility:** Decreasing mobility due to higher channel doping (Lowers I_{Dsat})

Equivalent Scaling

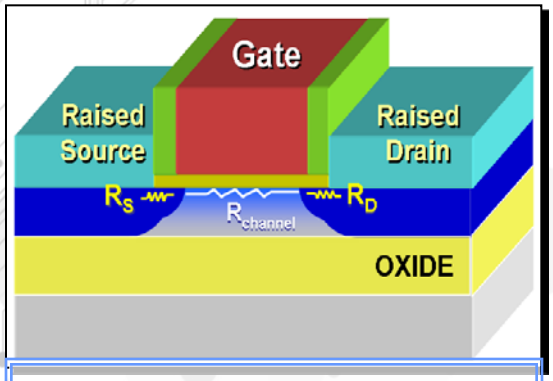
$$I_{Dsat} \approx \tfrac{1}{2} C_{ox} \mu (W/L_g)(V_G - V_T)^2$$

$= \varepsilon_o \varepsilon_s / T_{ox}$

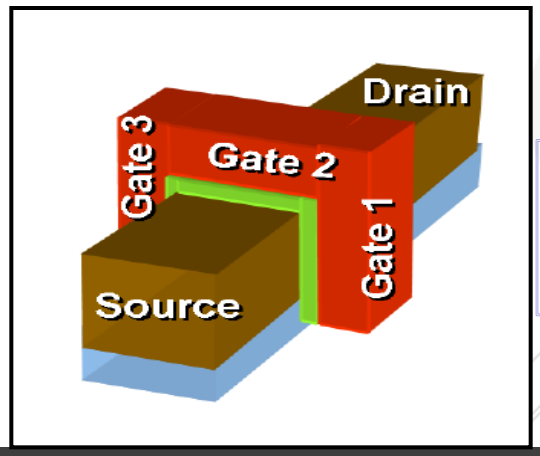
➢ Increase Gate Dielectric Constant (K)
→ New Material



➢ Increase Mobility (μ)
→ Strain



➢ Reduce parasitic capacitance and resistance
→ New Dev. Topology



➢ 3D (FinFET)
→ New Dev. Topology

Perguntas?