Tecnologia CMOS

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History Proceeds along Ages

280M

12M

Permian Triasic Jurassic Cretaceous Tertiary Quarternary

2.5M

3500BC

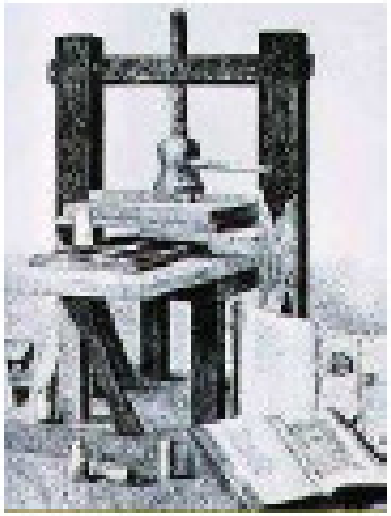
1500BC

Stone Bronze Iron

Old (Paleolithic) Middle (Mesolitic) New (Neolitic)

Tecnologias de informação

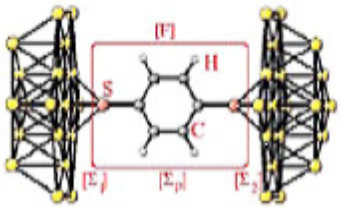
- Printing press (1456) – number of books jumped from 10,000 to 10 million in 50 yrs.
- Telegraph (1844)
- Radio (1895)
- Television (1936)
- Computers (1950s)
- Internet (1970s)
  - Huge extrasomatic storage: Well above brain storage



- Após ano 1945 aconteceu muito mais revolução tecnológica, do que revolução científica

- A informática só explodiu por causa da **tecnologia de silício**

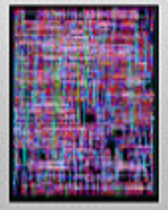
Design in the Late Silicon Age

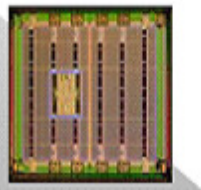


1950's

Late 2010's

Pre-silicon | Silicon | Post-silicon





70's

Late 90's

Early-Silicon | Silicon | Late-Silicon

The Custom Era

The ASIC Age

??

Definição da Informática

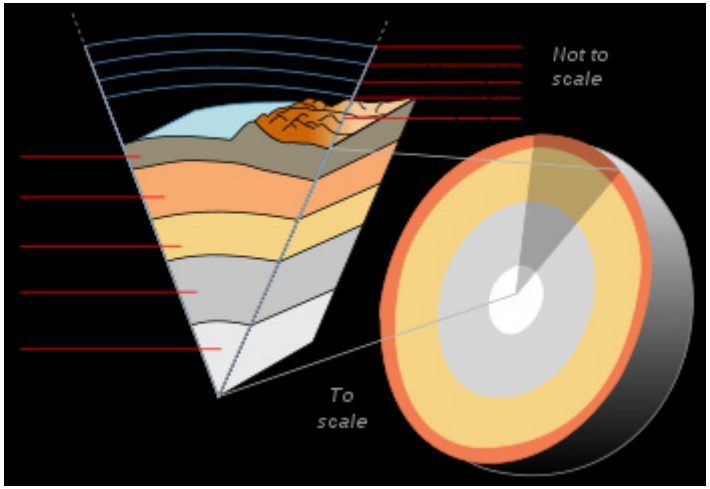
- Processamento de informação
- Armazenamento de informação
- Transmissão de informação

Características do Si

- Óxido nativo resistente
- Interface SiO_2/Si com poucos estados
- Resistência mecânica
- Abundância na crosta terrestre

Composição da Crosta terrestre

Óxidos	Percentagem
SiO_2	59.71
Al_2O_3	15.41
CaO	4.90
MgO	4.36
Na_2O	3.55
FeO	3.52
K_2O	2.80
Fe_2O_3	2.63
H_2O	1.52
TiO_2	0.60
P_2O_5	0.22
Total	99.22



MOSFET

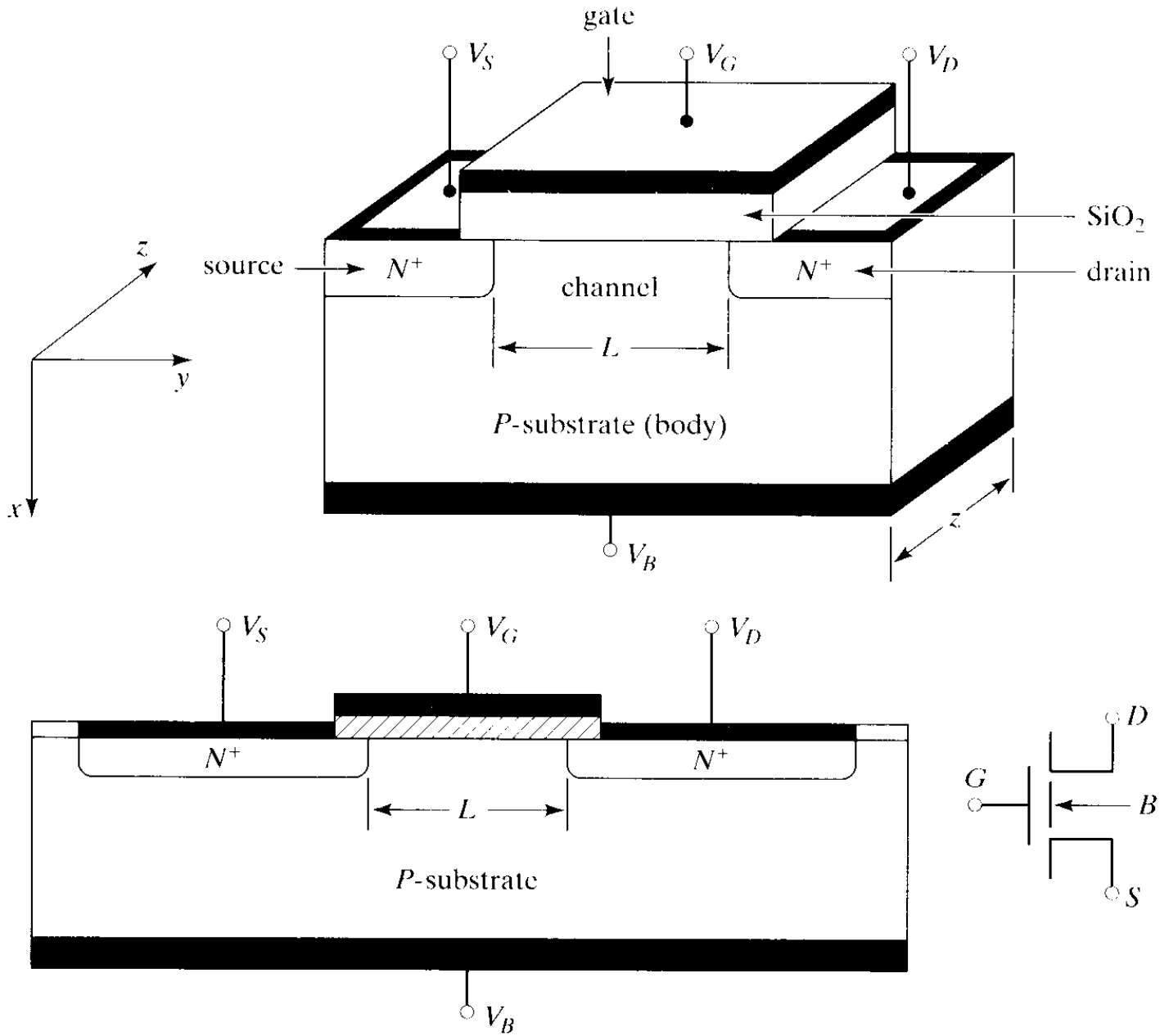
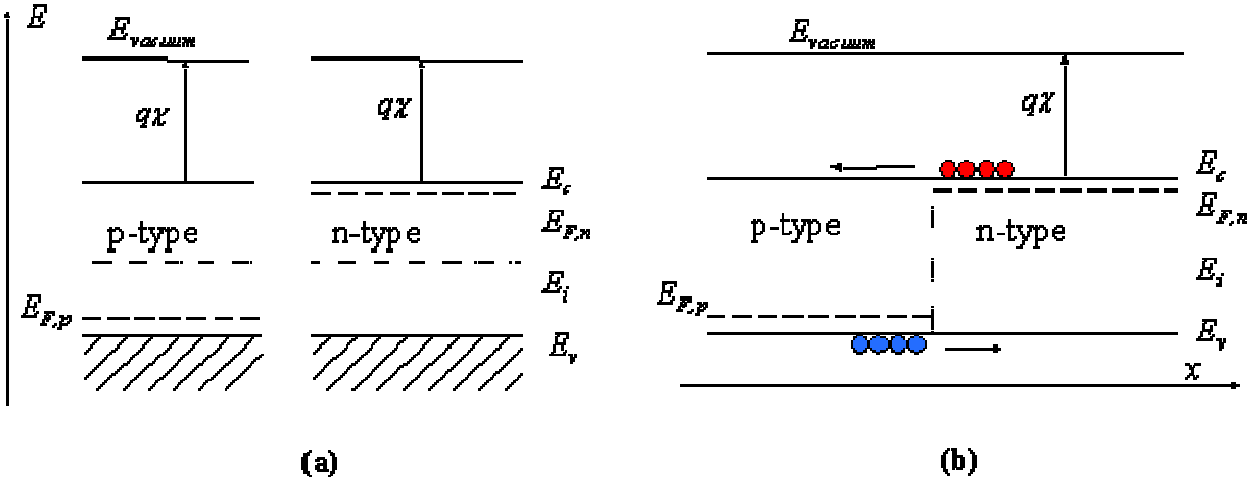
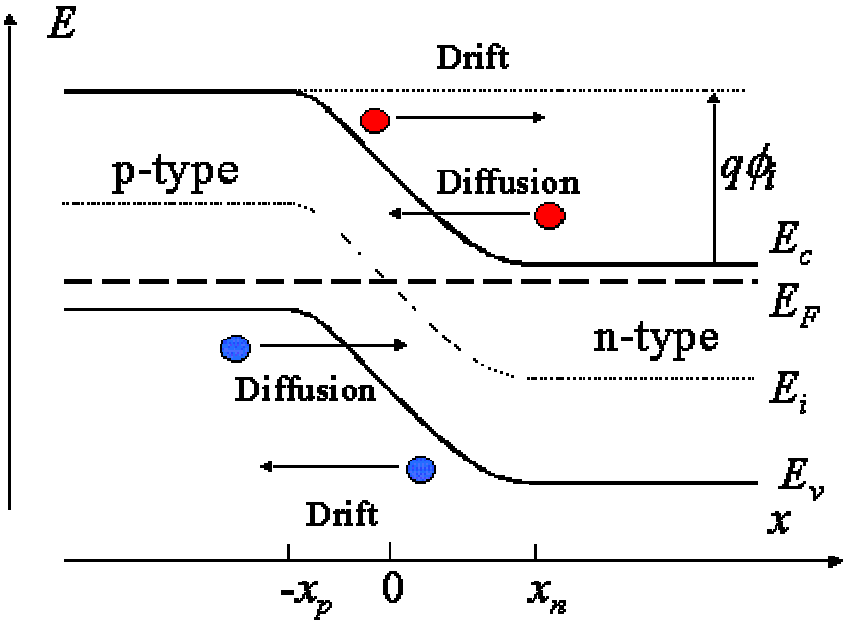


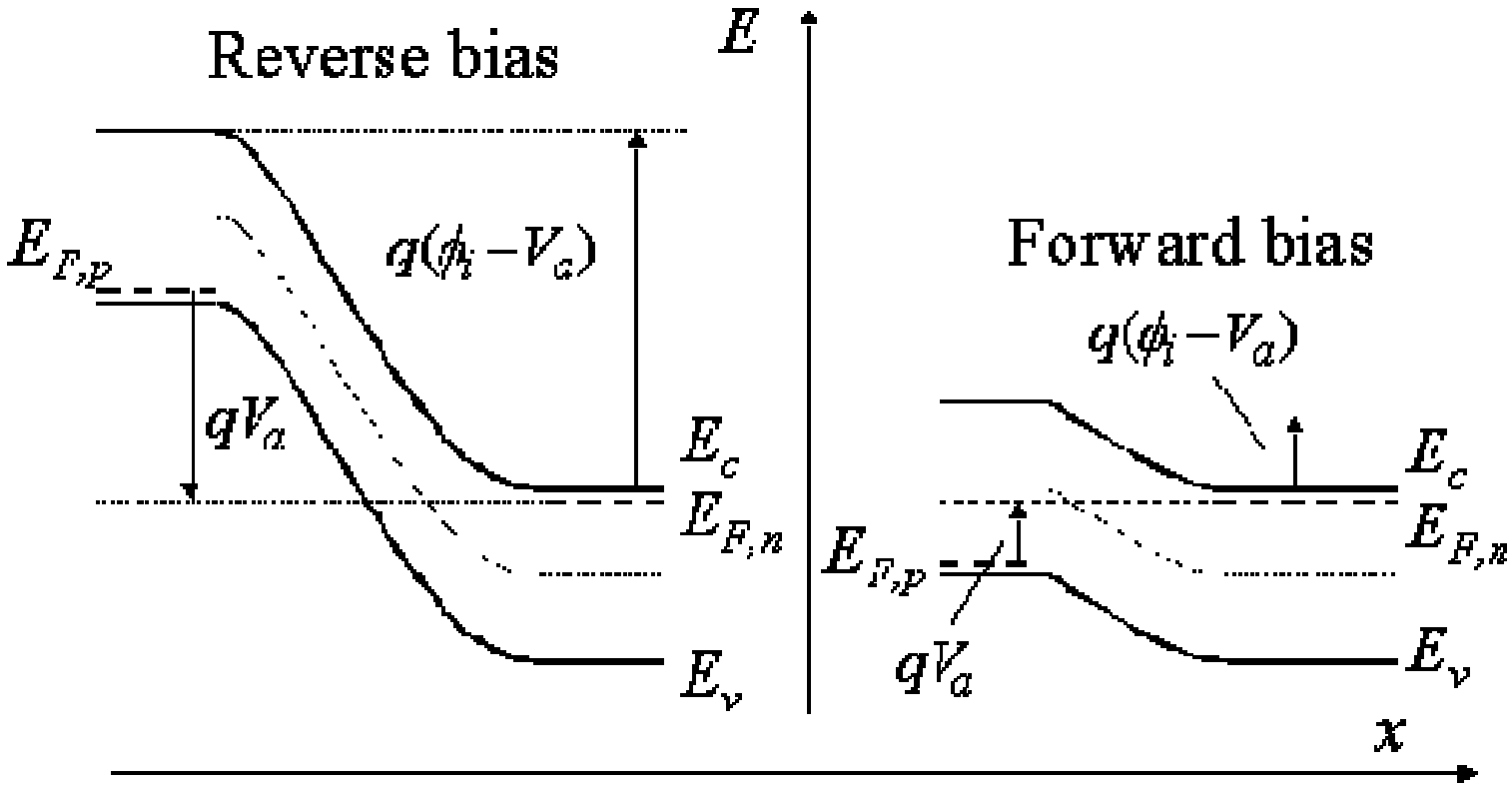
Figure 13.2 Perspective view, cross-section, and symbol of an N-channel MOSFET (NMOS).

Junção p-n


E
E_vacuum
qχ
E_c
E_F,n
p-type
n-type
E_i
E_F,p
E_v
x
(a)
(b)


E
Drift
p-type
Diffusion
qφ_i
E_c
E_F
n-type
Diffusion
E_i
E_v
Drift
x
-x_p
0
x_n

Junção p-n polarizada



Capacitor MOS

Estrutura MOS ideal

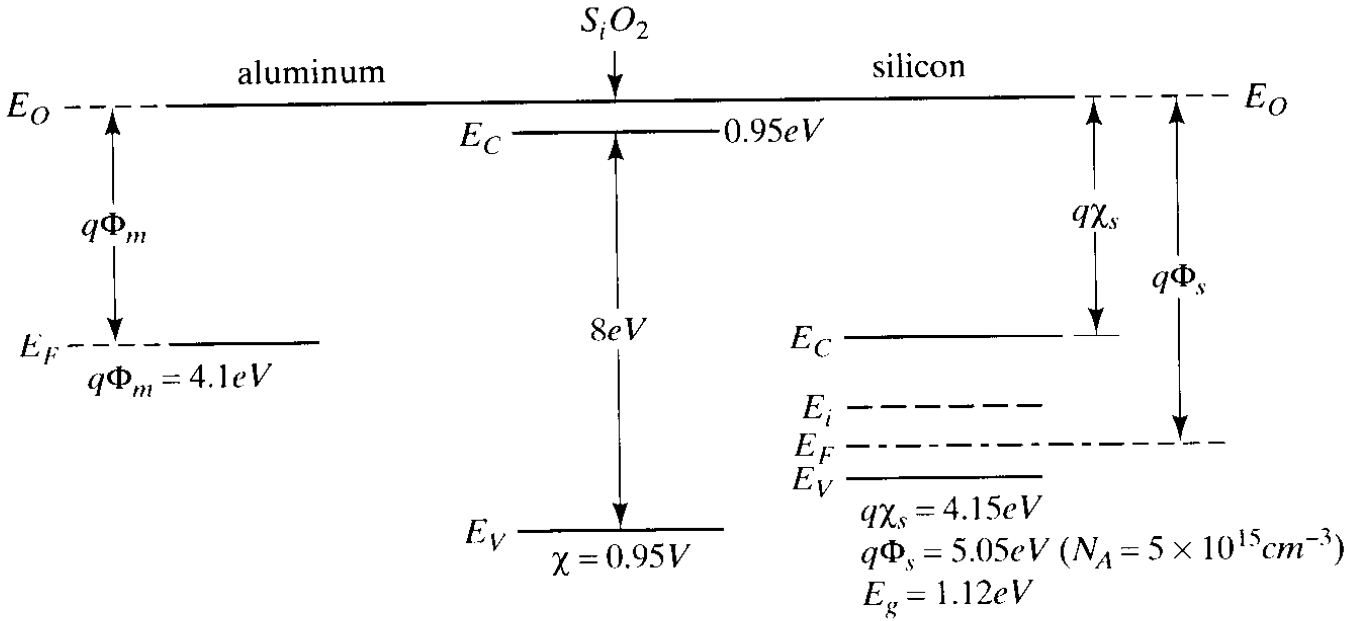


Figure 12.2 Energy level diagrams for aluminum, silicon dioxide, and P-silicon.

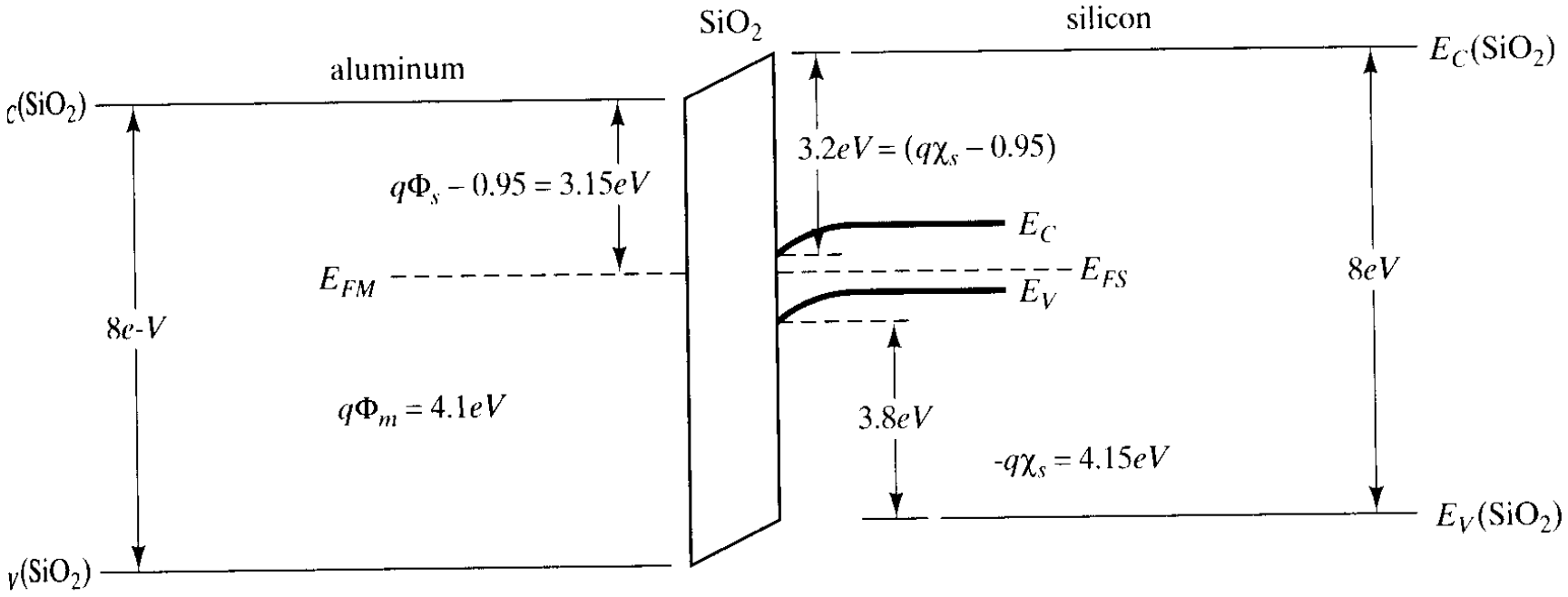
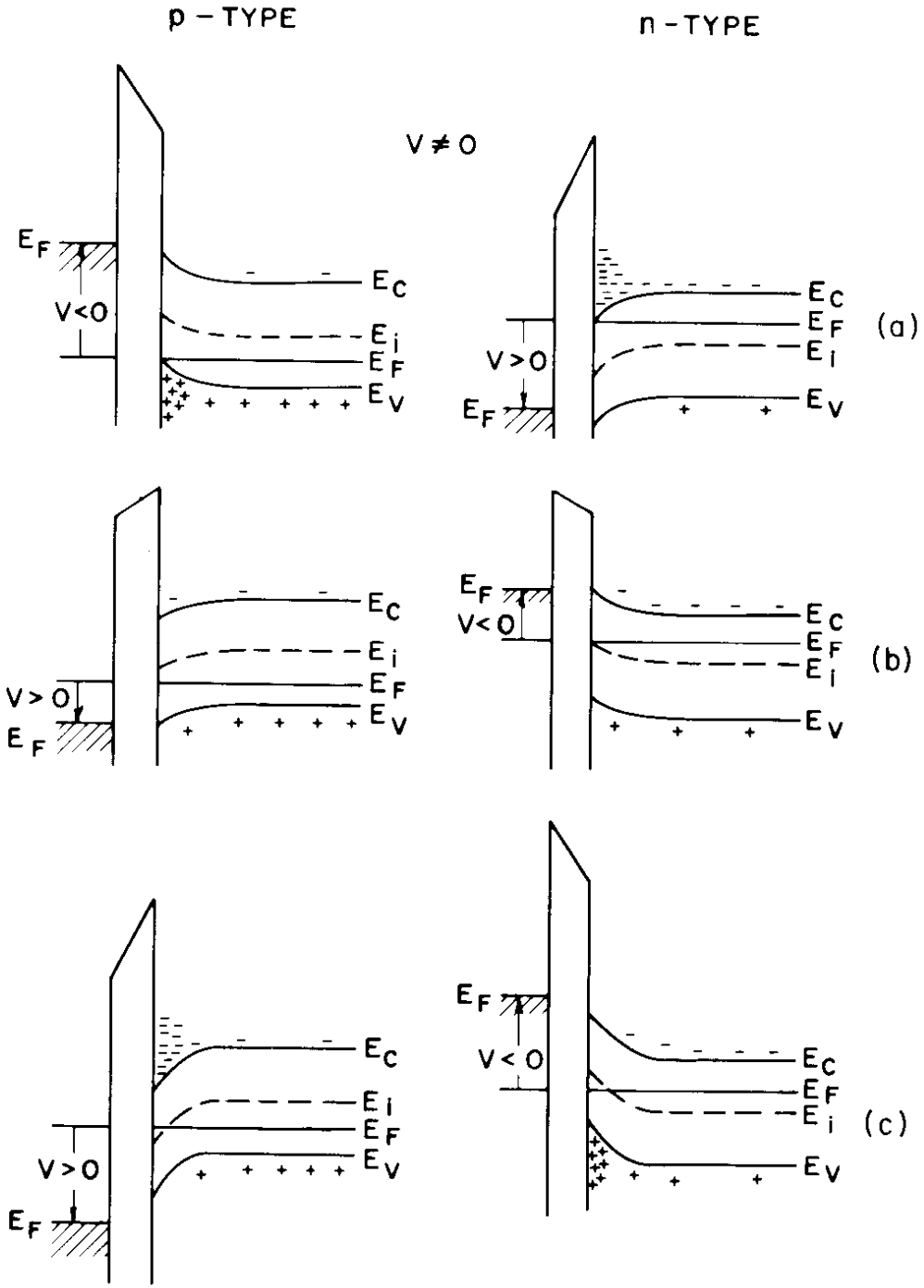
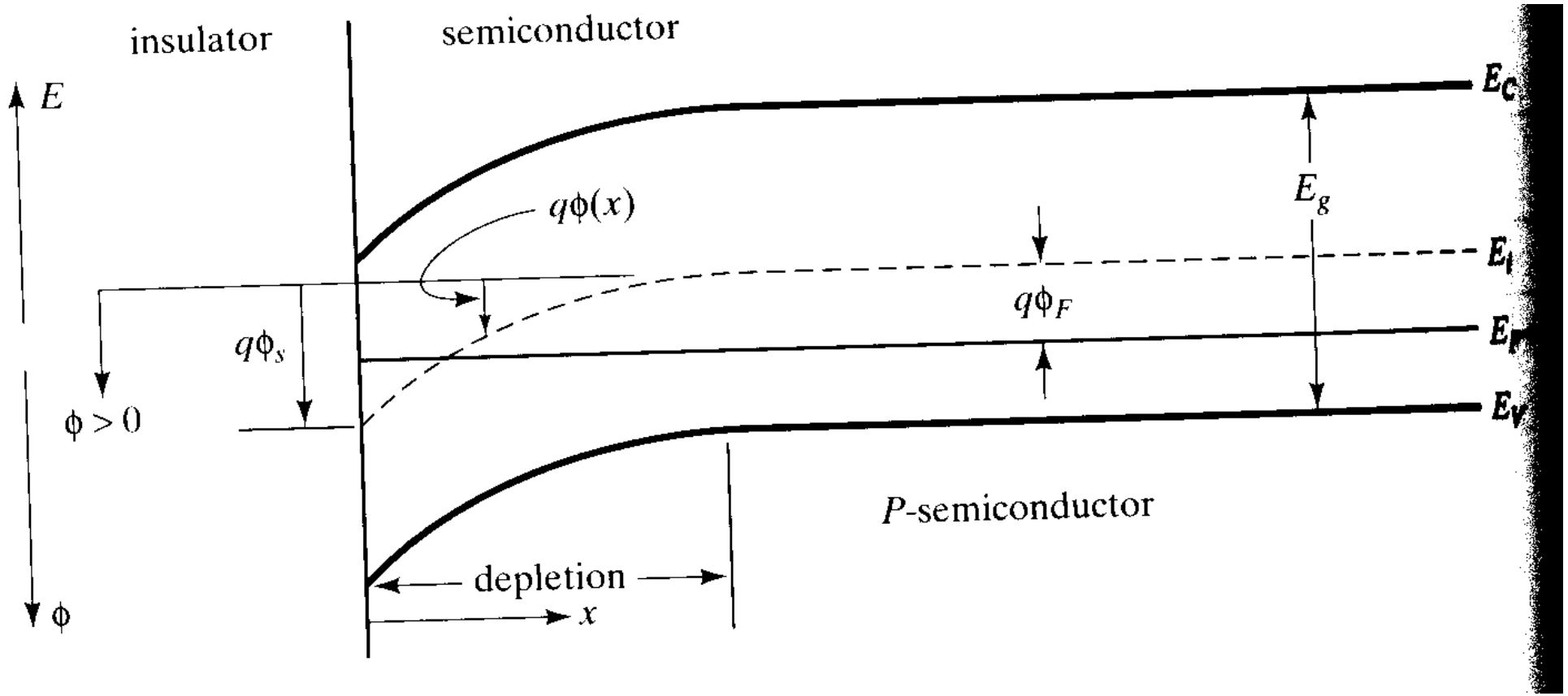


Figure 12.3 Energy level diagram after contact.


p – TYPE
n – TYPE
V ≠ 0
E_F
V<0
E_C
E_i
E_F
E_V
V>0
E_F
E_C
E_F
E_i
E_V
(a)
V>0
E_F
E_C
E_i
E_F
E_V
E_F
V<0
E_C
E_F
E_i
E_V
(b)
V>0
E_F
E_C
E_i
E_F
E_V
E_F
V<0
E_C
E_F
E_i
E_V
(c)

Surface Space-Charge Region



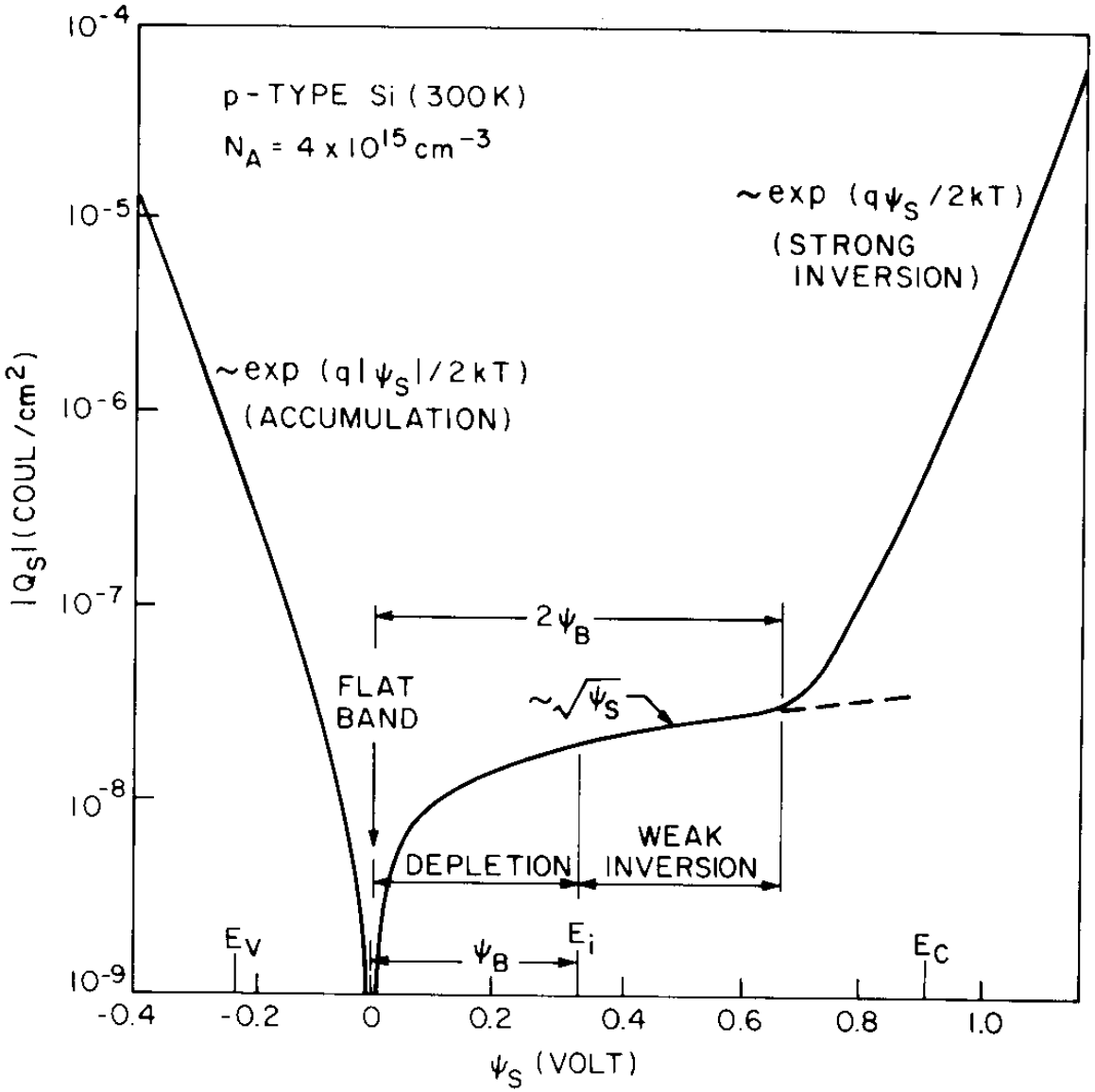
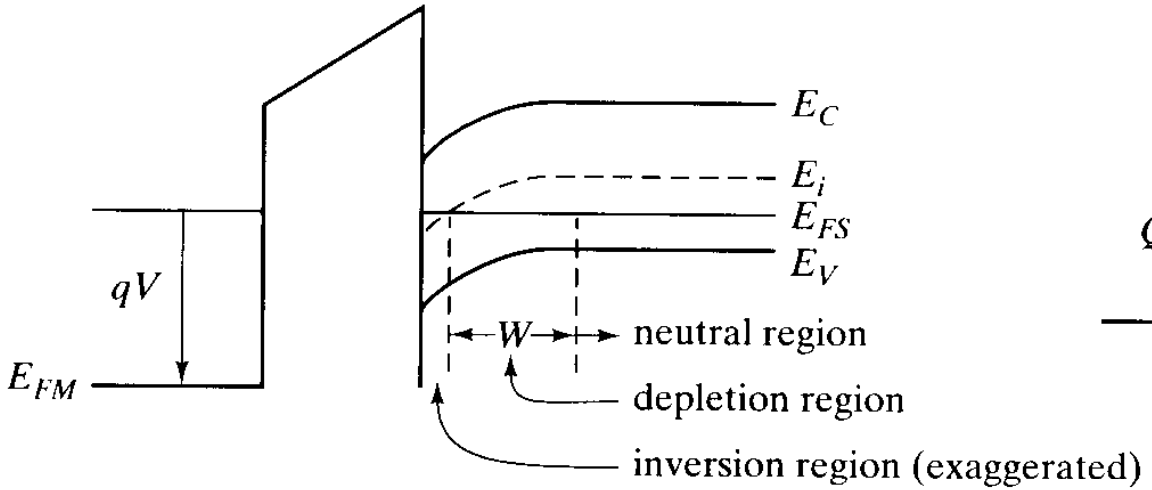
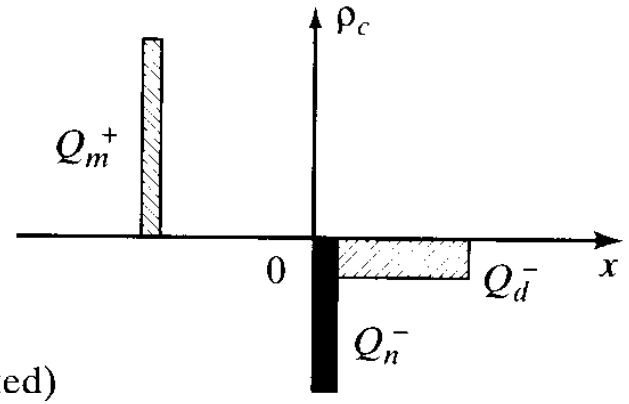


Fig. 5 Variation of space-charge density in the semiconductor as a function of the surface potential ψ_s for a *p*-type silicon with $N_A = 4 \times 10^{15}\,cm^{-3}$ at room temperature; ψ_B is the potential difference between the Fermi level and the intrinsic level of the bulk semiconductor. (After Garrett and Brattain, Ref. 13.)

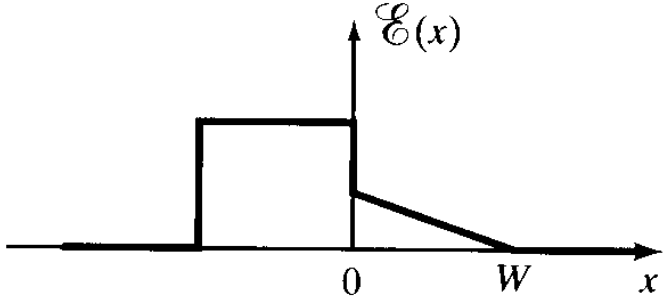
Cargas, campo e potencial



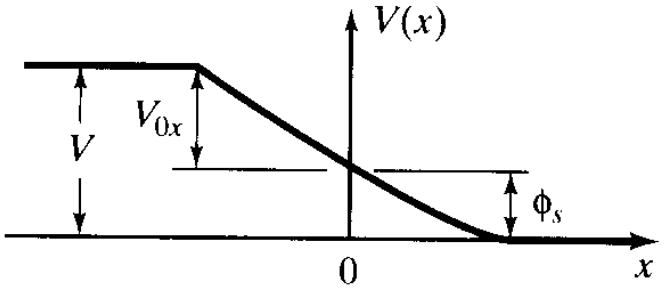
(a)



(b)



(c)



(d)

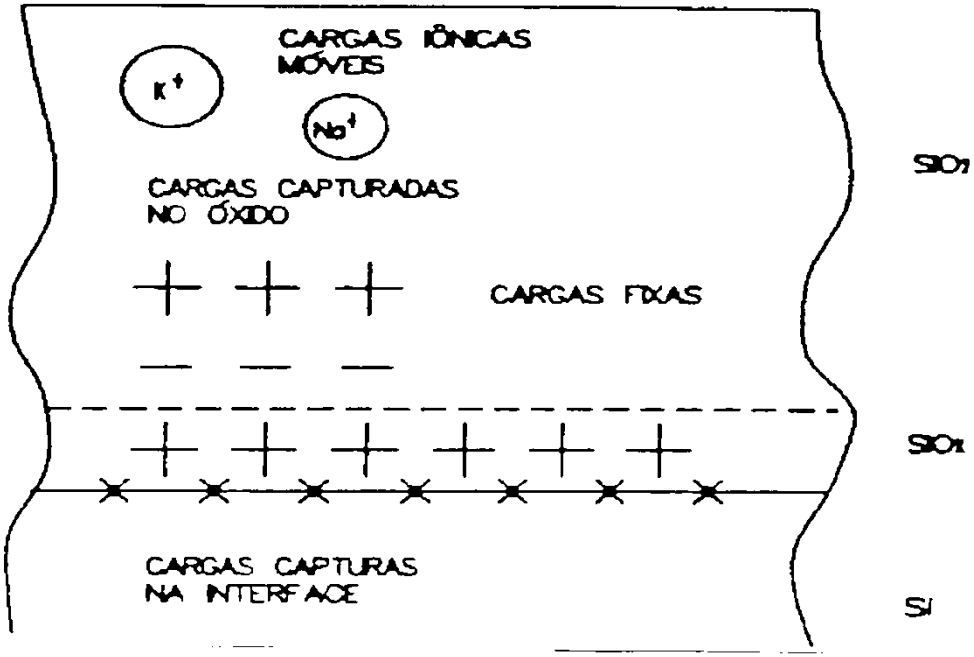


Figura A.7 - Cargas no Silício Termicamente Oxidado [10].

•Presença no óxido ou na interface óxido/semicondutor diminui a integridade do filme isolante e aumenta a instabilidade do comportamento dos dispositivos MOS, gera ruídos, aumenta as correntes de fuga das junções e da superfície, diminui a tensão de ruptura dielétrica, altera o potencial de superfície ψs, afeta a tensão de limiar V_t.

•Níveis aceitáveis de densidade de carga efetiva no óxido em circuitos ULSI são da ordem de 10^{10} cm^{-2}.

Q_m - CARGAS MÓVEIS (+ ou -) → 10^{10} a 10^{12} cm^{-2}

- íons dos metais alcalinos Na^+, K^+ e Li^+ e íons H^+ e H_3O^+.

INCORPORAÇÃO → ETAPAS DE PROCESSO EM AMBIENTES COM ESTES CONTAMINANTES

CARACTERÍSTICA → MOBILIDADE SOB AÇÃO DO CAMPO ELÉTRICO

Q_{ot} - CARGAS CAPTURADAS NO ÓXIDO (+ ou -) → 10^{9} a 10^{13} cm^{-2}

DEFEITOS NA ESTRUTURA DO ÓXIDO

INCORPORAÇÃO → ETAPAS DE PROCESSO COM RADIAÇÃO IONIZANTE

CARACTERÍSTICA → ELÉTRONS E LACUNAS CAPTURADOS EM POÇOS DE POTENCIAIS (DEFEITOS NA ESTRUTURA)

Q_f - CARGAS FIXAS NO ÓXIDO (+) → 10^{10} a 10^{12} cm^{-2}

INCORPORAÇÃO → IONIZAÇÃO DO ÁTOMO DE O → SiO_X
LIGADO A UM SÓ TETRAEDRO

CARACTERÍSTICA → DEPENDE DA ORIENTAÇÃO CRISTALINA
$Q_f(100) < Q_f(111)$

↓

ESTADOS LENTOS: SOB AÇÃO DO CAMPO ELÉTRICO
RESPONDEM MUITO LENTAMENTE

Q_{it} - CARGAS CAPTURADAS NA INTERFACE → 10^{10} eV^{-1} cm^{-2}

INCORPORAÇÃO →
- DEFORMAÇÃO ABRUPTA DA ESTRUTURA DO Si
- LIGAÇÃO INSATURADA
- IMPUREZAS METÁLICAS

CARACTERÍSTICA → APARECIMENTO DE ESTADOS QUÂNTICOS
NA BANDA PROIBIDA

↓

ESTADOS RÁPIDOS: TEMPO DE RESPOSTA DE μs
SOB AÇÃO DO CAMPO ELÉTRICO

TRATAMENTO DAS CARGAS

Q_m →
- LIMPEZA DOS TUBOS COM Cl
- OXIDAÇÃO COM Cl
- LIMPEZA DE LÂMINAS

Q_{ot} →
- TRATAMENTO TÉRMICO A 450ºC EM FORMING-GAS (N_2 E H_2)

Q_f →
- TRATAMENTO TÉRMICO EM ALTA TEMPERATURA EM N_2

Q_{it} →
- TRATAMENTO TÉRMICO A 450ºC EM FORMING-GAS (N_2 E H_2)

Processos de fabricação de dispositivos na tecnologia planar do silício

Crescimento epitaxial

Difusão

Oxidação térmica

Implantação iônica

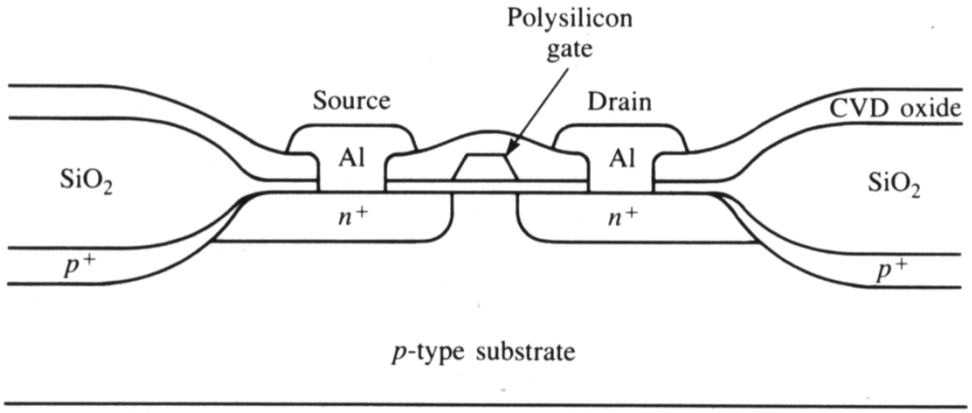
Recozimento

Foto litografia

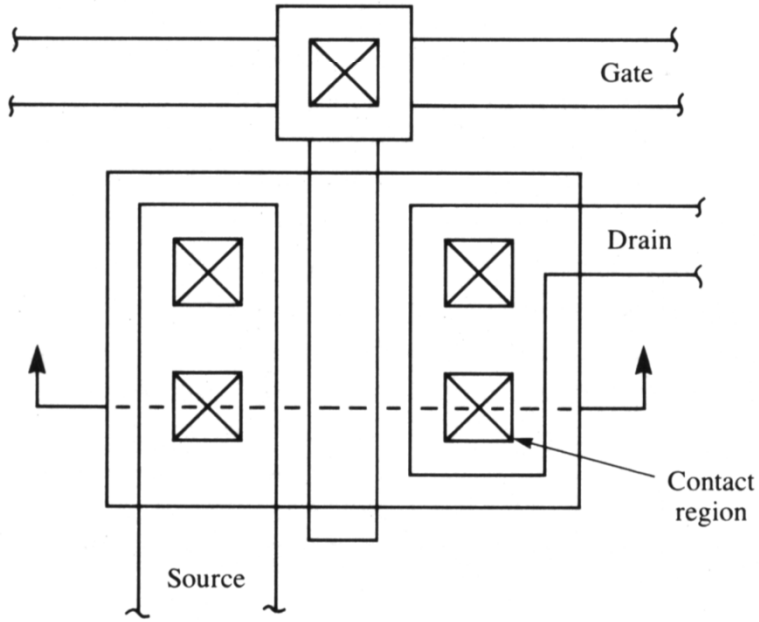
Deposição de filmes

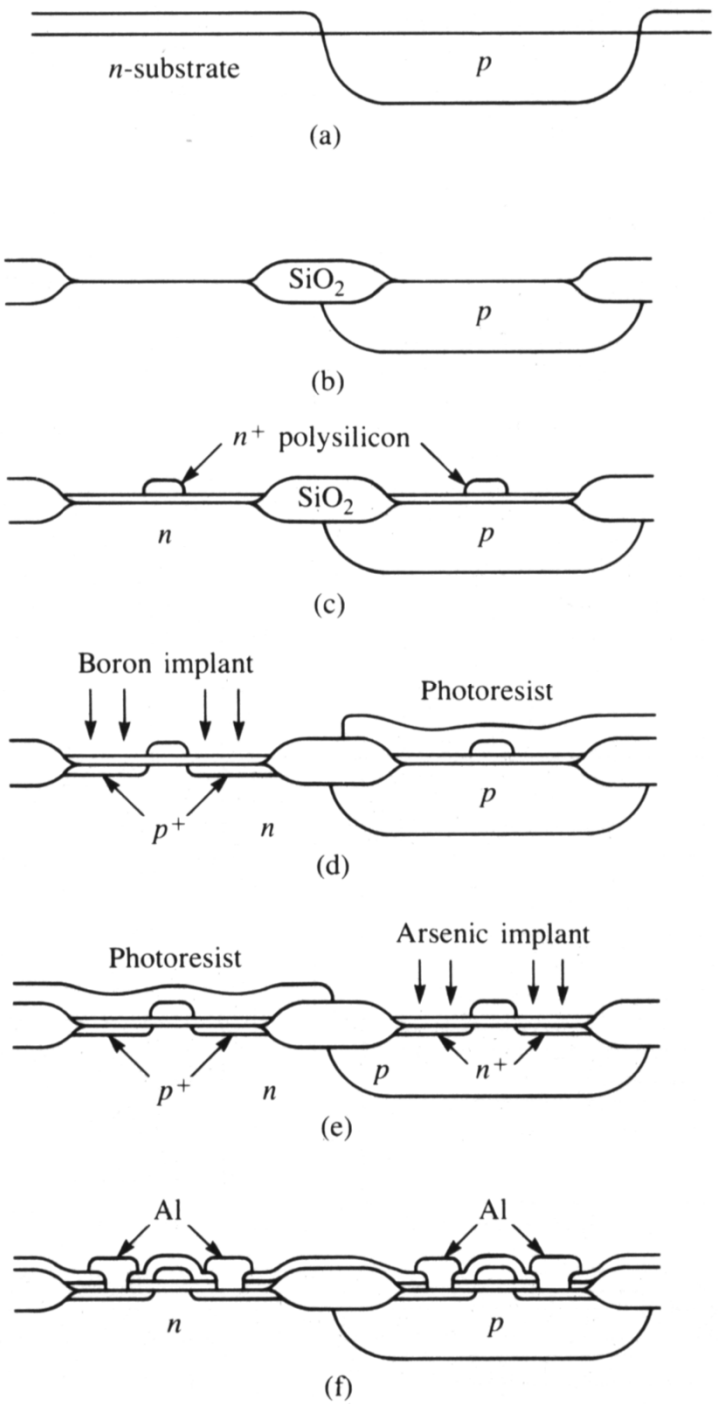
Ataques úmidos e por plasma, limpezas

NMOS

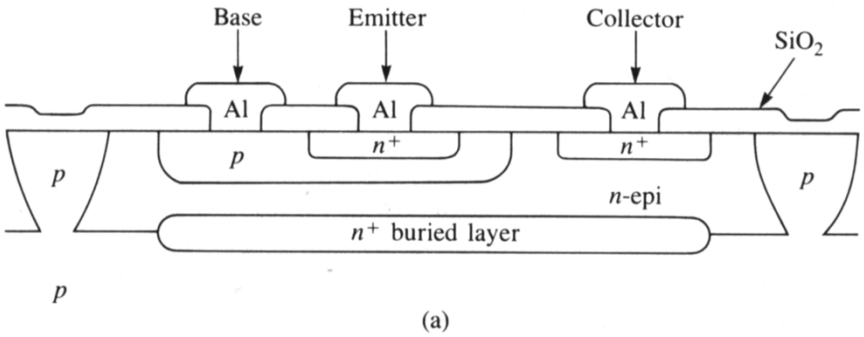

Polysilicon
gate
Source
Drain
CVD oxide
Al
Al
SiO_2
SiO_2
n^+
n^+
p^+
p^+
p-type substrate

(a)

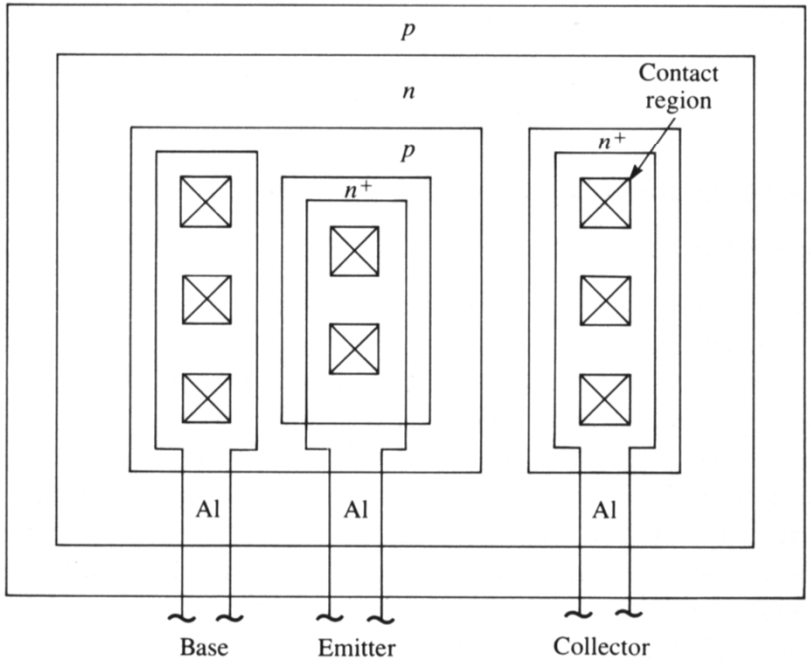

Gate
Drain
Contact
region
Source


n-substrate
p
(a)
SiO2
p
(b)
n+ polysilicon
SiO2
n
p
(c)
Boron implant
Photoresist
p+
n
p
(d)
Photoresist
Arsenic implant
p+
n
p
n+
(e)
Al
Al
n
p
(f)

CMOS

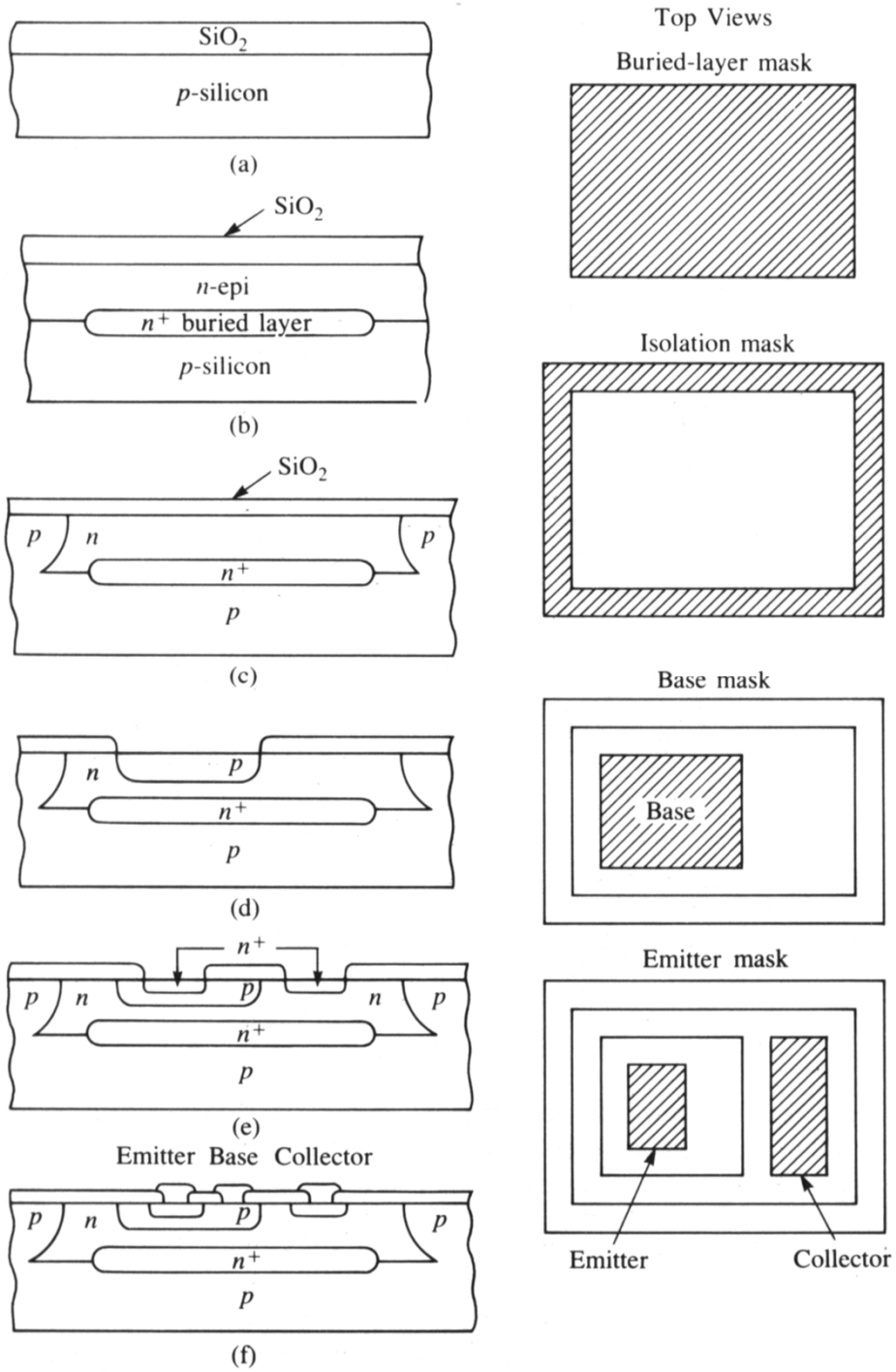

Base
Emitter
Collector
SiO_2
Al
Al
Al
n^+
n^+
p
p
p
p
n-epi
n^+ buried layer
p

(a)


p
n
Contact region
p
n^+
n^+
Al
Al
Al
Base
Emitter
Collector

(b)

bipolar


SiO2
p-silicon
(a)
SiO2
n-epi
n+ buried layer
p-silicon
(b)
SiO2
p
n
p
n+
p
(c)
n
p
n+
p
(d)
n+
p
n
p
n
p
n+
p
(e)
Emitter Base Collector
p
n
p
p
n+
p
(f)
Top Views
Buried-layer mask
Isolation mask
Base mask
Base
Emitter mask
Emitter
Collector

bipolar

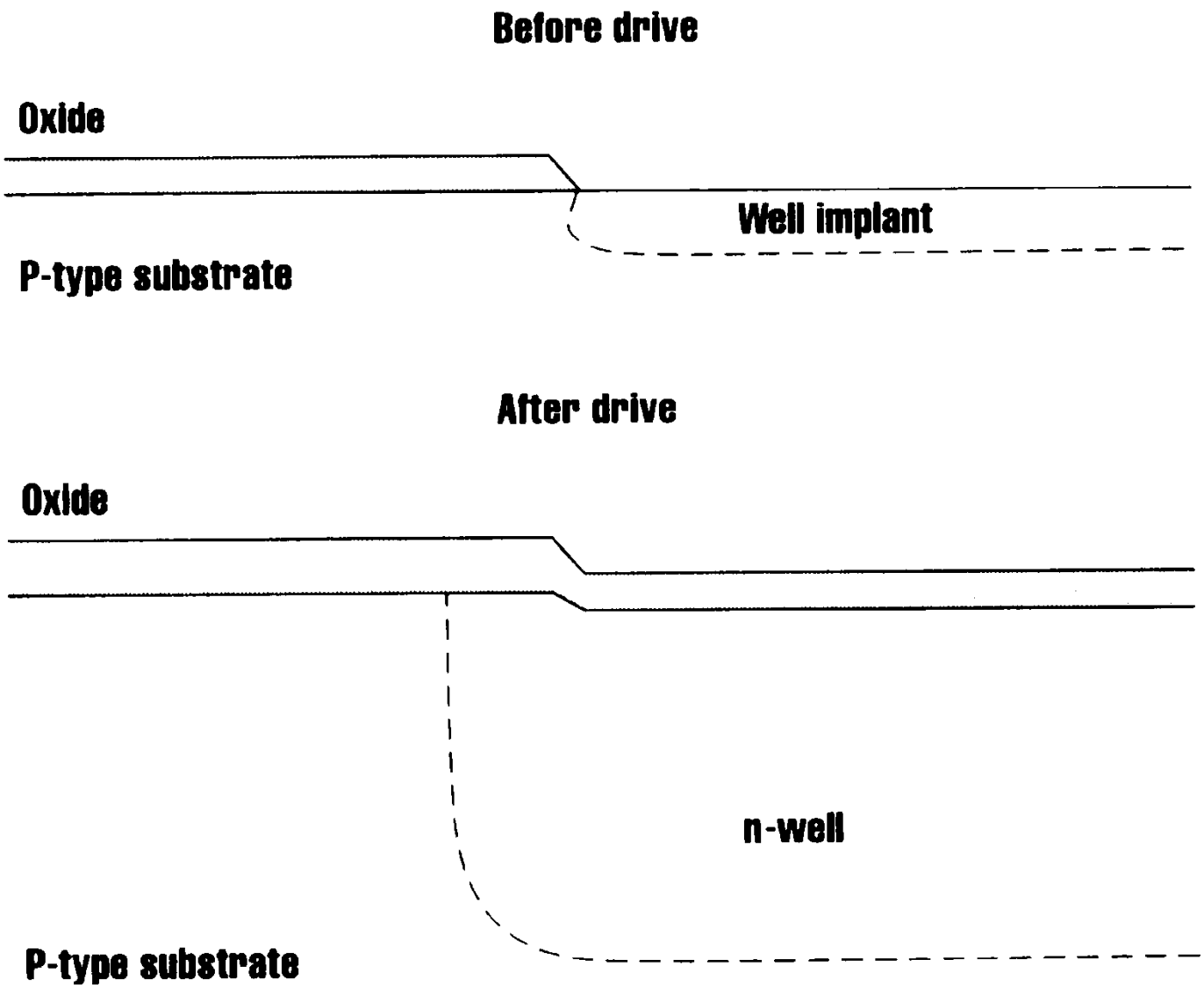


Figure 16-4 Cross-sectional views of an inverter structure after well drive.

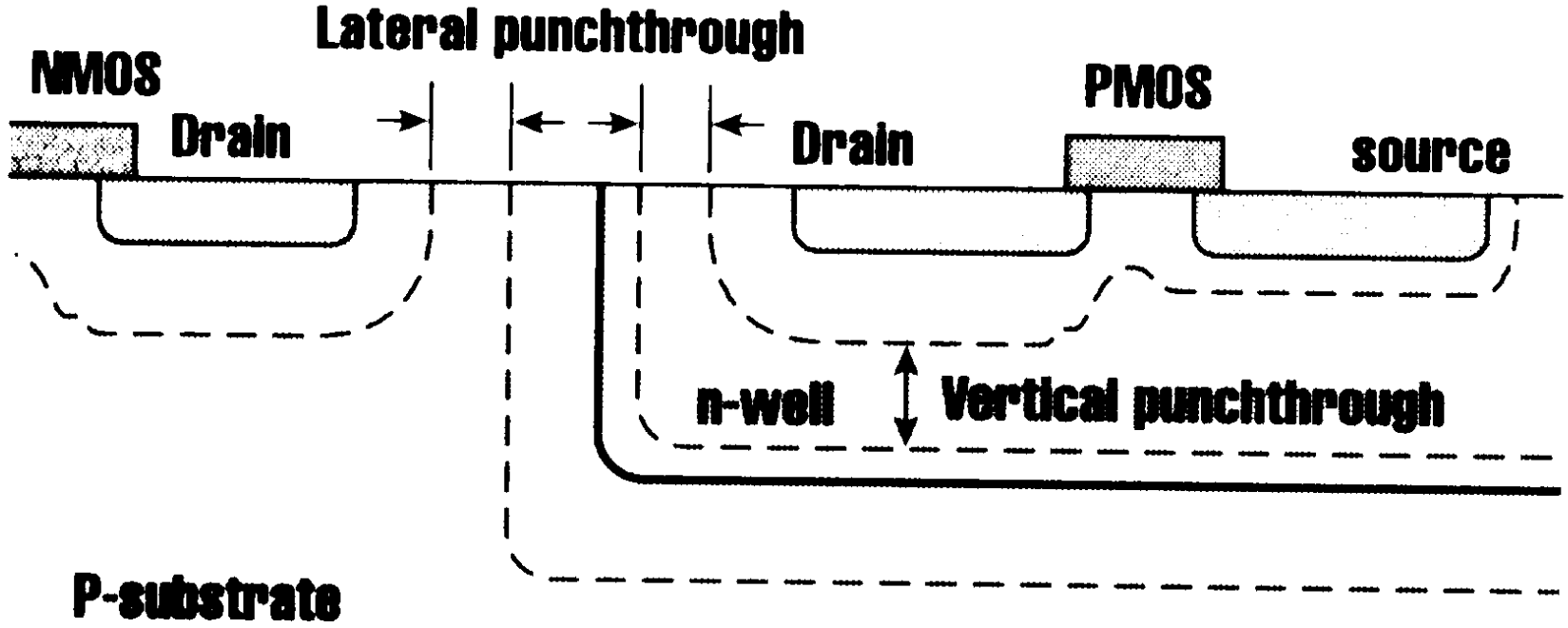


Figure 16-5 The minimum well depth must be chosen so as to prevent punchthrough from the reverse biased source/well and source/substrate junctions.

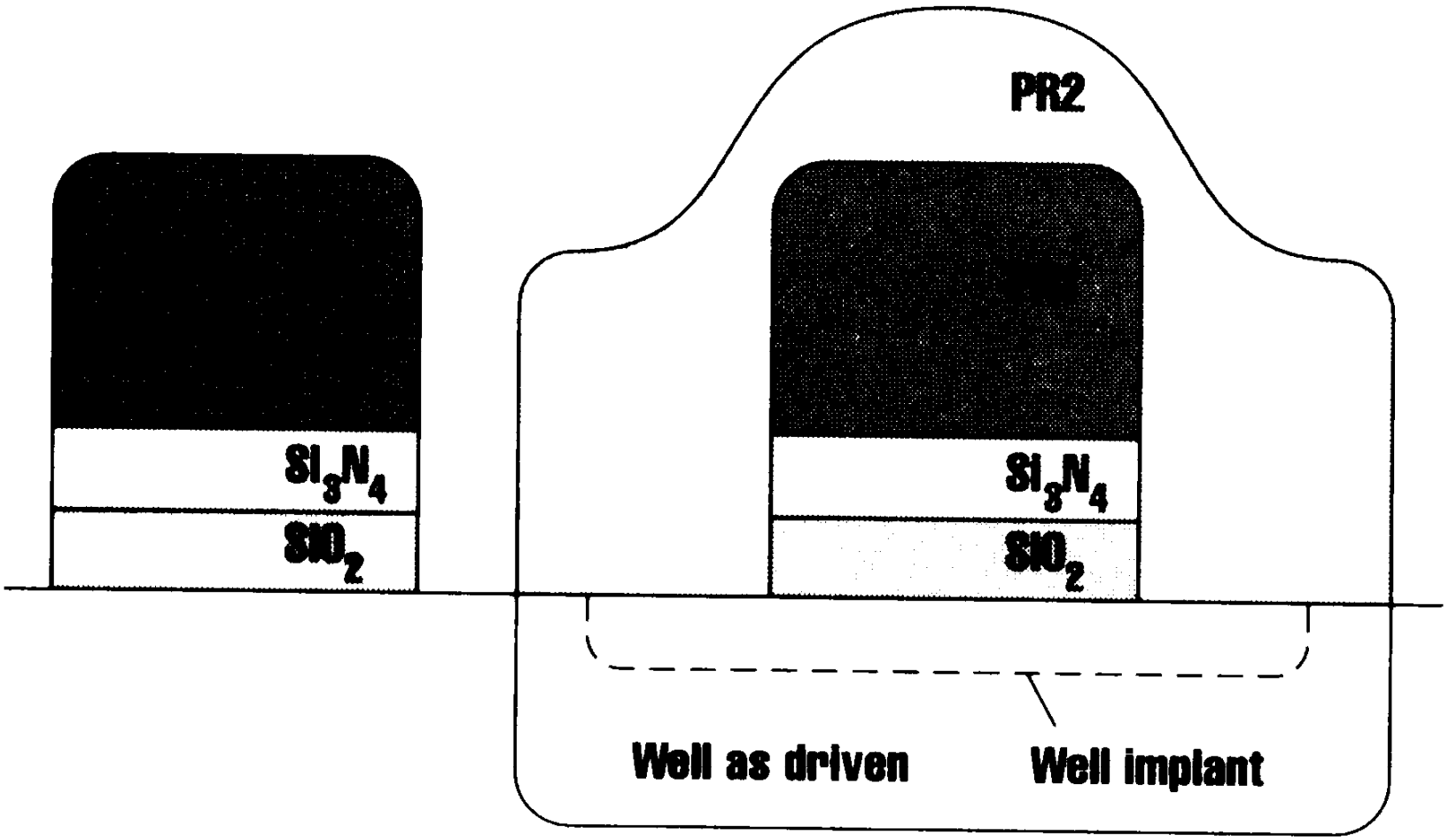


Figure 16-6 The field implant mask is the inverse of the well, but the features are bloated to account for lateral diffusion.

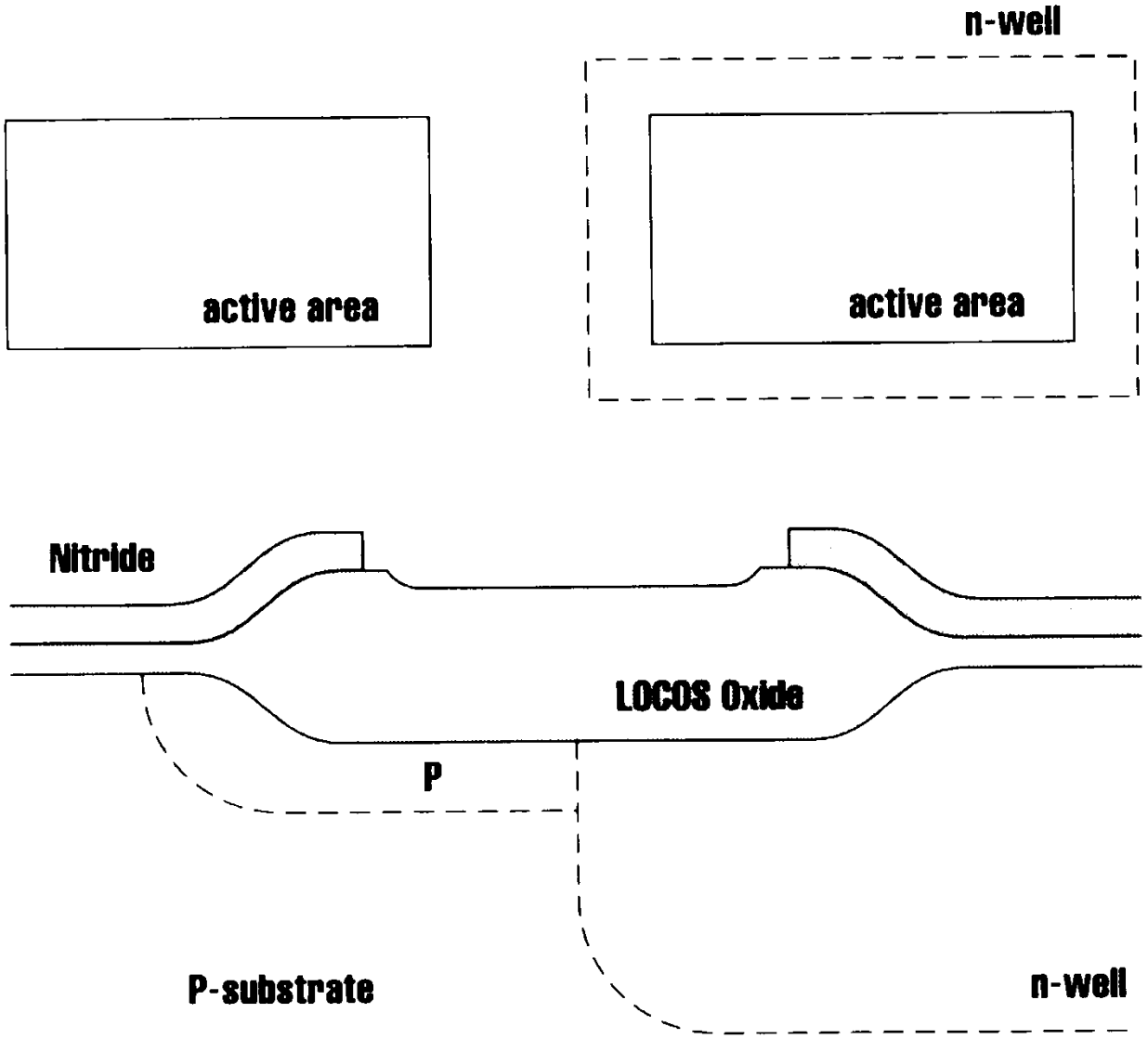


Figure 16-7 Top and cross-sectional views of a CMOS inverter after field oxidation.

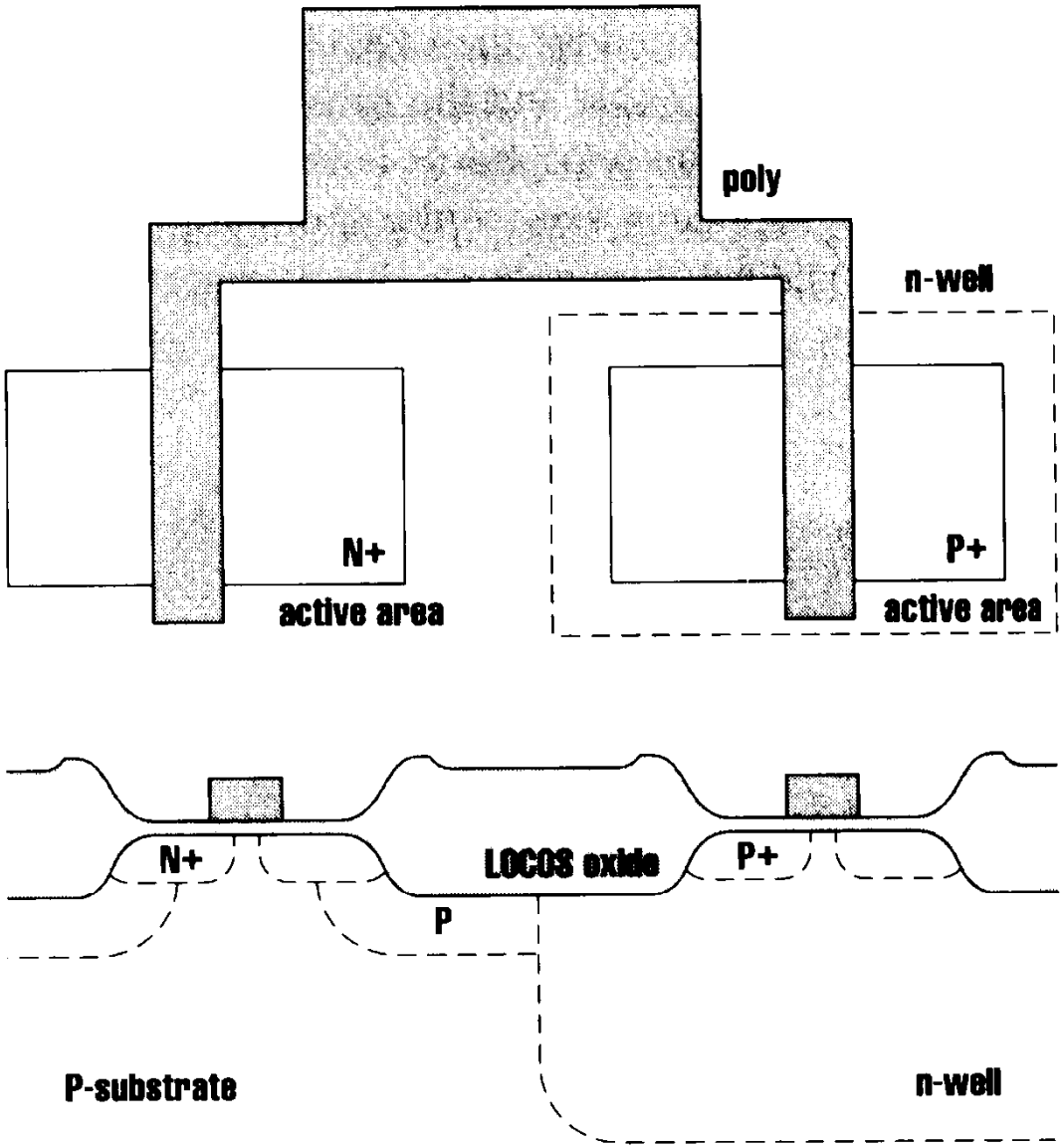


Figure 16-8 Top and cross-sectional views of a CMOS inverter after source/drain implants.

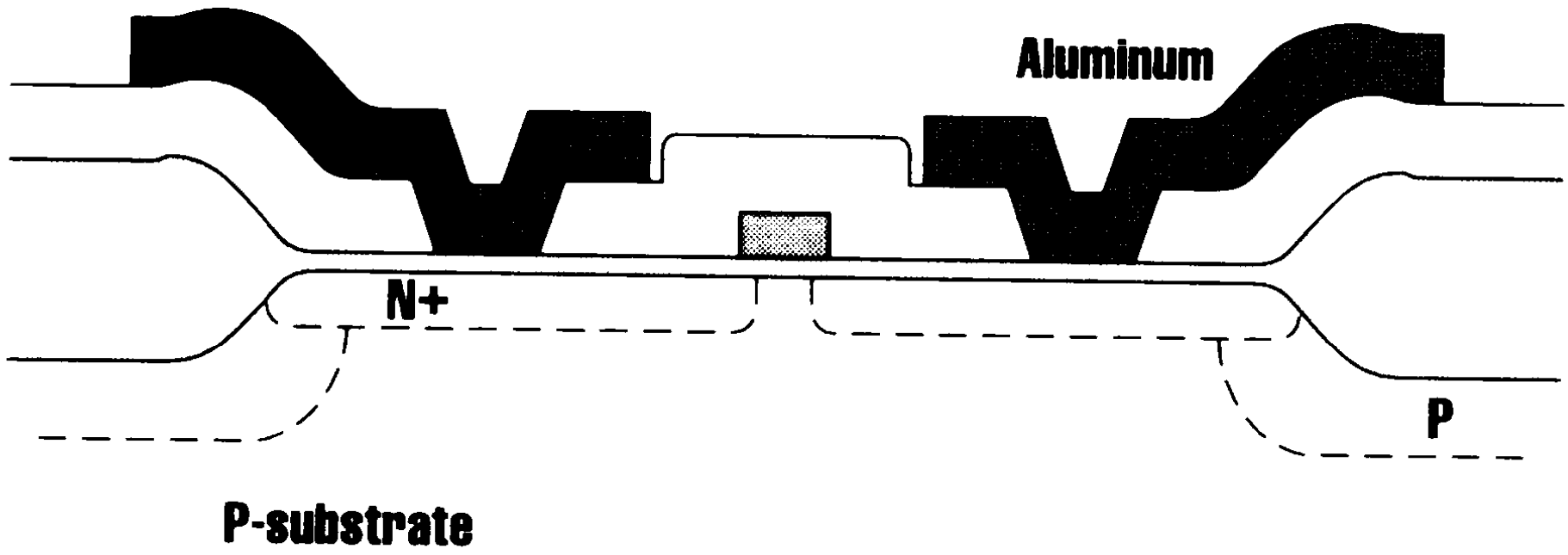


Figure 16-9 Top and cross-sectional views of a CMOS inverter after PSG deposition and reflow and metallization

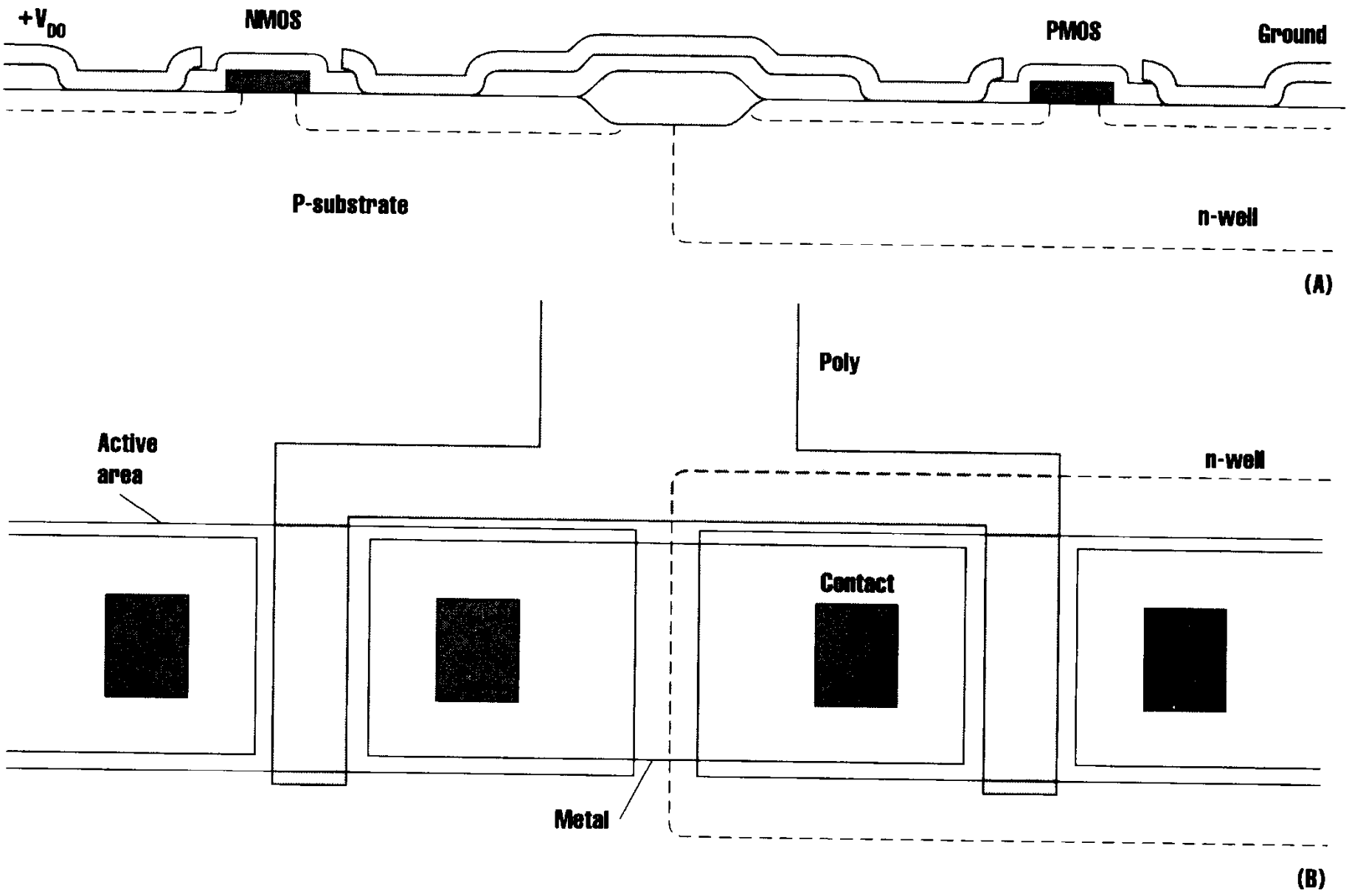


Figure 16-10 Top and cross-sectional views of a completed CMOS inverter fabricated with a simple 3 μm process.

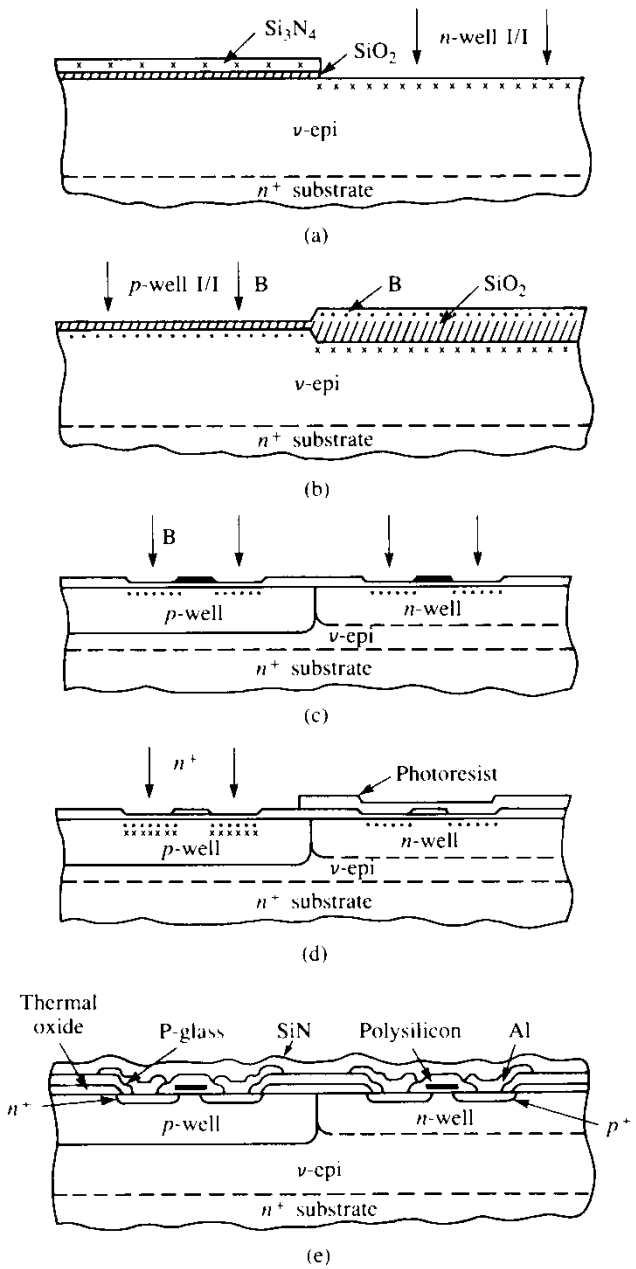
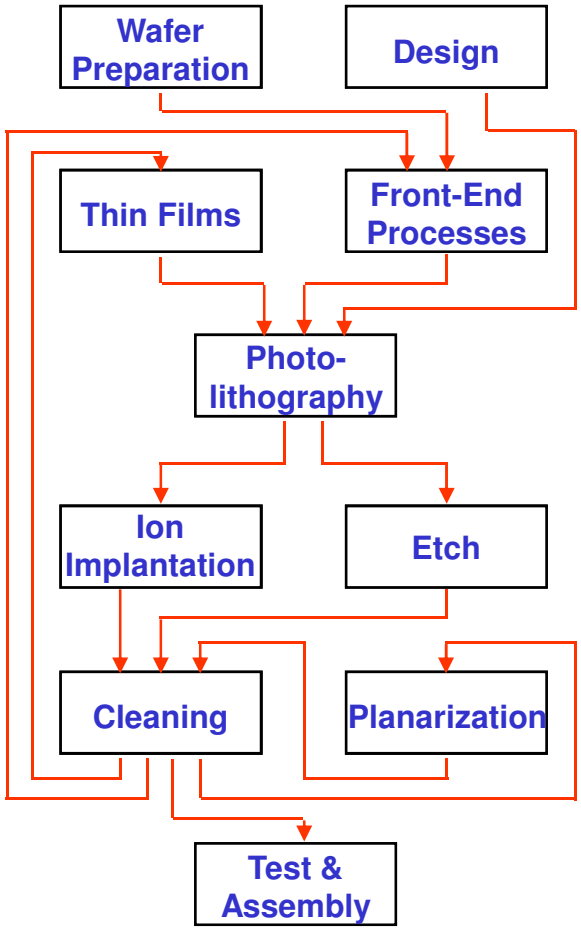


Fig. 9.15 Twin-well CMOS structure at several stages of the process. (a) n-well ion implant; (b) p-well implant; (c) nonselective p^+ source/drain implant; (d) selective n^+ source/drain implant using photoresist mask; (e) final structure. Copyright 1980 IEEE. Reprinted with permission from ref. [10].

Semiconductor Manufacturing Processes

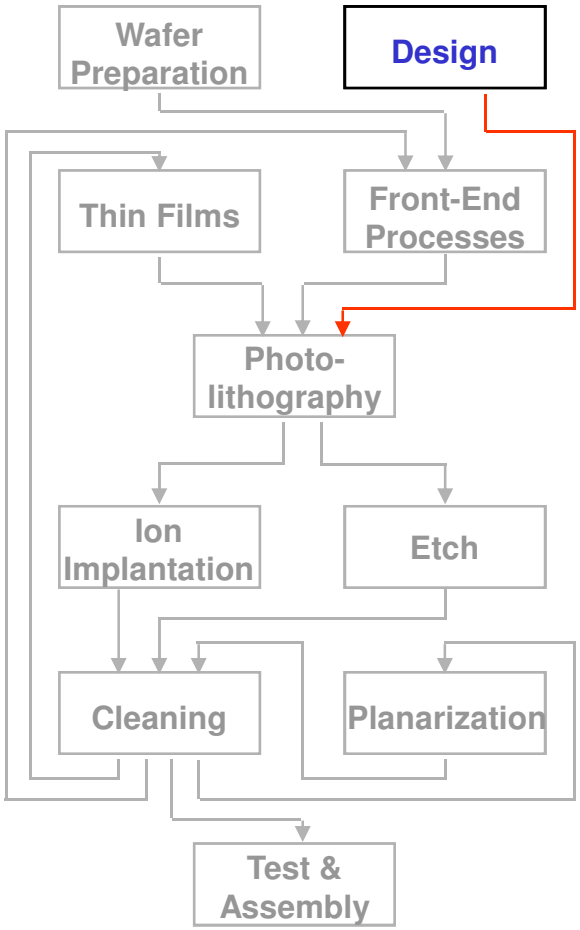
Semiconductor Manufacturing Processes

- Design
- Wafer Preparation
- Front-end Processes
- Photolithography
- Etch
- Cleaning
- Thin Films
- Ion Implantation
- Planarization
- Test and Assembly

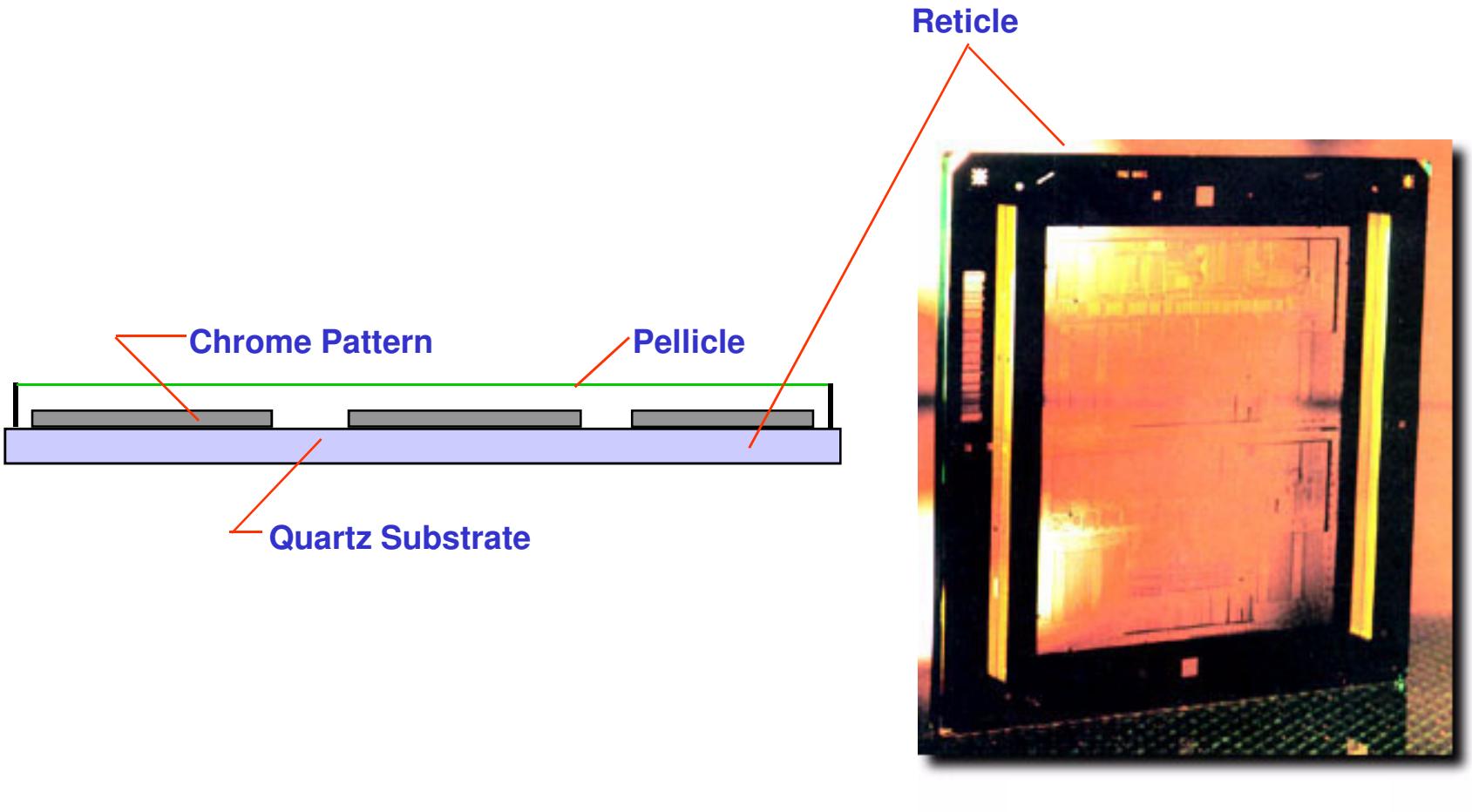


Design

- Establish Design Rules
- Circuit Element Design
- Interconnect Routing
- Device Simulation
- Pattern Preparation

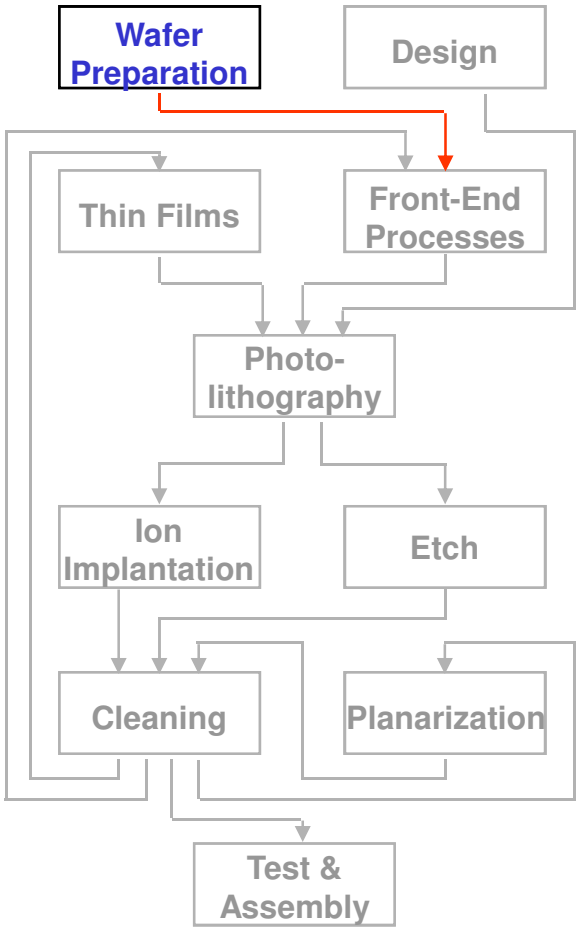


Pattern Preparation



Wafer Preparation

- Polysilicon Refining
- Crystal Pulling
- Wafer Slicing & Polishing
- Epitaxial Silicon Deposition



Polysilicon Refining

Chemical Reactions

Silicon Refining: $SiO_2 + 2\ C \rightarrow Si + 2\ CO$

Silicon Purification: $Si + 3\ HCl \rightarrow HSiCl_3 + H_2$

Silicon Deposition: $HSiCl_3 + H_2 \rightarrow Si + 3\ HCl$

Reactants

H_2

Silicon Intermediates

H_2SiCl_2

$HSiCl_3$

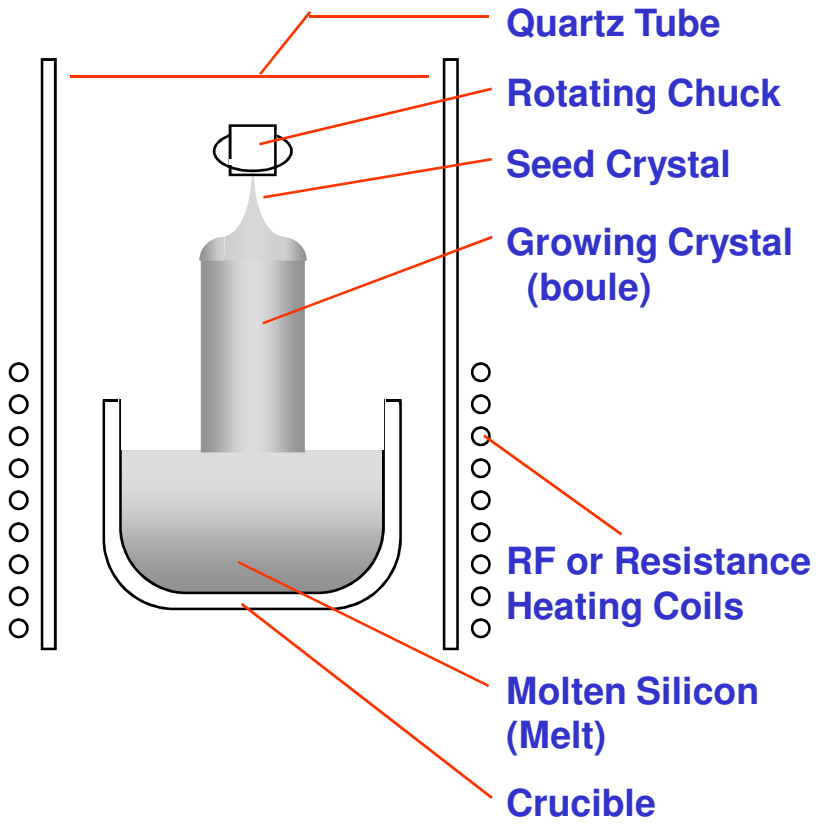
Crystal Pulling

Process Conditions

Flow Rate: 20 to 50 liters/min
Time: 18 to 24 hours
Temperature: >1,300 degrees C
Pressure: 20 Torr

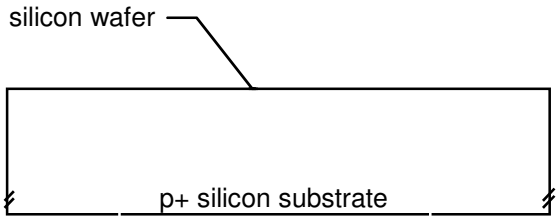
Materials

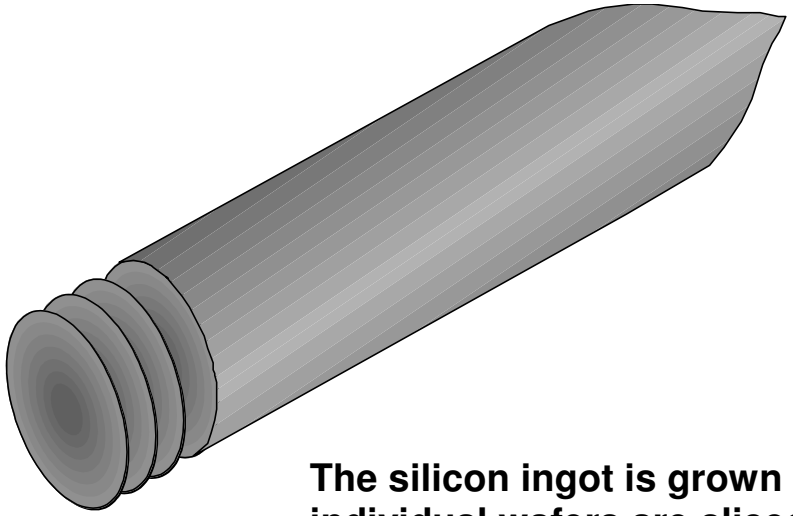
Polysilicon Nodules *
Ar *
H_2



* High proportion of the total product use

Wafer Slicing & Polishing

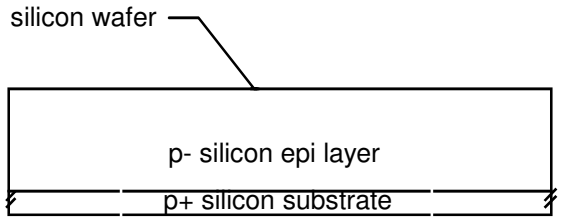




The silicon ingot is grown and individual wafers are sliced.

The silicon ingot is sliced into individual wafers, polished, and cleaned.

Epitaxial Silicon Deposition



Chemical Reactions

Silicon Deposition: $HSiCl_3 + H_2 \rightarrow Si + 3\ HCl$

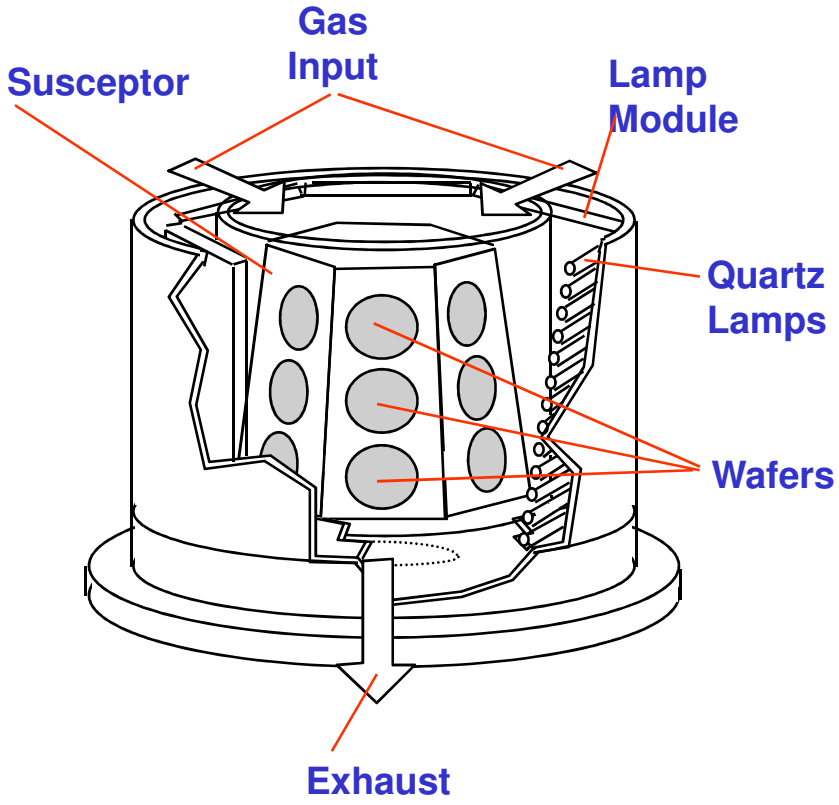
Process Conditions

Flow Rates: 5 to 50 liters/min

Temperature: 900 to 1,100 degrees C.

Pressure: 100 Torr to Atmospheric

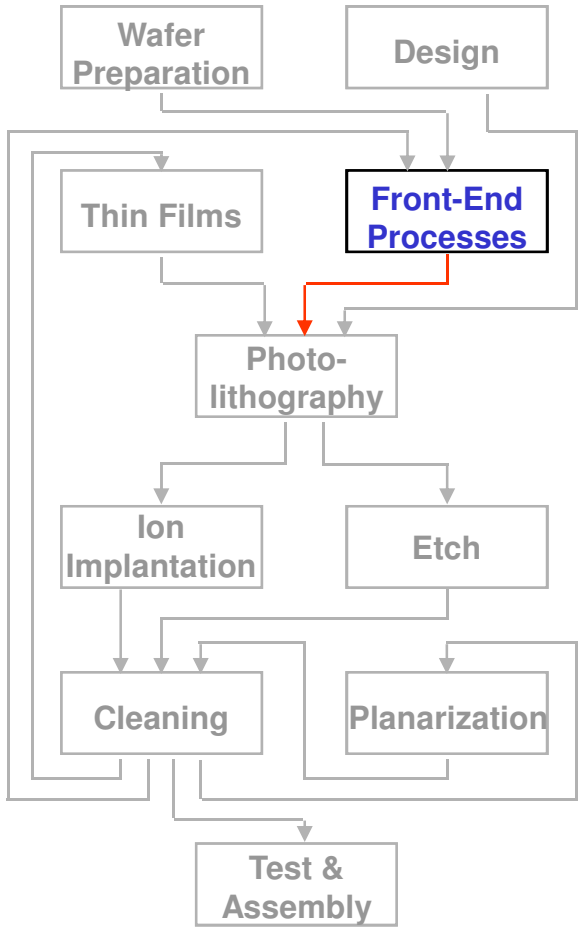
Silicon Sources	Dopants	Etchant
SiH_4	AsH_3	HCl
H_2SiCl_2	B_2H_6	**Carriers**
$HSiCl_3$ *	PH_3	Ar
$SiCl_4$ *		H_2 *
		N_2



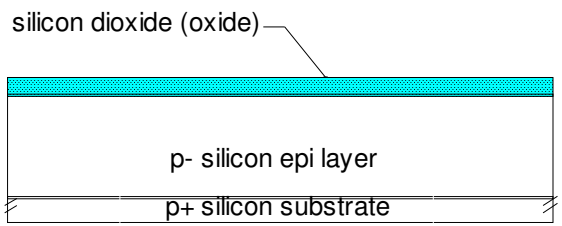
* High proportion of the total product use

Front-End Processes

- Thermal Oxidation
- Silicon Nitride Deposition
  - Low Pressure Chemical Vapor Deposition (LPCVD)
- Polysilicon Deposition
  - Low Pressure Chemical Vapor Deposition (LPCVD)
- Annealing



Front-End Processes



Chemical Reactions

Thermal Oxidation: $Si + O_2 \rightarrow SiO_2$

Nitride Deposition: $3\ SiH_4 + 4\ NH_3 \rightarrow Si_3N_4 + 12\ H_2$

Polysilicon Deposition: $SiH_4 \rightarrow Si + 2\ H_2$

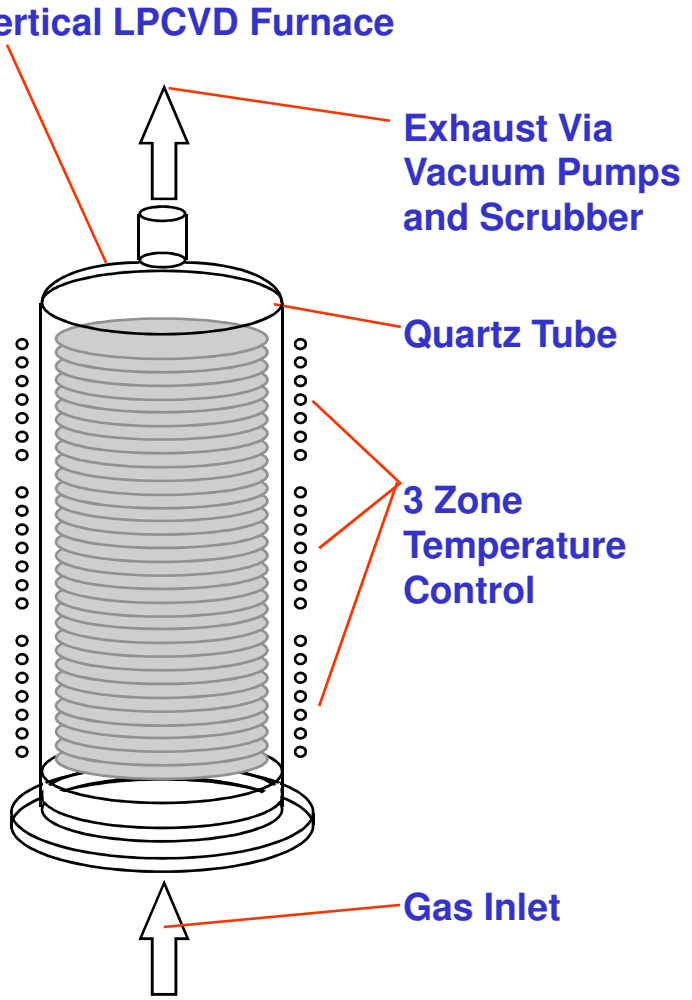
Process Conditions (Silicon Nitride LPCVD)

Flow Rates: 10 - 300 sccm

Temperature: 600 degrees C.

Pressure: 100 mTorr

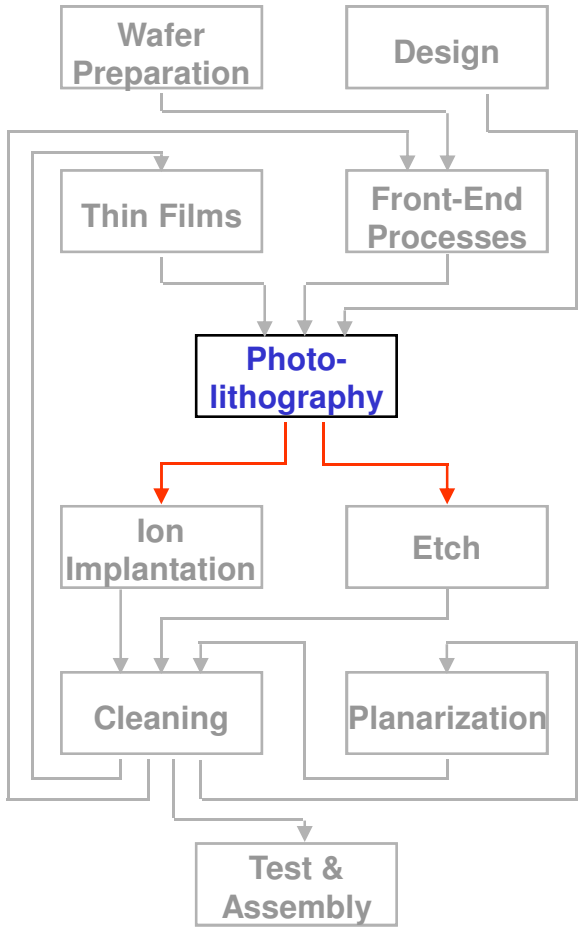
Oxidation	Polysilicon	Nitride	Annealing
Ar	H_2	NH_3 *	Ar
N_2	N_2	H_2SiCl_2 *	He
H_2O	SiH_4 *	N_2	H_2
Cl_2	AsH_3	SiH_4 *	N_2
H_2	B_2H_6	$SiCl_4$	
HCl *	PH_3		
O_2 *			
Dichloroethene *			



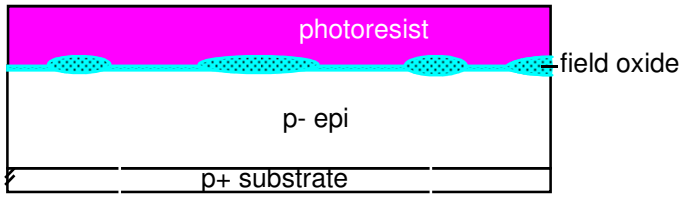
* High proportion of the total product use

Photolithography

- Photoresist Coating Processes
- Exposure Processes



Photoresist Coating Processes



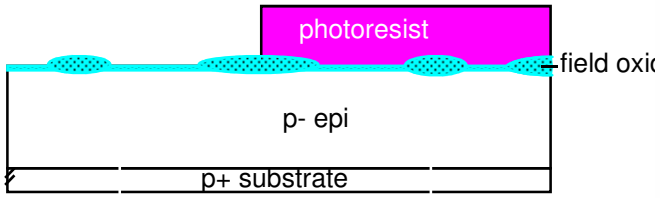
Photoresists
- Negative Photoresist *
- Positive Photoresist *

Other Ancillary Materials (Liquids)
- Edge Bead Removers *
- Anti-Reflective Coatings *
- Adhesion Promoters/Primers (HMDS) *
- Rinsers/Thinners/Corrosion Inhibitors *
- Contrast Enhancement Materials *

Developers
- TMAH *
- Specialty Developers *

Inert Gases
- Ar
- N_2

Exposure Processes

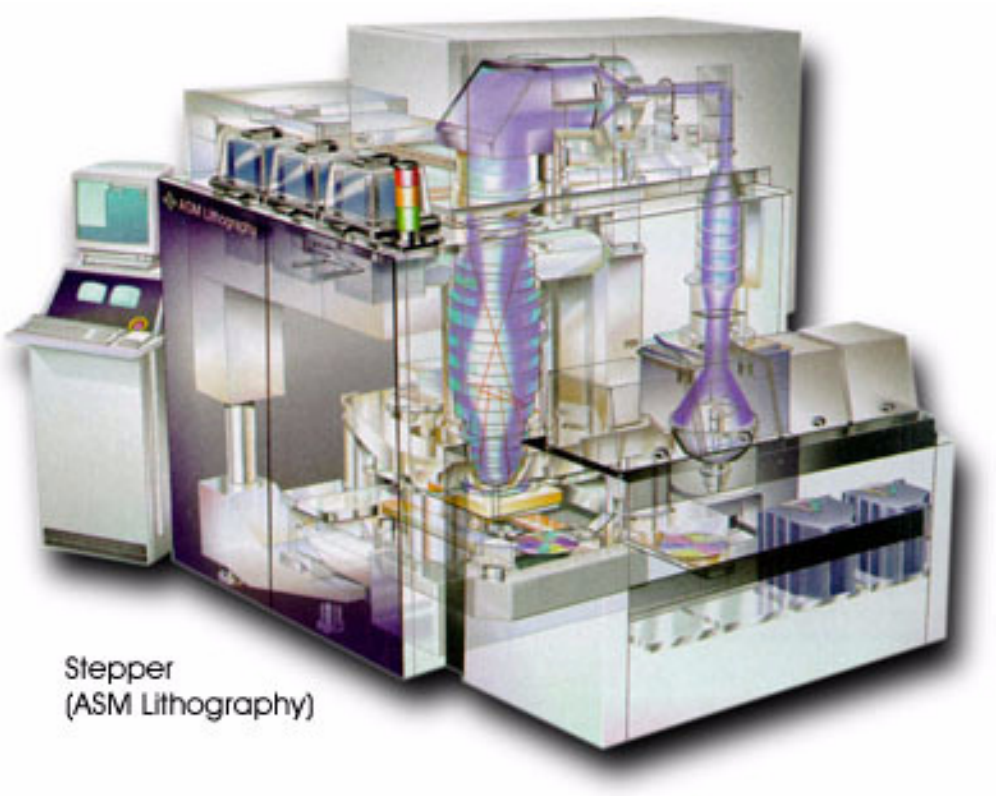


Expose

$Kr + F_2$ (gas) *

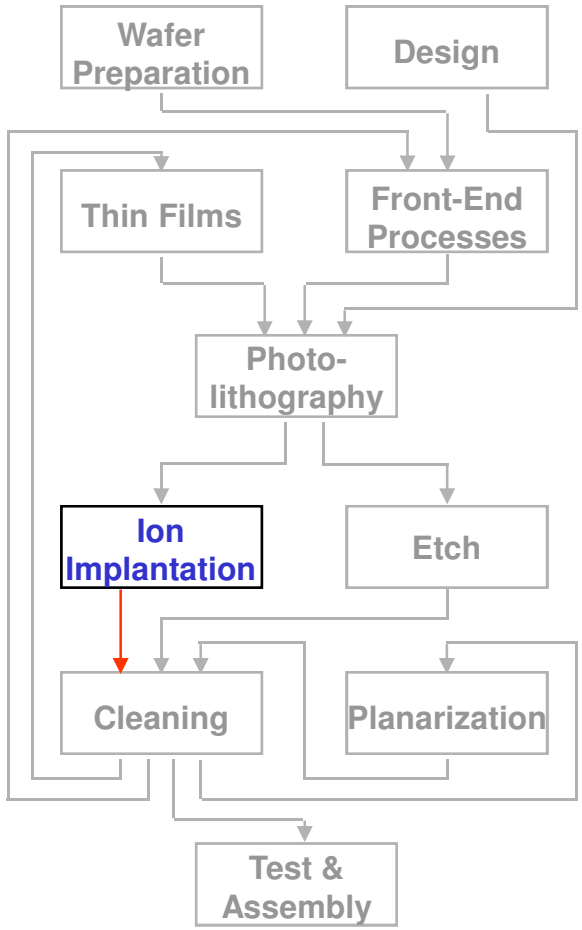
Inert Gases

N_2

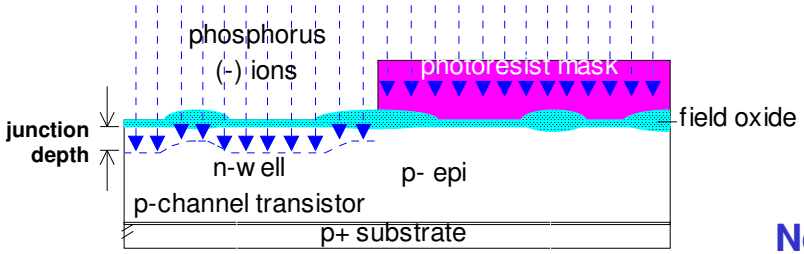


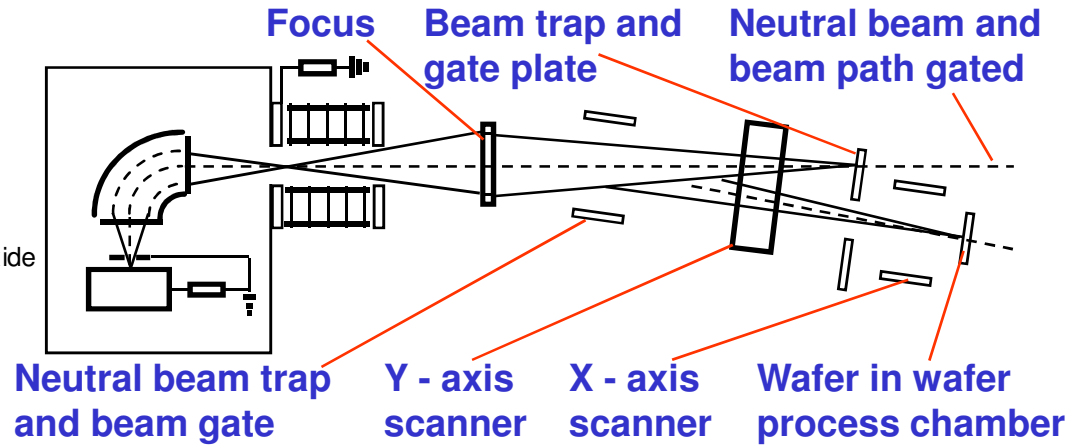
Ion Implantation

- Well Implants
- Channel Implants
- Source/Drain Implants



Ion Implantation





Process Conditions

Flow Rate: 5 sccm

Pressure: 10^{-5} Torr

Accelerating Voltage: 5 to 200 keV

Gases

Ar

AsH_3

$B^{11}F_3$ *

He

N_2

PH_3

SiH_4

SiF_4

GeH_4

Solids

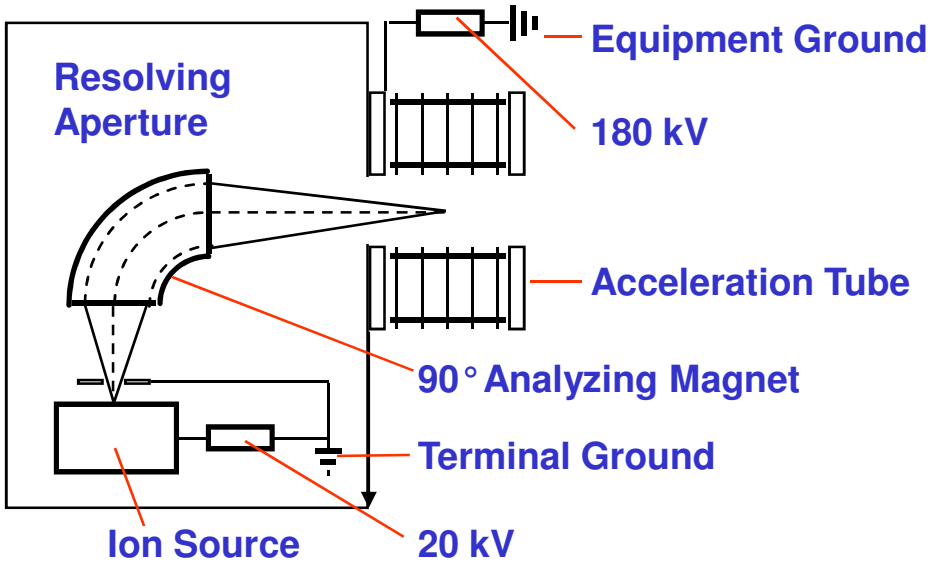
Ga

In

Sb

Liquids

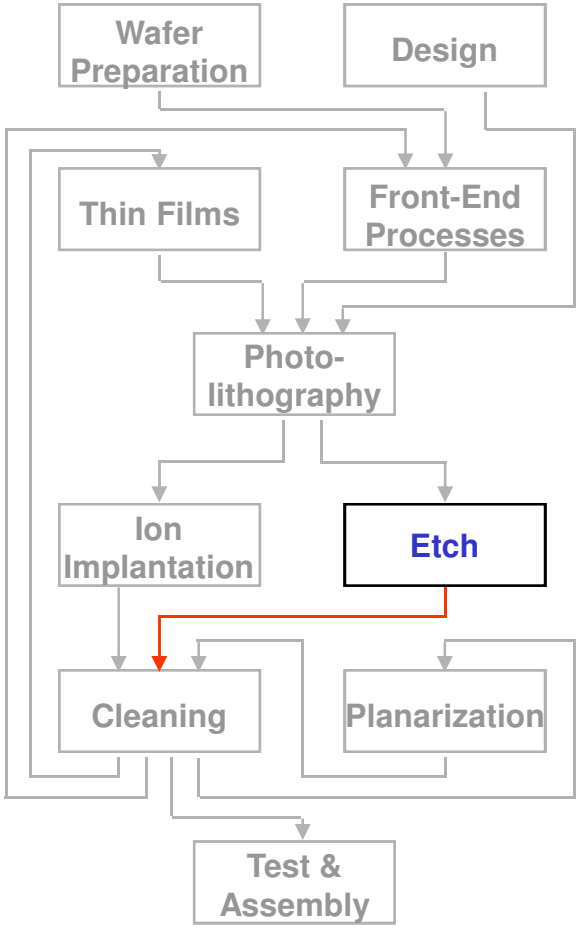
$Al(CH_3)_3$



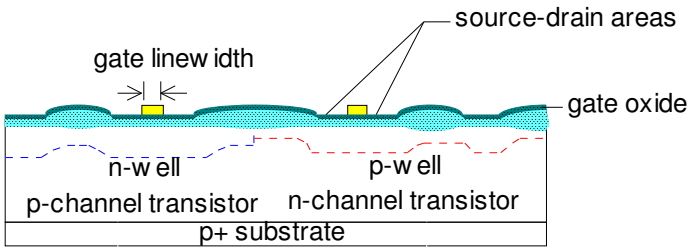
* High proportion of the total product use

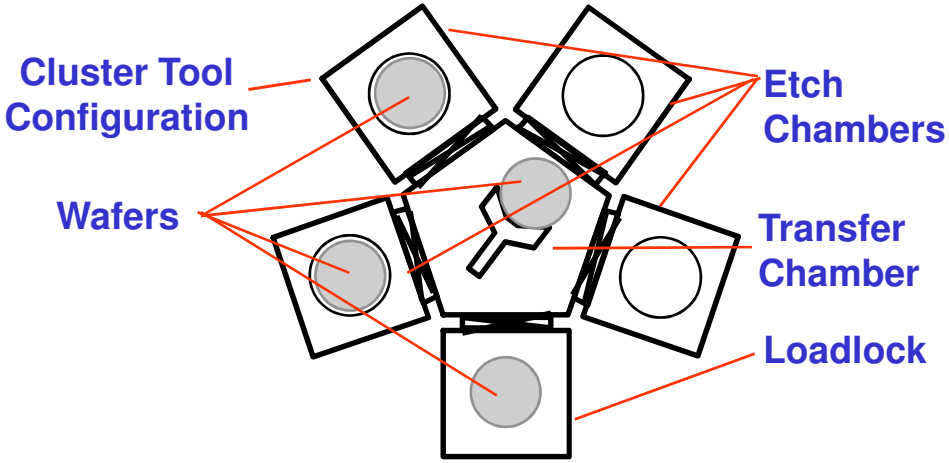
Etch

- Conductor Etch
  - Poly Etch and Silicon Trench Etch
  - Metal Etch
- Dielectric Etch



Conductor Etch





Chemical Reactions

Silicon Etch: $Si + 4\ HBr \rightarrow SiBr_4 + 2\ H_2$

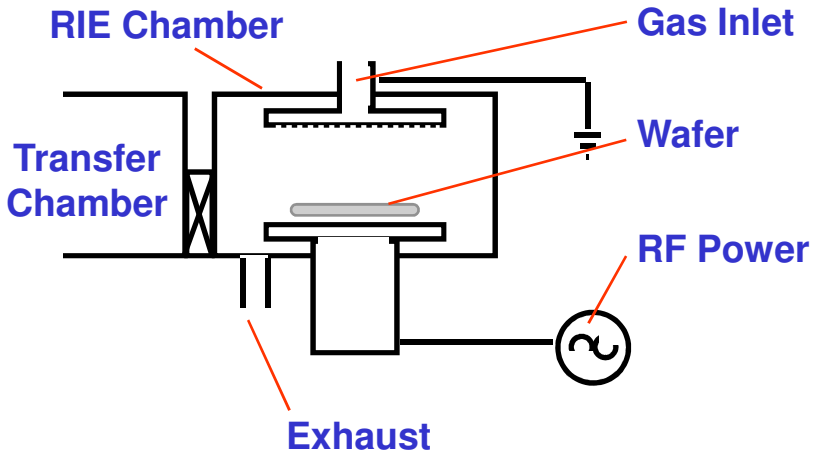
Aluminum Etch: $Al + 2\ Cl_2 \rightarrow AlCl_4$

Process Conditions

Flow Rates: 100 to 300 sccm

Pressure: 10 to 500 mTorr

RF Power: 50 to 100 Watts



Polysilicon Etches

- HBr *
- C_2F_6
- SF_6 *
- NF_3 *
- O_2

Aluminum Etches

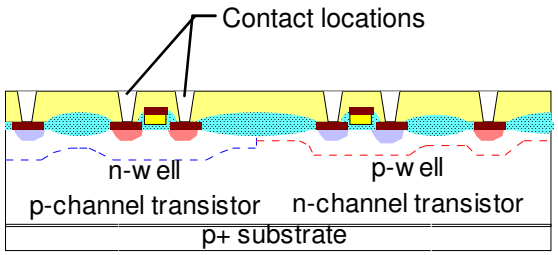
- BCl_3 *
- Cl_2

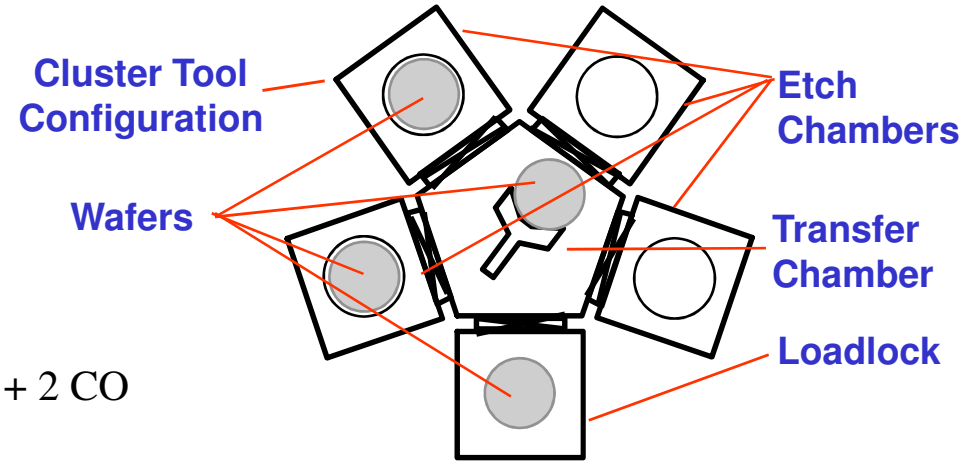
Diluents

- Ar
- He
- N_2

* High proportion of the total product use

Dielectric Etch





Chemical Reactions

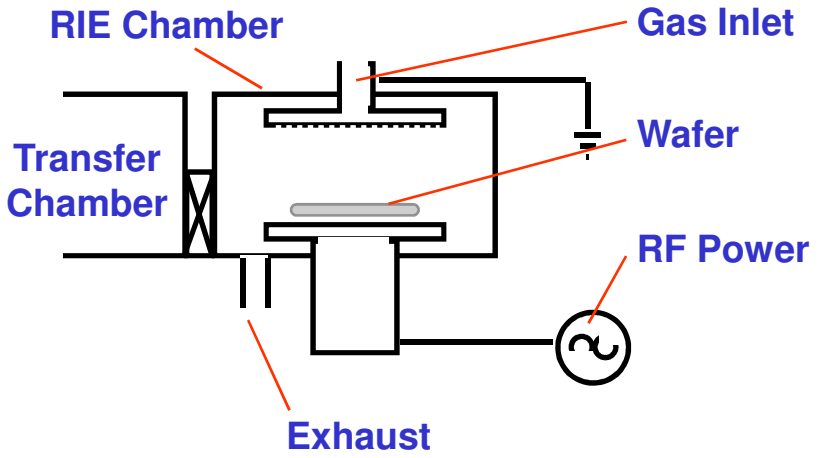
Oxide Etch: $SiO_2 + C_2F_6 \rightarrow SiF_4 + CO_2 + CF_4 + 2\ CO$

Process Conditions

Flow Rates: 10 to 300 sccm

Pressure: 5 to 10 mTorr

RF Power: 100 to 200 Watts



Plasma Dielectric Etches

CHF_3 *
CF_4
C_2F_6
C_3F_8
CO *
CO_2
O_2
SF_6
SiF_4

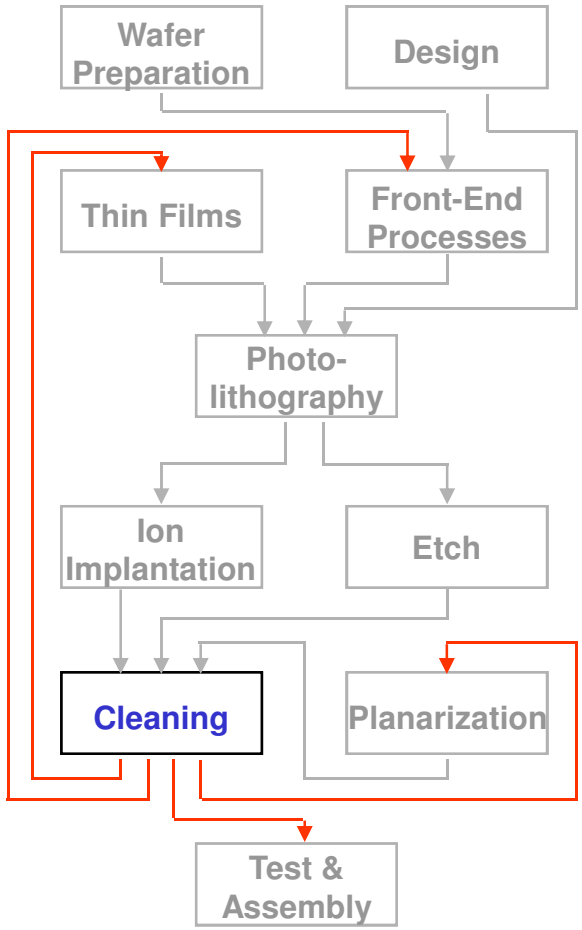
Diluents

Ar
He
N_2

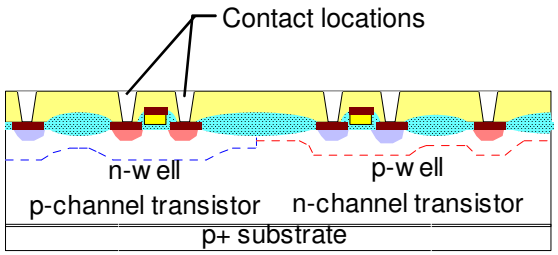
* High proportion of the total product use

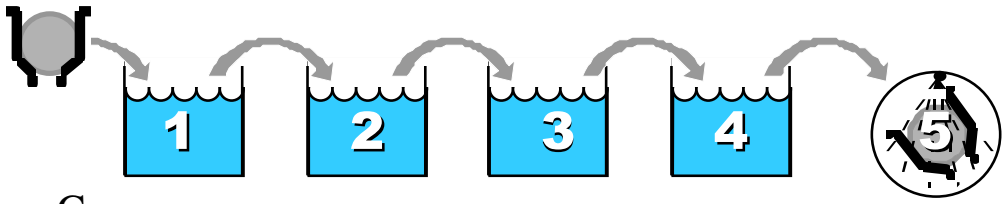
Cleaning

- Critical Cleaning
- Photoresist Strips
- Pre-Deposition Cleans



Critical Cleaning





1 Organics
H_2SO_4 +
H_2O_2
H_2O Rinse

2 Oxides
HF +
H_2O
H_2O Rinse

3 Particles
NH_4OH +
$H_2O_2 + H_2O$
H_2O Rinse

4 Metals
HCl +
$H_2O_2 + H_2O$
H_2O Rinse

5 Dry
H_2O or IPA +
N_2

Process Conditions

Temperature: Piranha Strip is 180 degrees C.

RCA Clean

SC1 Clean ($H_2O + NH_4OH + H_2O_2$) *

* SC2 Clean ($H_2O + HCl + H_2O_2$) *

Piranha Strip

* $H_2SO_4 + H_2O_2$ *

Nitride Strip

H_3PO_4 *

Oxide Strip

HF + H_2O *

Dry Strip

N_2O

O_2

$CF_4 + O_2$

O_3

Solvent Cleans

NMP

Proprietary Amines (liquid)

Dry Cleans

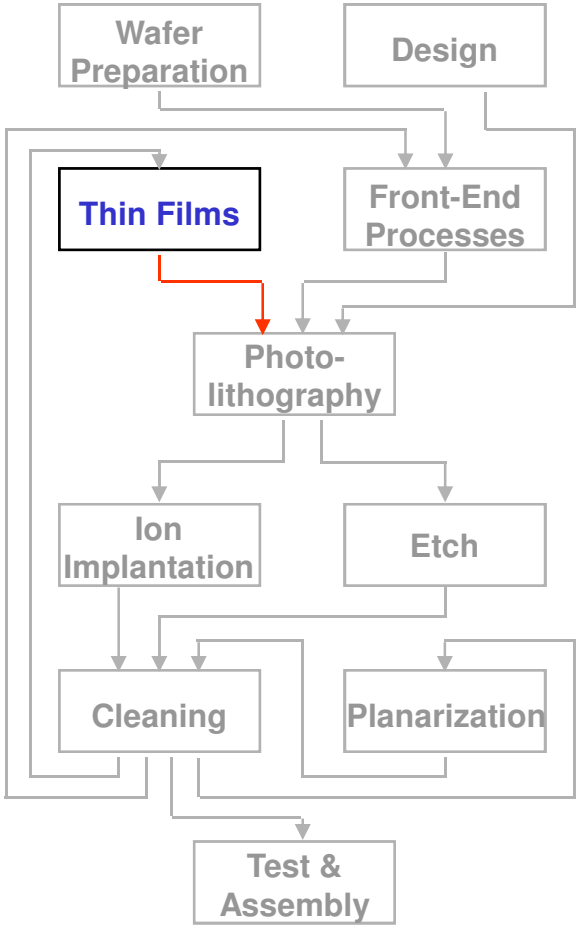
HF

O_2 Plasma

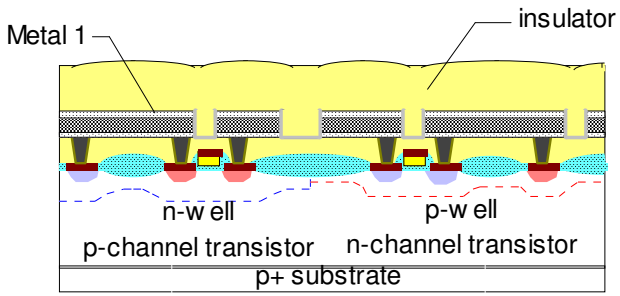
Alcohol + O_3

Thin Films

- Chemical Vapor Deposition (CVD) Dielectric
- CVD Tungsten
- Physical Vapor Deposition (PVD)
- Chamber Cleaning



Chemical Vapor Deposition (CVD) Dielectric



Chemical Reactions

$Si(OC_2H_5)_4 + 9\ O_3 \rightarrow SiO_2 + 5\ CO + 3\ CO_2 + 10\ H_2O$

Process Conditions (ILD)

Flow Rate: 100 to 300 sccm

Pressure: 50 Torr to Atmospheric

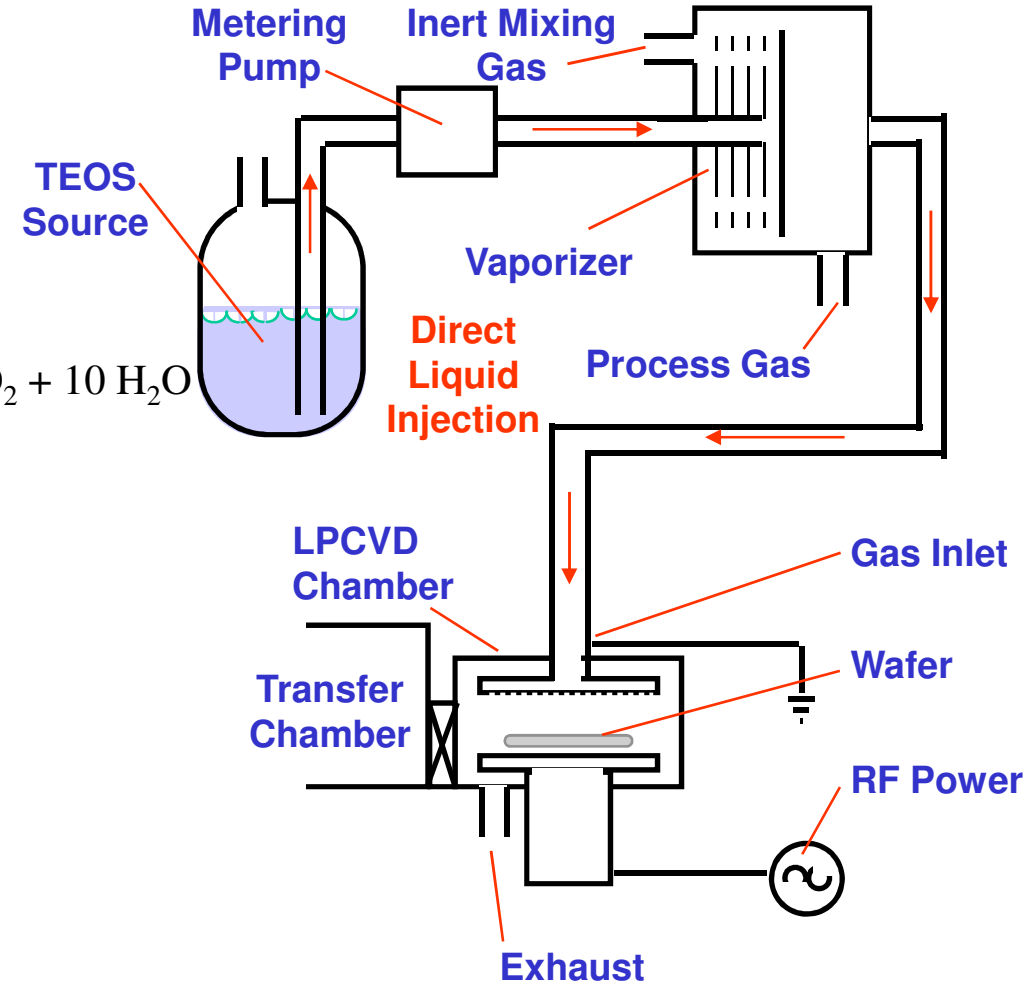
CVD Dielectric

O_2

O_3

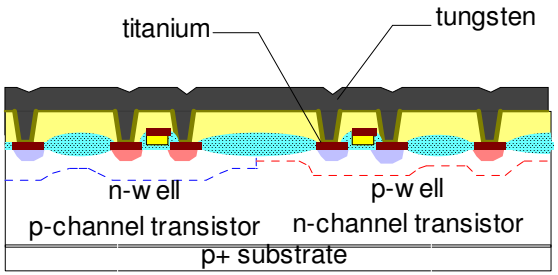
TEOS *

TMP *



* High proportion of the total product use

Chemical Vapor Deposition (CVD) Tungsten



Chemical Reactions

$WF_6 + 3\ H_2 \rightarrow W + 6\ HF$

Process Conditions

Flow Rate: 100 to 300 sccm

Pressure: 100 mTorr

Temperature: 400 degrees C.

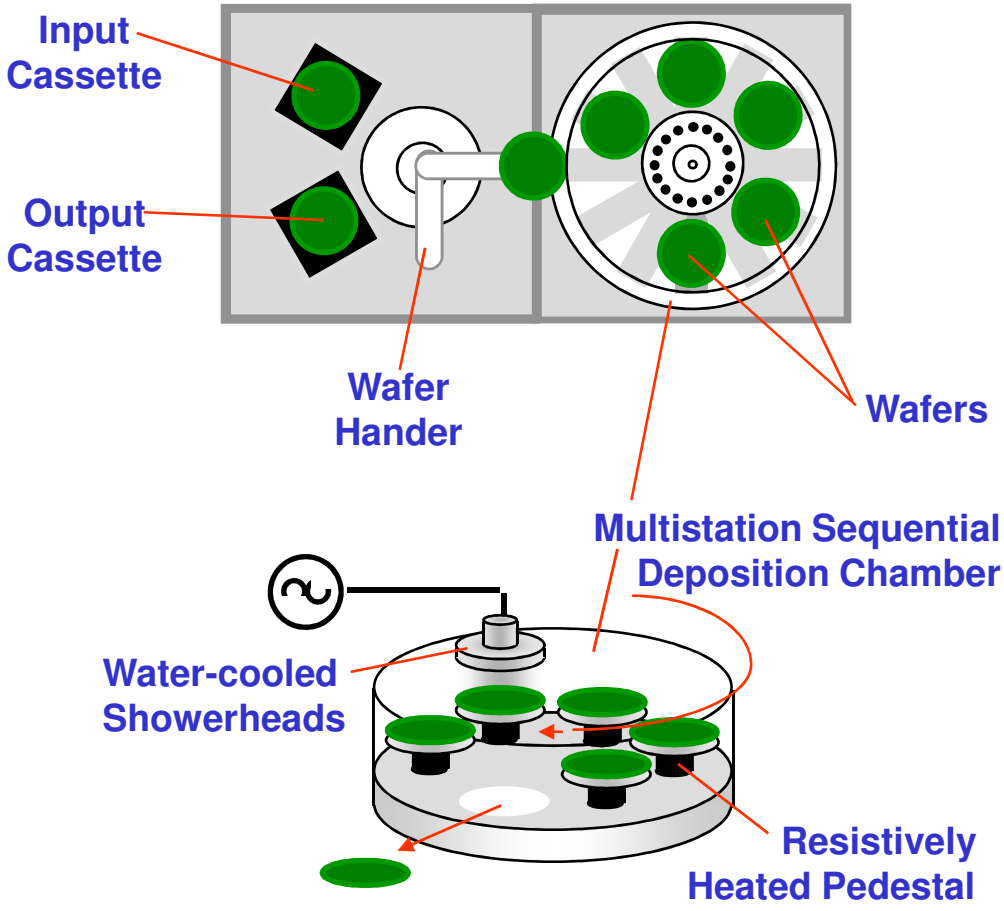
CVD Dielectric

WF_6 *

Ar

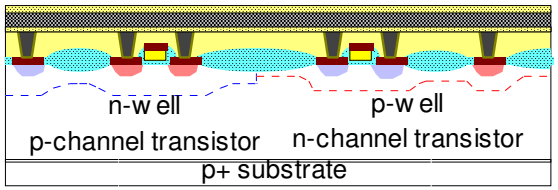
H_2

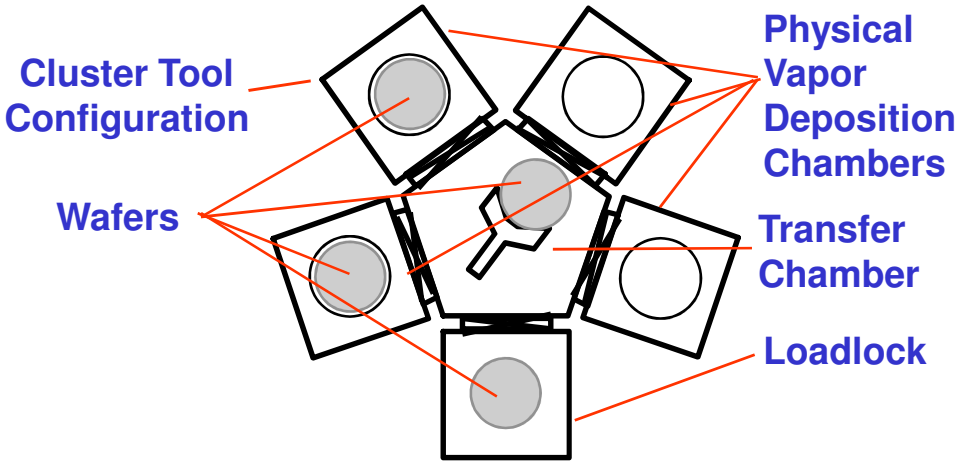
N_2



* High proportion of the total product use

Physical Vapor Deposition (PVD)



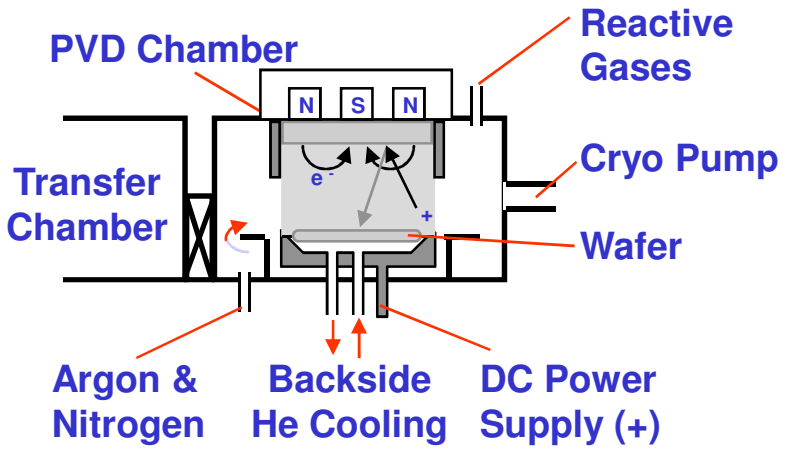


Process Conditions

Pressure: < 5 mTorr
Temperature: 200 degrees C.
RF Power:

Barrier Metals

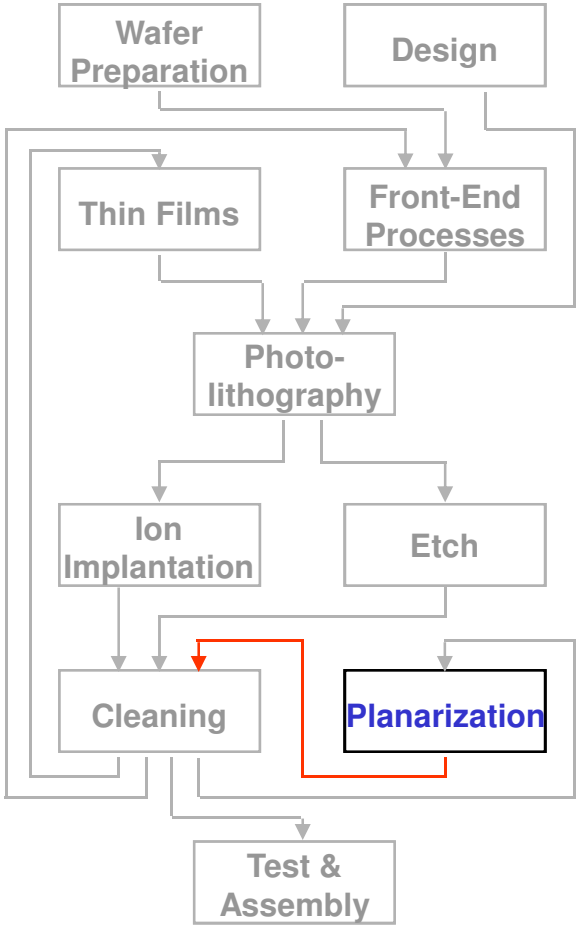
SiH_4
Ar
N_2
N_2
Ti PVD Targets *



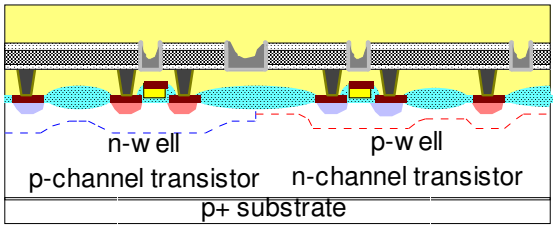
* High proportion of the total product use

Planarization

- Oxide Planarization
- Metal Planarization



Chemical Mechanical Planarization (CMP)



Process Conditions (Oxide)

Flow: 250 to 1000 ml/min
Particle Size: 100 to 250 nm
Concentration: 10 to 15%, 10.5 to 11.3 pH

Process Conditions (Metal)

Flow: 50 to 100 ml/min
Particle Size: 180 to 280 nm
Concentration: 3 to 7%, 4.1 - 4.4 pH

Backing (Carrier) Film

Polyurethane

Pad

Polyurethane

Pad Conditioner

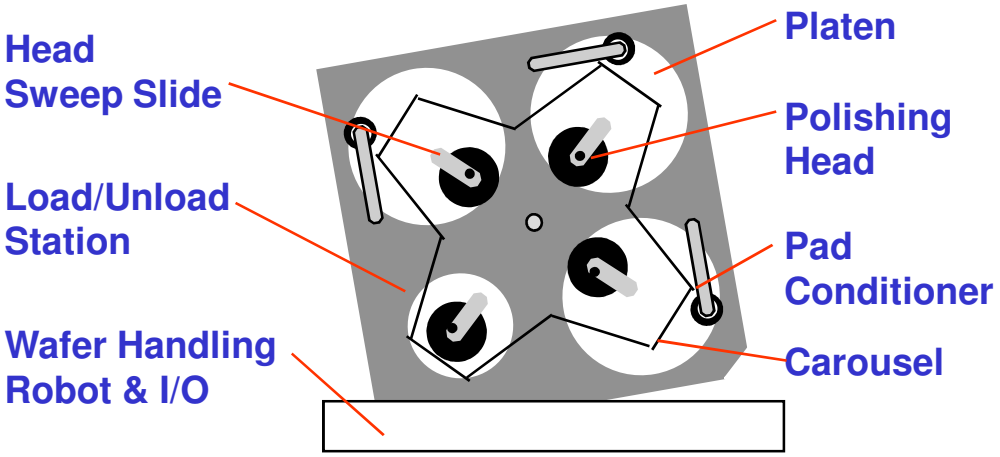
Abrasive

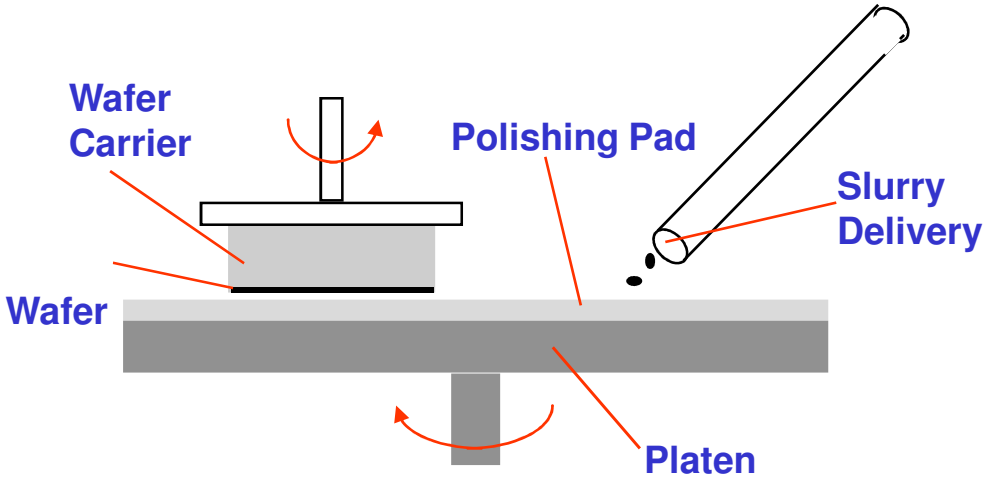
CMP (Oxide)

Silica Slurry *
KOH *
NH_4OH
H_2O

CMP (Metal)

Alumina *
$FeNO_3$

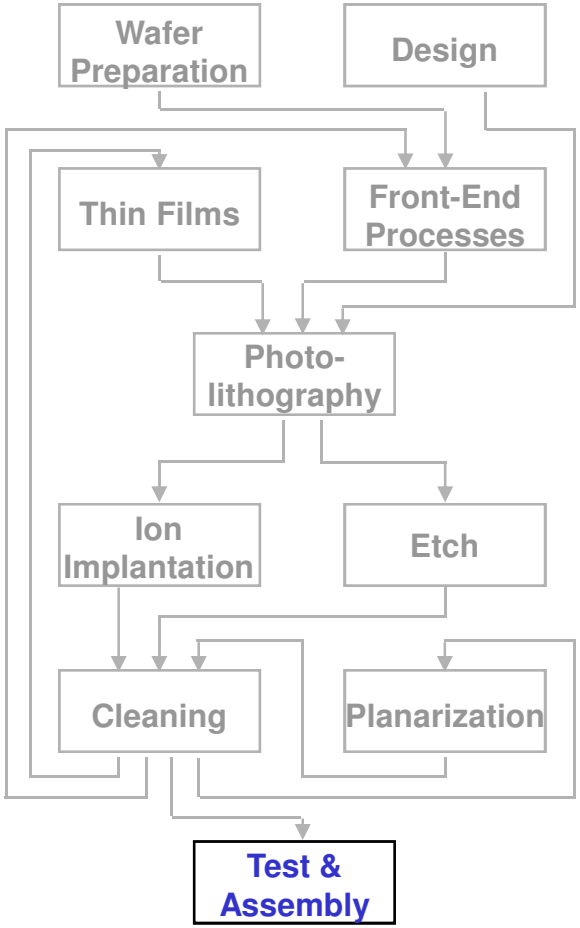




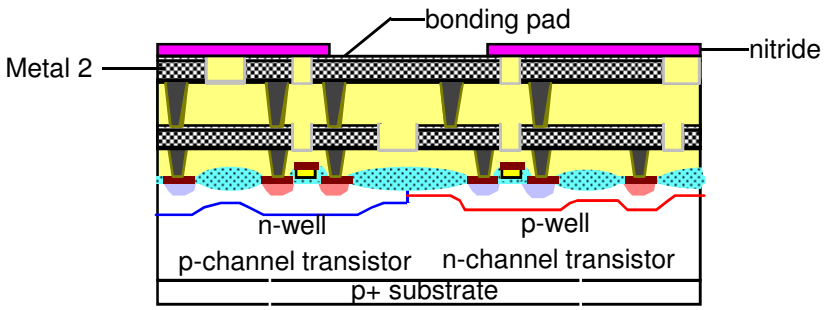
* High proportion of the total product use.

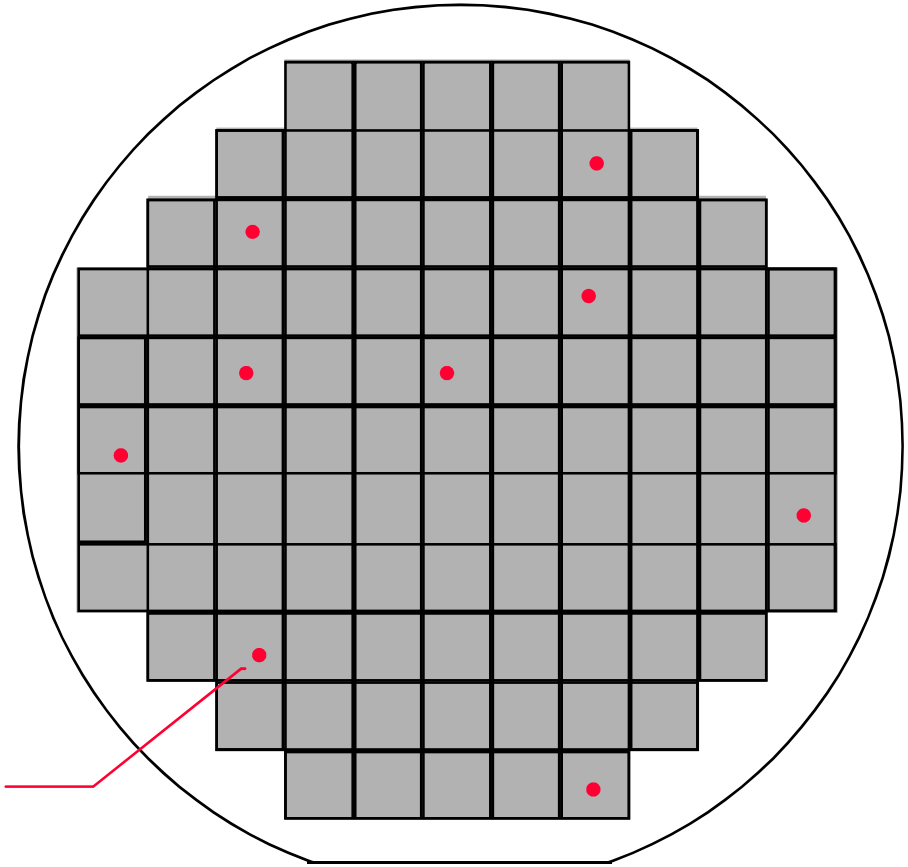
Test and Assembly

- Electrical Test Probe
- Die Cut and Assembly
- Die Attach and Wire Bonding
- Final Test



Electrical Test Probe

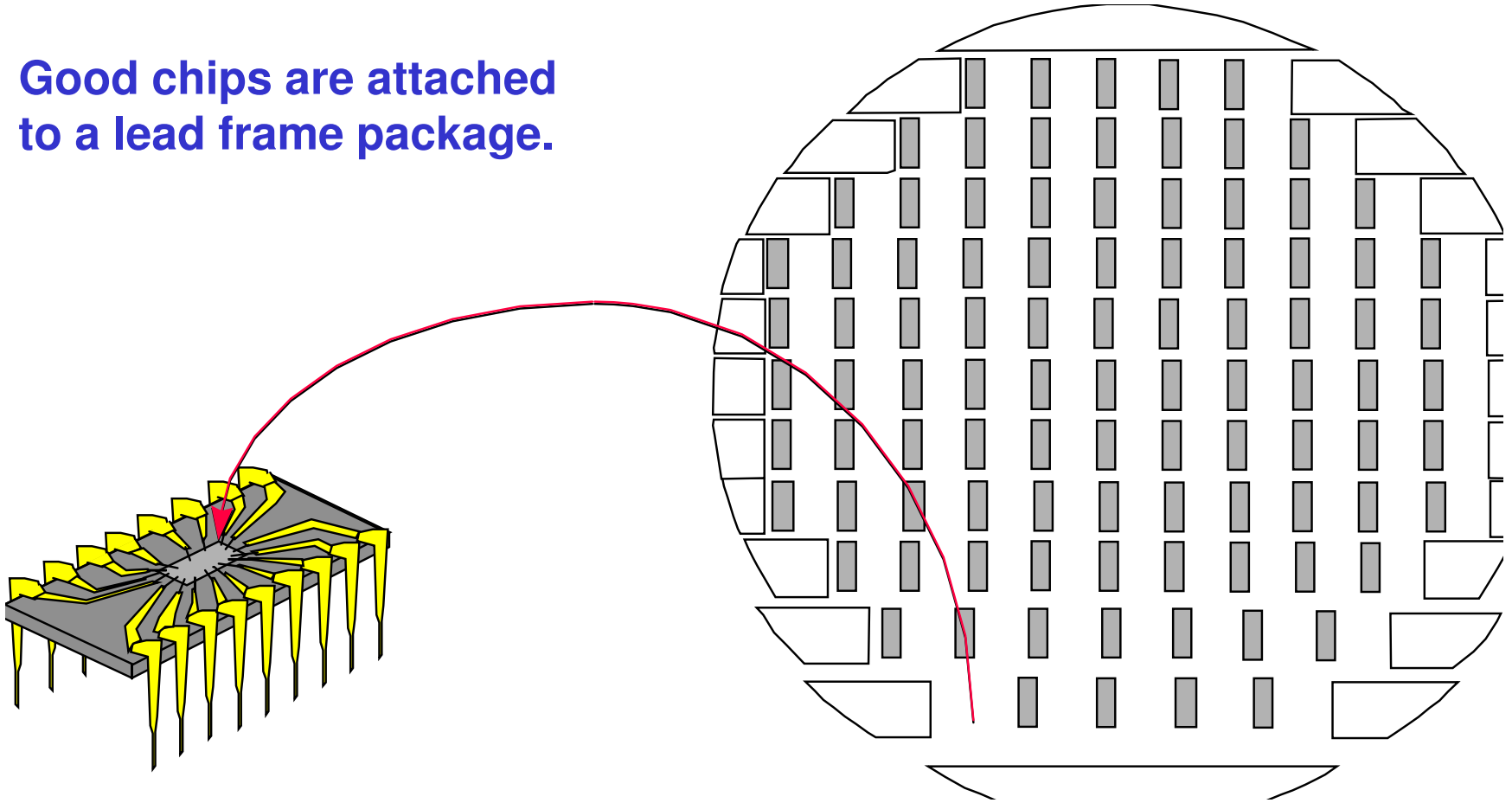




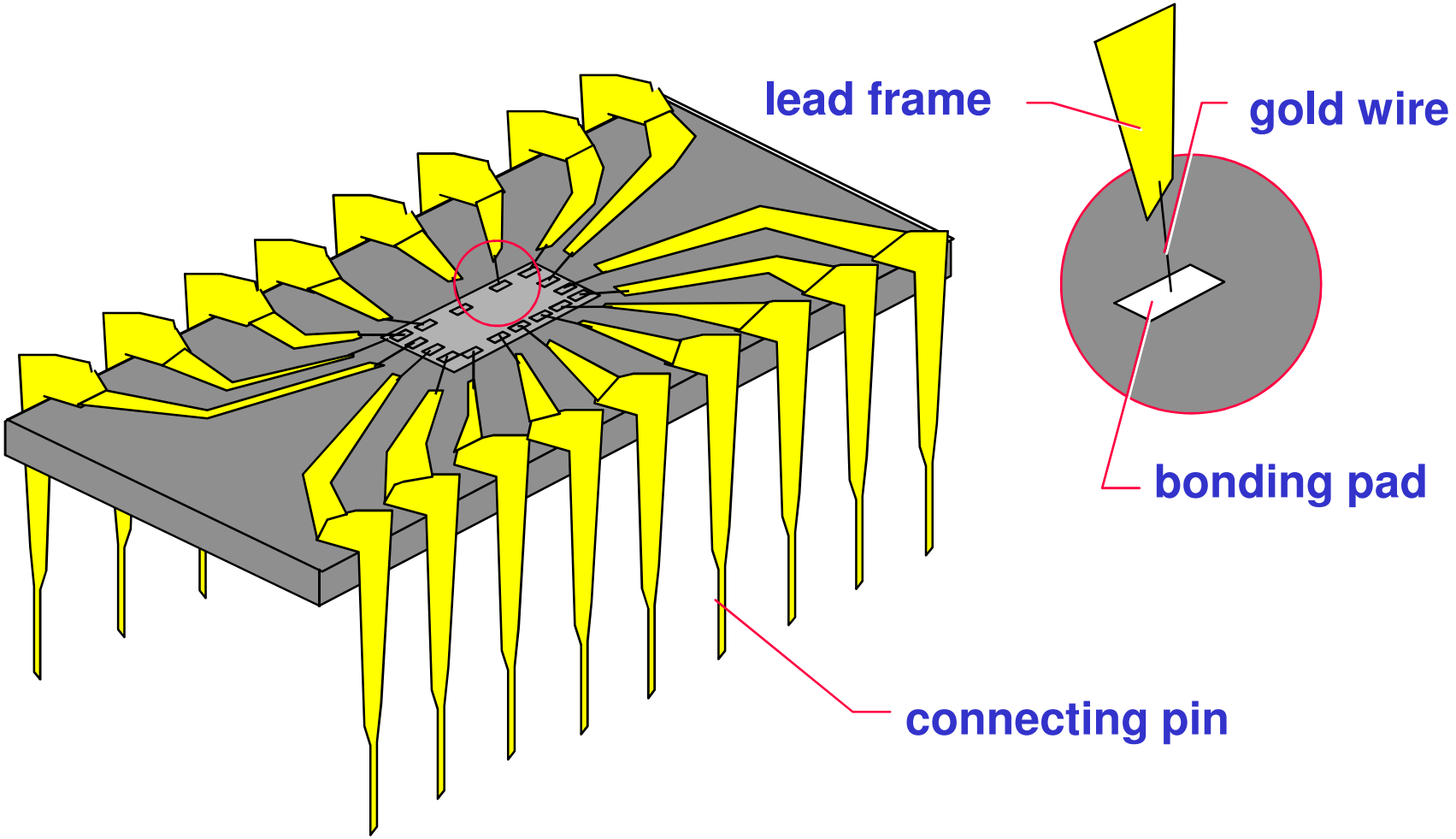
Individual integrated circuits are tested to distinguish good die from bad ones.

Die Cut and Assembly

Good chips are attached to a lead frame package.

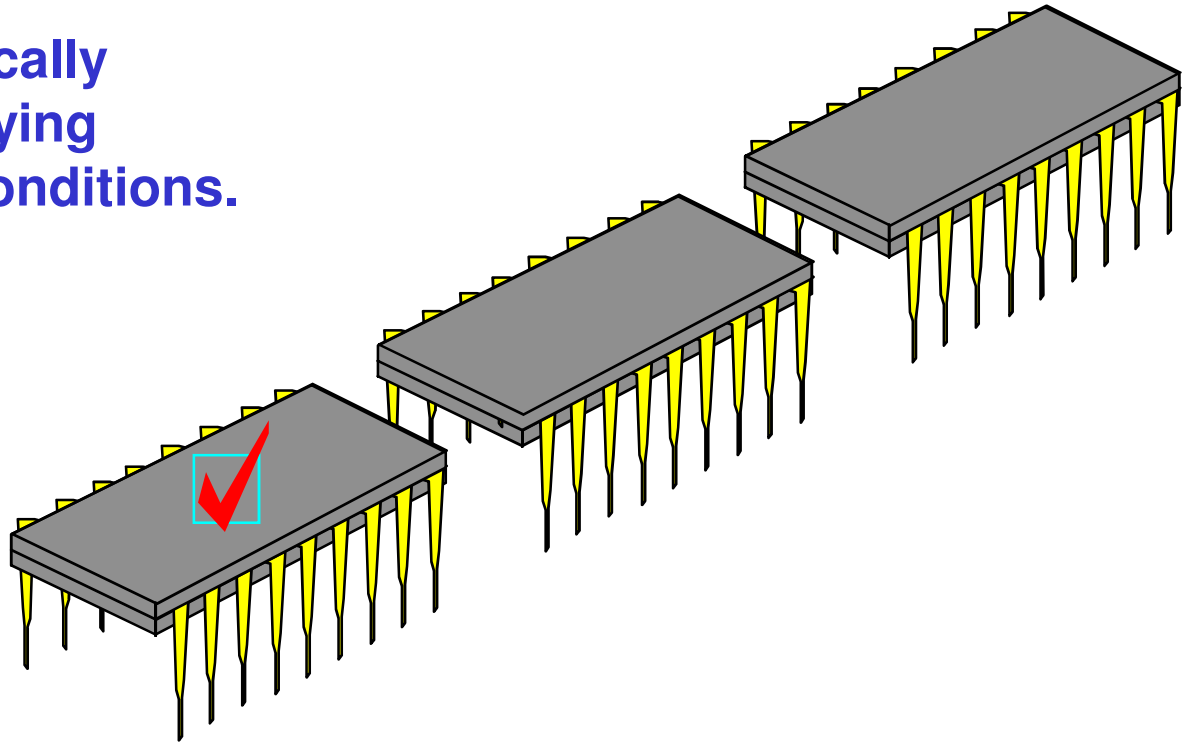


Die Attach and Wire Bonding



Final Test

Chips are electrically tested under varying environmental conditions.



Obrigado