EMICRO/SIM 2013
XV Escola de Microeletrônica da SBC / XXVIII Simpósio Sul de Microeletrônica
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Portas Lógicas CMOS

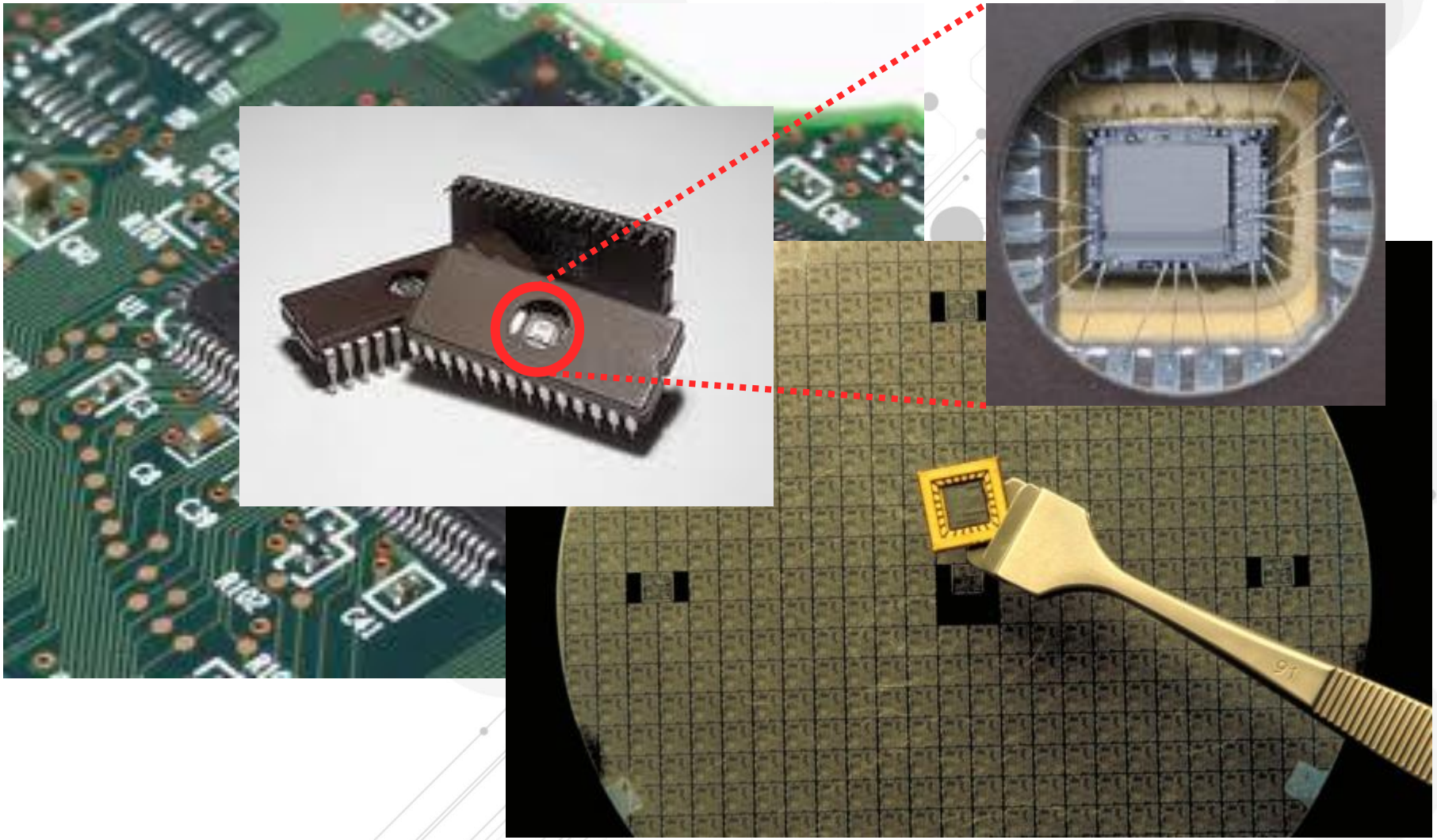
Paulo F. Butzen

Organização
UFRGS

Promoção
SBC CAS SBC IEEE

Apoio
FAPERGS CNPq CAPES CEITEC S.A semiconductors

Curso de Projeto de Circuitos Integrados



Definição da Arquitetura

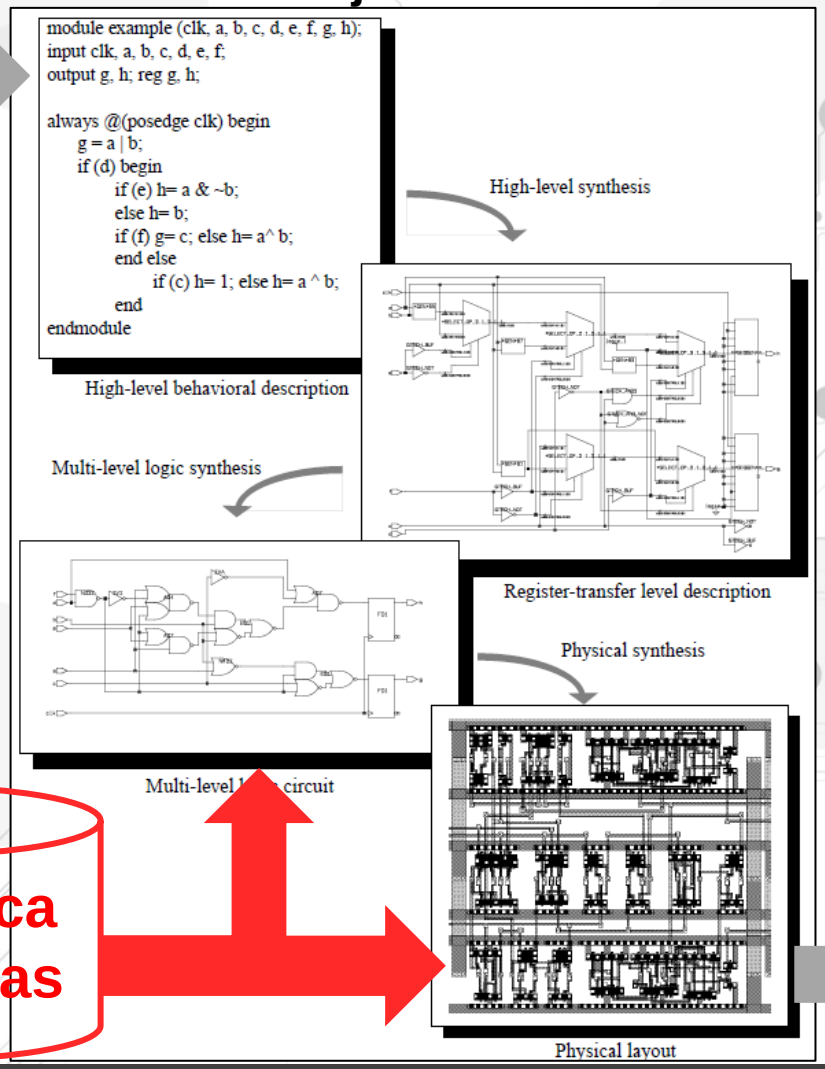
Problema / Necessidade:

- **Rastreamento bovino**
- **TV Digital**
- **Monitoramento de Processos**
- **...**

Conjunto pré-definido, projetado e caracterizado de portas lógicas

Biblioteca de Células

Fluxo de Projeto Automatizado



Envio para Fabricação

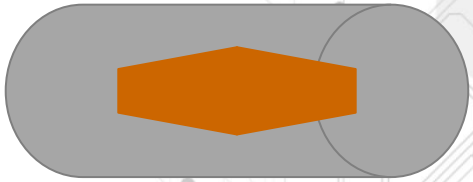
Outline

Apresentação dos projetos lógico, elétrico e físico de portas lógicas CMOS combinacionais e sequenciais, bem como das suas características elétricas e análise de desempenho

- Lógica de com chaves
- Transistor MOS como chave
- Lógica Combinacional CMOS
  - Projeto Lógico
  - Projeto Físico
  - Características Temporais e de Potência
  - Projeto Elétrico
- Lógica Sequencial
  - Latches
  - Flip-Flops

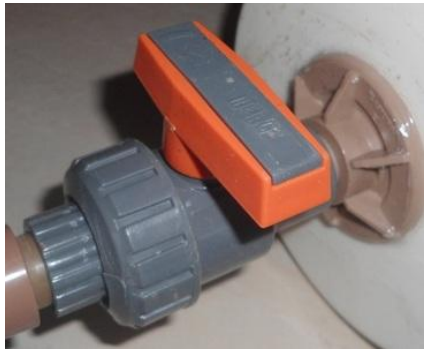
Lógica com Chaves

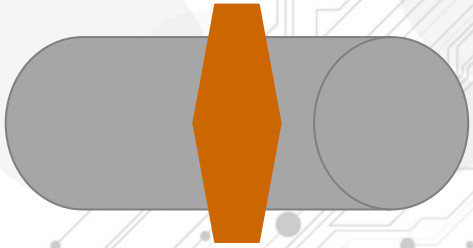
- Associação com Registro Hidráulico



<u>Permite</u> o fluxo de água

Chaves

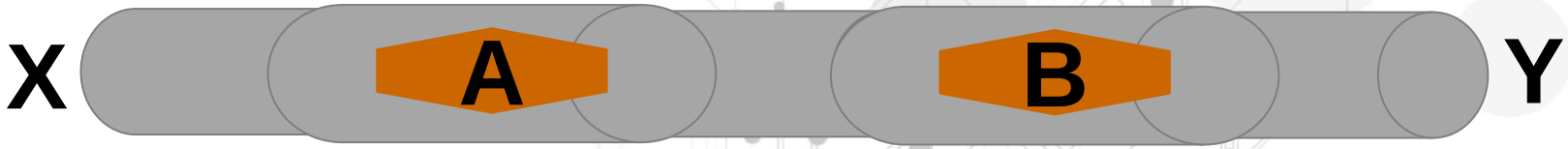




<u>Tranca</u> o fluxo de água

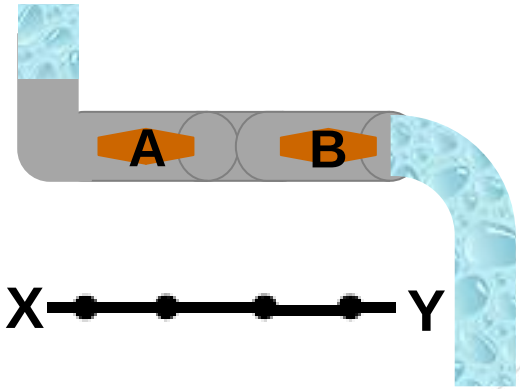
Lógica com Chaves

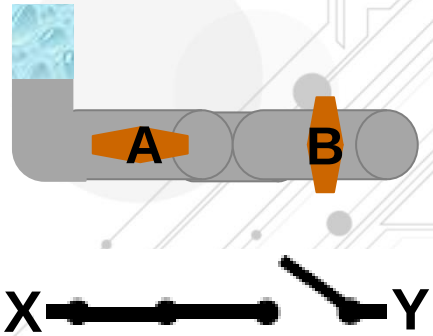
- Associação com Registro Hidráulico

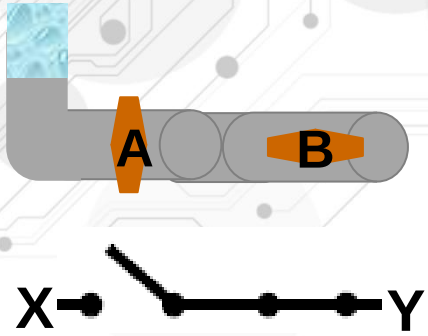


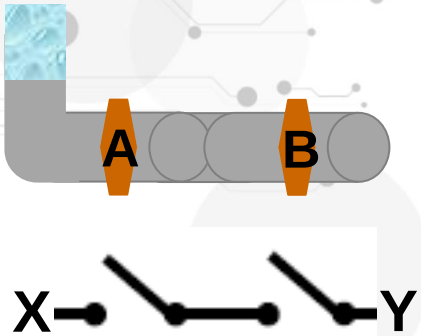
Existirá fluxo de água entre os pontos X e Y

se o "registro A" *E* se o "registro B" permitirem



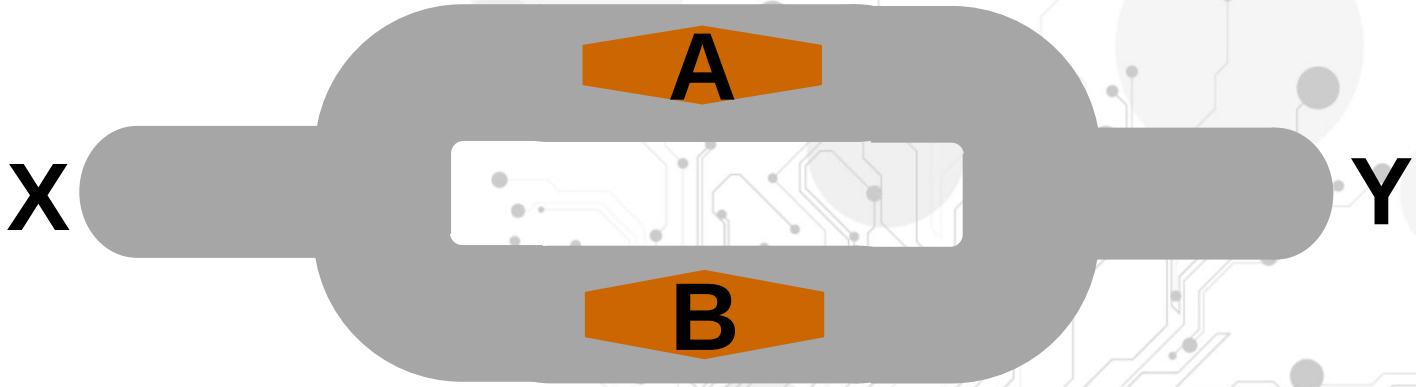






Lógica com Chaves

- Associação com Registro Hidráulico



Existirá fluxo de água entre os pontos X e Y
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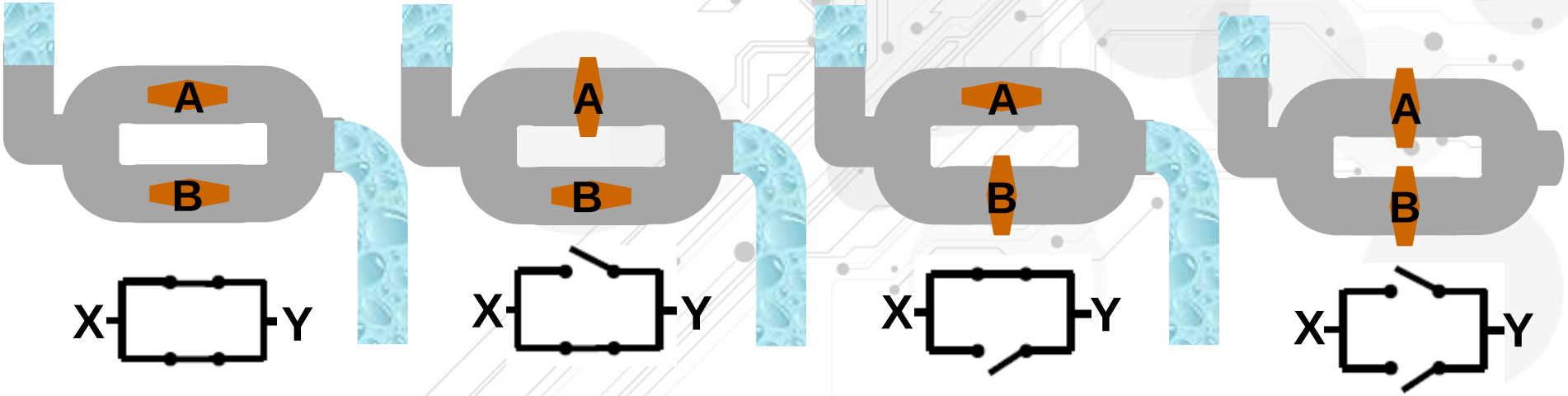
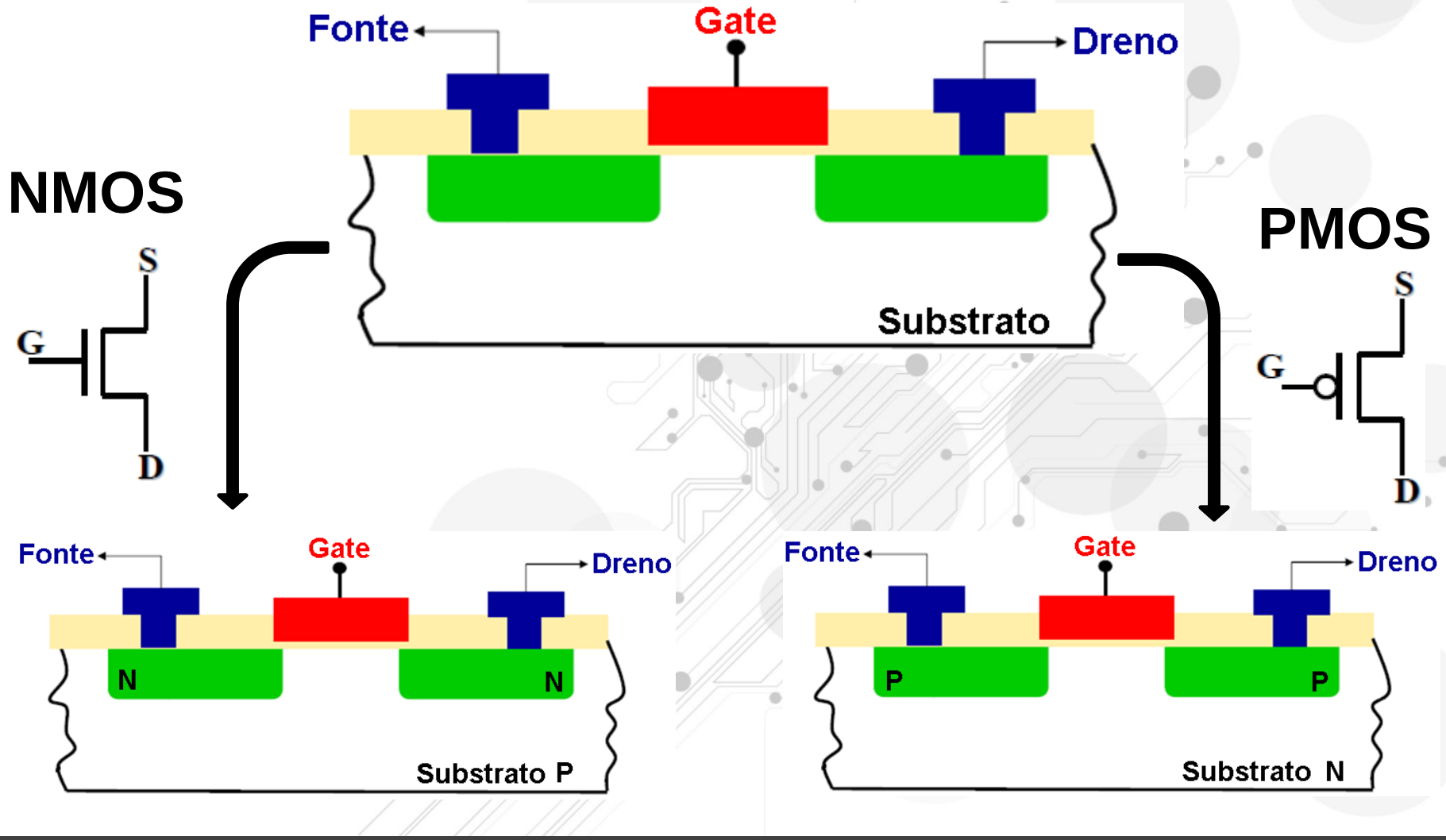
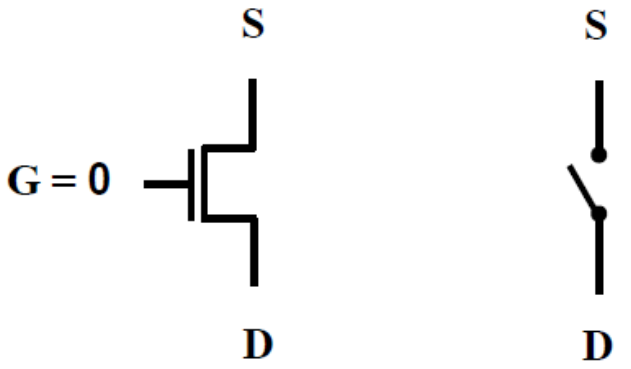


Transistor MOS



O Transistor NMOS

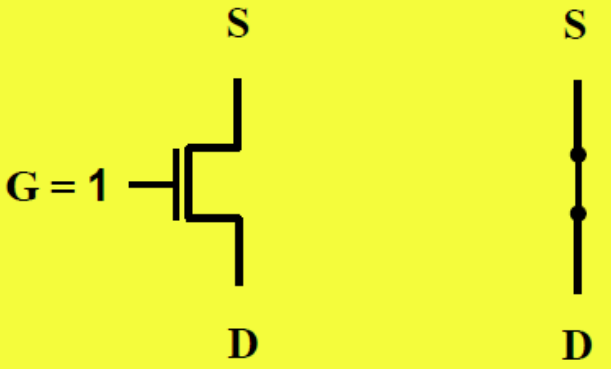
Funcionamento Simplificado: "uma chave eletrônica ideal"



chave aberta

(sem corrente elétrica)

D≠S



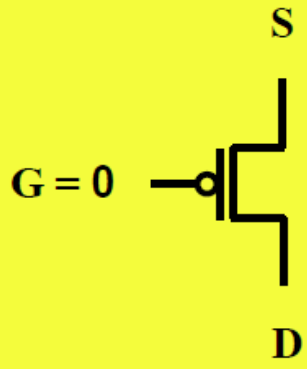
chave fechada

com corrente elétrica até que

D=S

O Transistor PMOS

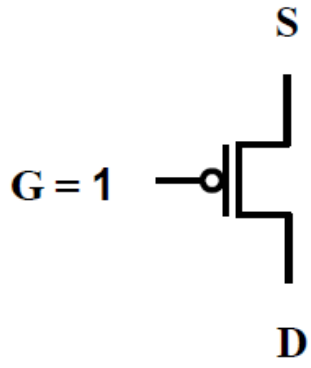
Funcionamento Simplificado: "uma chave eletrônica ideal"



chave fechada

com corrente elétrica até que

D=S



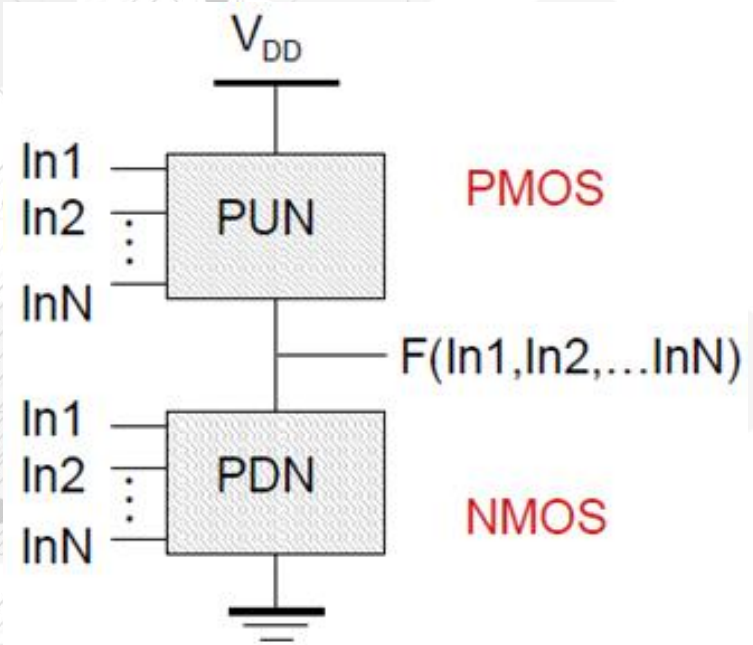
chave aberta

(sem corrente elétrica)

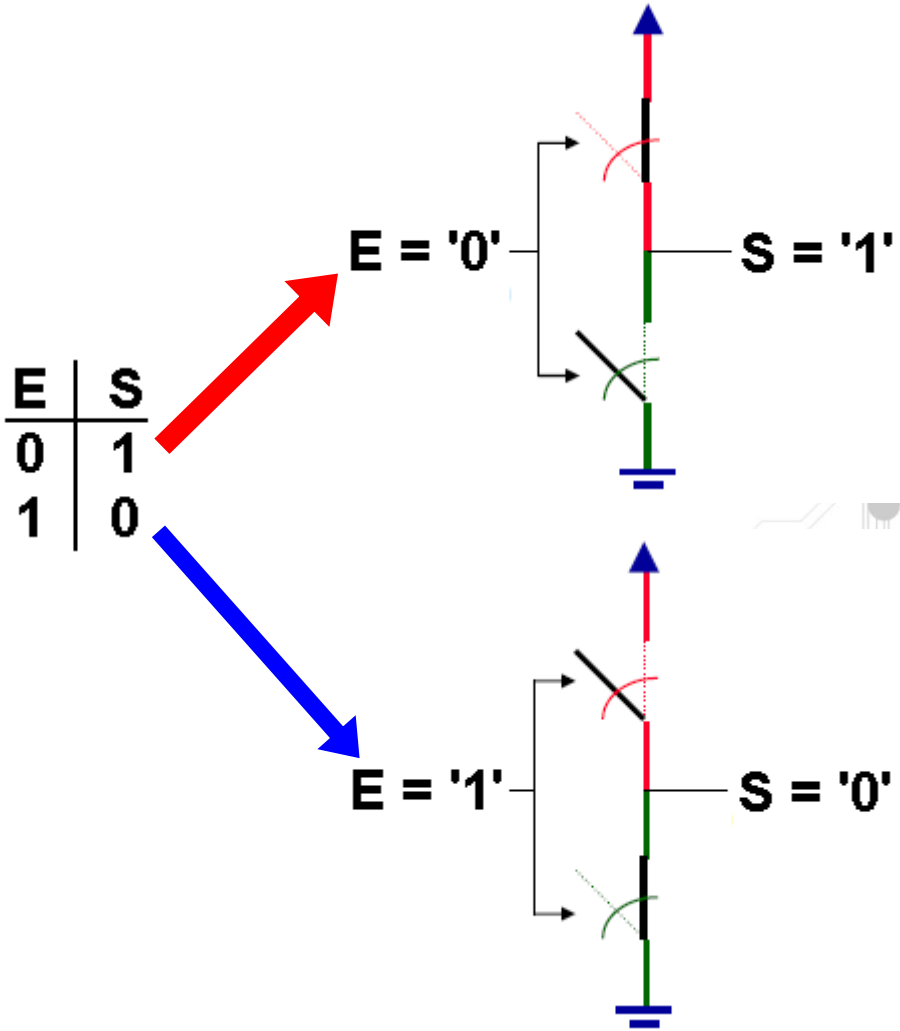
D≠S

Portas Lógicas CMOS

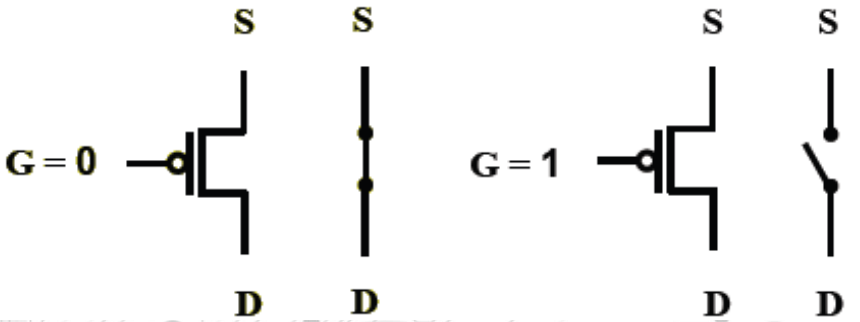
- Família Lógica CMOS
  - Plano Pull-up (PUP) é composto por transistores PMOS
    - NMOS não conduz bem o '1' lógico
  - Plano Pull-down (PDN) é composto por transistores NMOS
    - PMOS não conduz bem o '0' lógico
  - Somente funções negativas são projetadas
    - INV, NAND, NOR, ...
  - As redes de transistores PUP e PDN são complementares

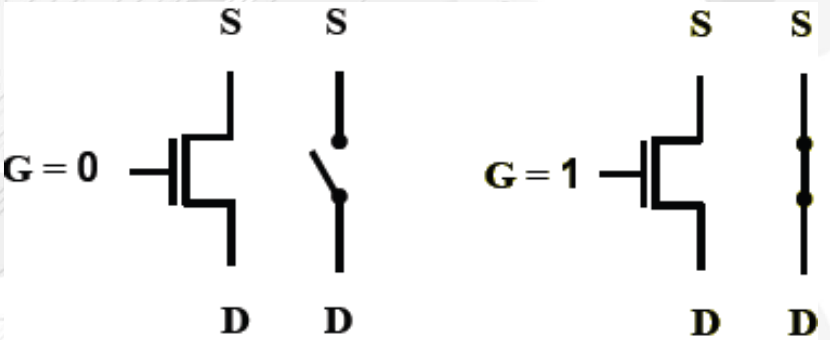


Inversor CMOS



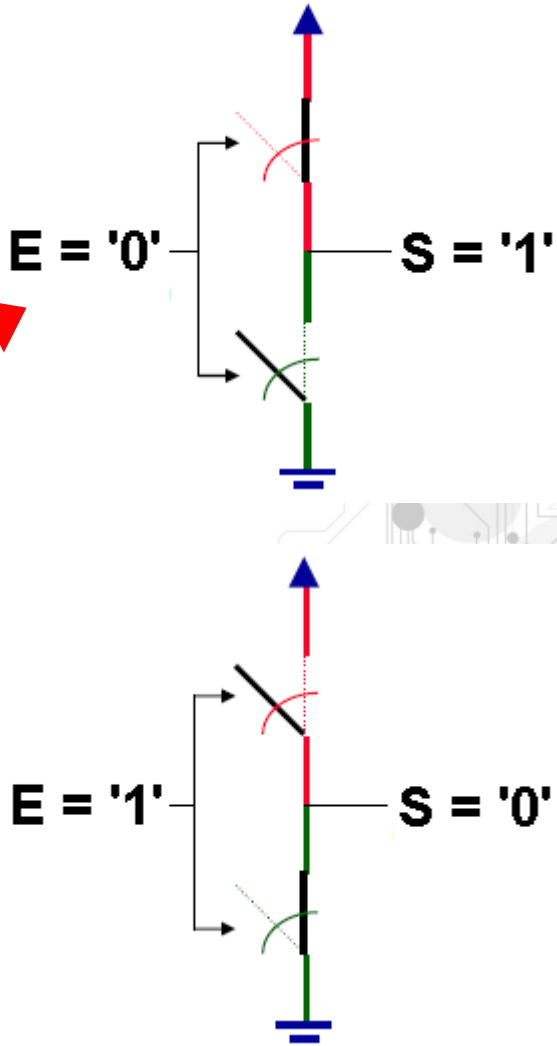
E	S
0	1
1	0

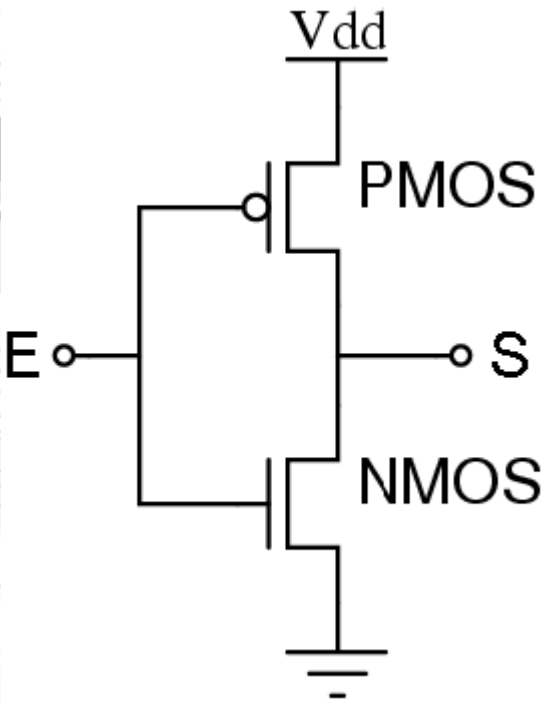




Inversor CMOS

E	S
0	1
1	0

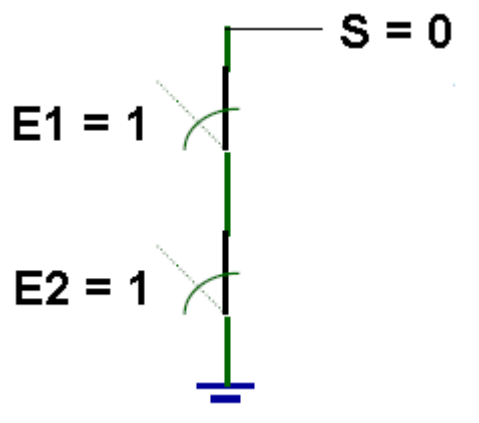


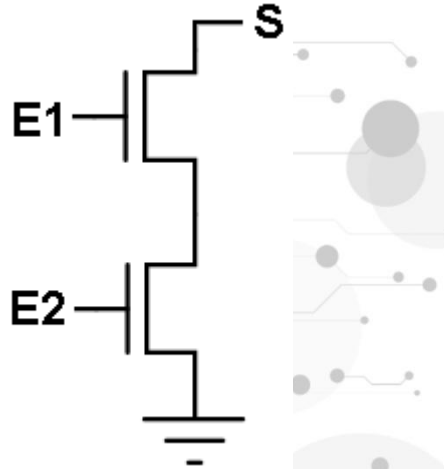


Rede de Transistores

- Transistores NMOS em série
  - Existirá um caminho condutivo SOMENTE se E1 = 1 **'E'** E2 = 1
  - Lógica NAND → S = !(E1*E2)

E1	E2	S
0	0	1
0	1	1
1	0	1
1	1	0

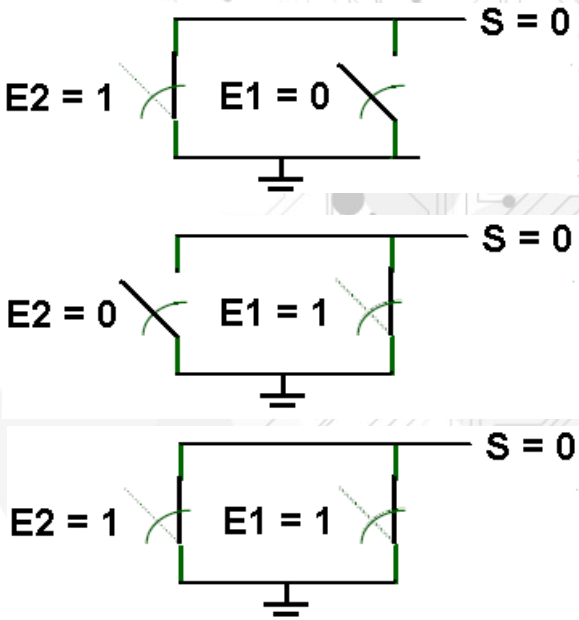


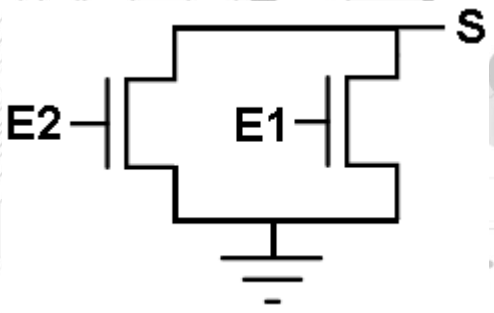


Rede de Transistores

- Transistores NMOS em Paralelo
  - Existirá caminho se E1 = 1 **'OU'** E2 = 1
  - Lógica NOR → S = !(E1 + E2)

E1	E2	S
0	0	1
0	1	0
1	0	0
1	1	0

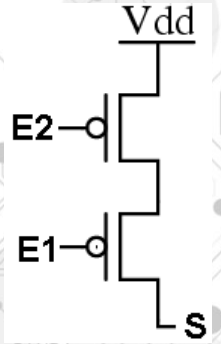




Rede de Transistores

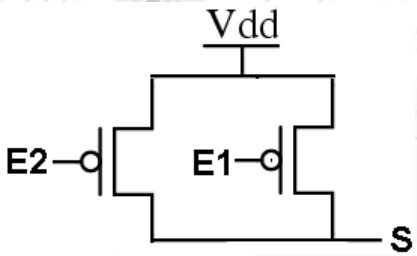
- Transistores PMOS em série
  - Existirá um caminho condutivo SOMENTE se E1 = 0 **'E'** E2 = 0
  - Porta lógica NOR

E1	E2	S
0	0	1
0	1	0
1	0	0
1	1	0



- Transistores PMOS em paralelo
  - Existirá caminho se E1 = 0 **'OU'** E2 = 0
  - Porta lógica NAND

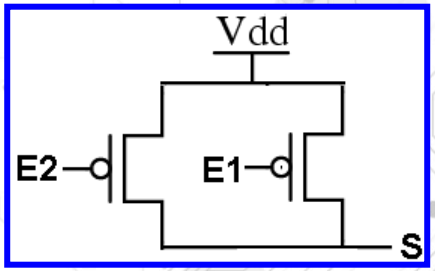
E1	E2	S
0	0	1
0	1	1
1	0	1
1	1	0

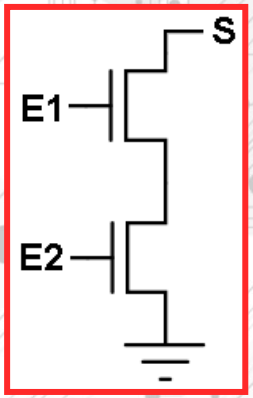


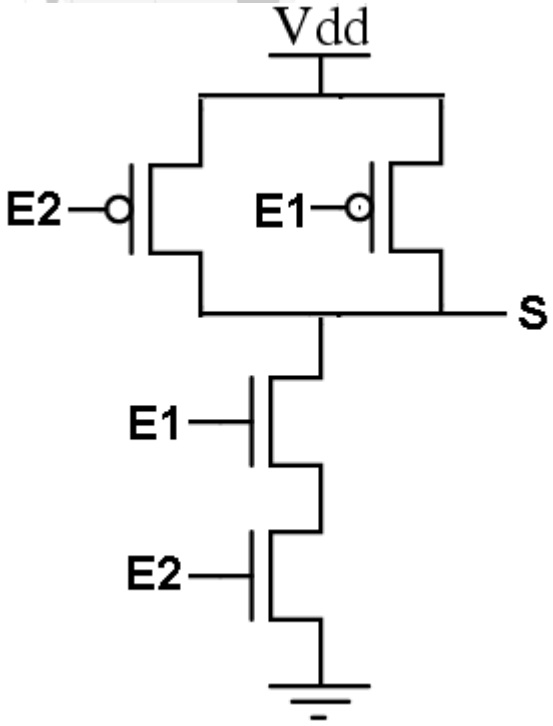
Porta Lógica NAND

- **S = !(E1 * E2)**

E1	E2	S
0	0	1
0	1	1
1	0	1
1	1	0



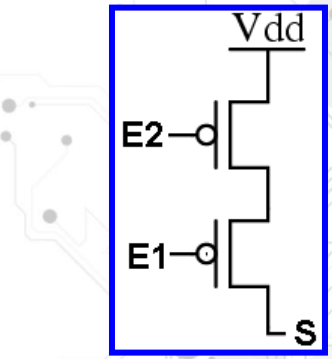


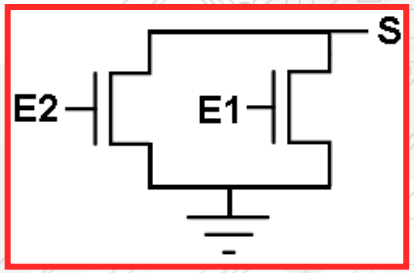


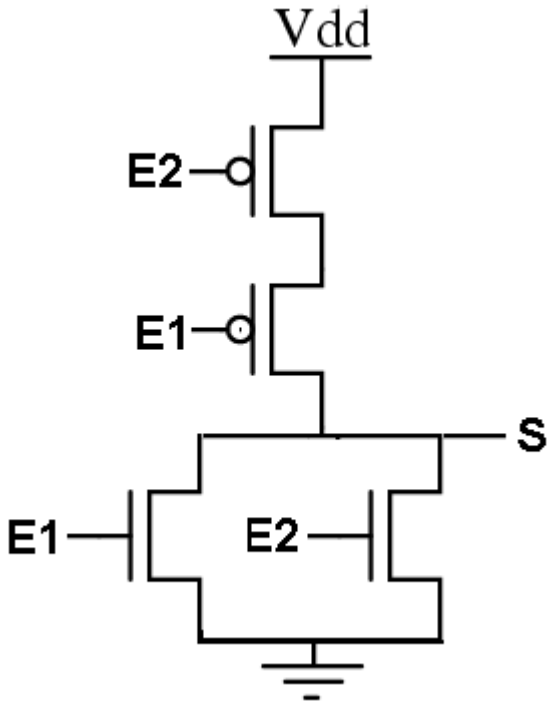
Porta Lógica NOR

- **S = !(E1 + E2)**

E1	E2	S
0	0	1
0	1	0
1	0	0
1	1	0







Portas Lógicas CMOS

- Regras Básica para construção:
  - Considere que a equação lógica sempre seja negada. Caso esta seja positiva, ao final será necessário acrescentar um inversor na saída da porta.
  - Projete uma associação de transistores NMOS para a rede pull-down.
  - Construa a rede pull-up com configuração complementar a rede pull-down

Portas Lógicas CMOS

- **S = !(A + (B*C))**

1. **Considere que a equação lógica sempre seja negada**. (Caso esta seja positiva, ao final será necessário acrescentar um inversor na saída da porta).
2. **Projete uma associação de transistores NMOS para a rede pull-down.**
3. **Construa a rede pull-up com configuração complementar a rede pull-down**

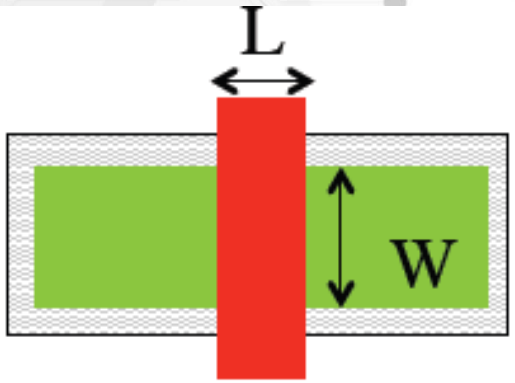
A	B	C	S
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Projeto Físico

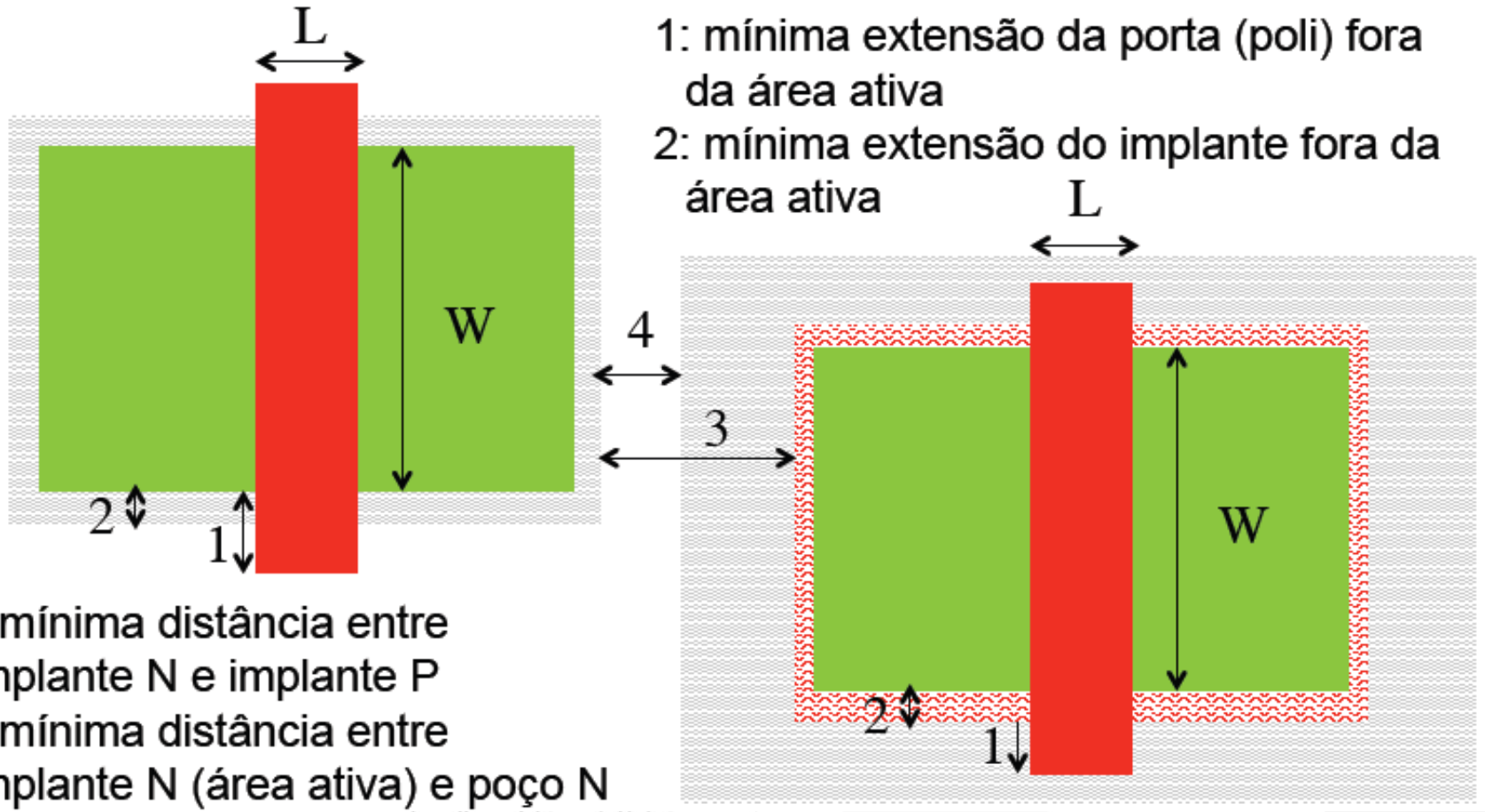
- Desenho do Leiaute das máscaras para fabricação do circuito integrado.
- Envolve:
  - Regras de Desenho (*design rules)*
  - Associações dos transistores
  - Posicionamento de transistores, fios e contatos

Regras de Desenho

- Definição das menores larguras e distâncias entre as camadas do leiaute
- Dimensões mais importantes
  - Comprimento do canal (L):
    - Em circuitos digitais, usualmente é o comprimento mínimo permitido pela tecnologia CMOS escolhida
  - Largura do canal (W):
    - Definido pelo projetista com base na área e no desempenho desejado



Regras de Desenho



1: mínima extensão da porta (poli) fora da área ativa

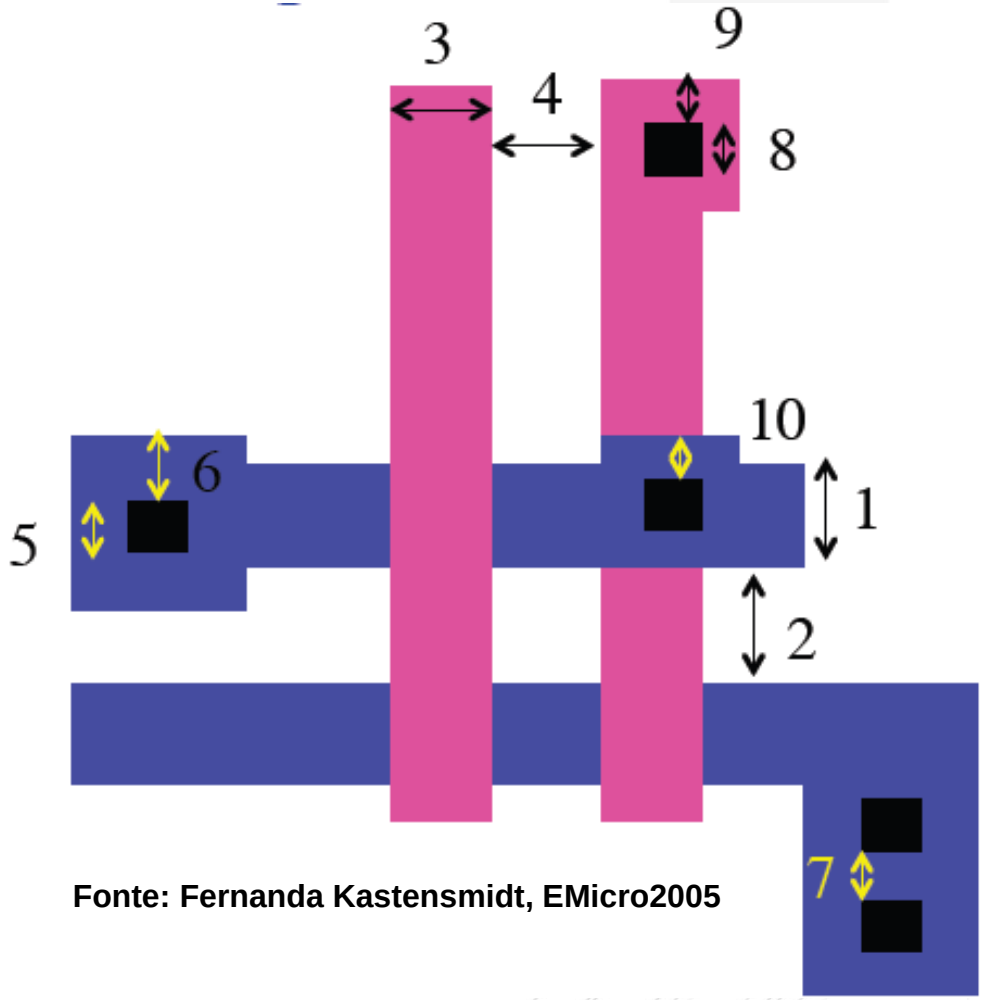
2: mínima extensão do implante fora da área ativa

3: mínima distância entre implante N e implante P

4: mínima distância entre implante N (área ativa) e poço N

Fonte: Fernanda Kastensmidt, EMicro2005

Regras de Desenho

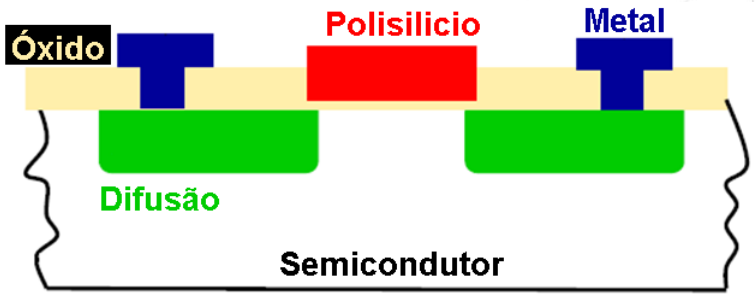


Fonte: Fernanda Kastensmidt, EMicro2005

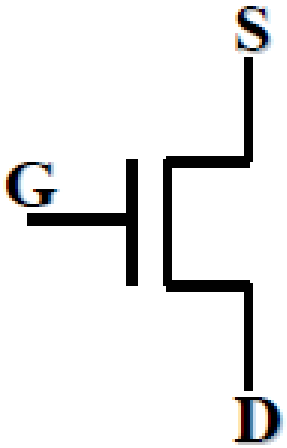
1: mínima largura de metal 1
2: mínima distância entre metal 1
3: mínima largura de metal 2
4: mínima distância entre metal 2
5: mínima largura do contado
6: mínima extensão de metal 1 para fora do contato
7: mínima distância entre contatos
8: mínima largura de via
9: mínima extensão de metal 2 para fora da via
10: mínima extensão de metal 1 para fora da via

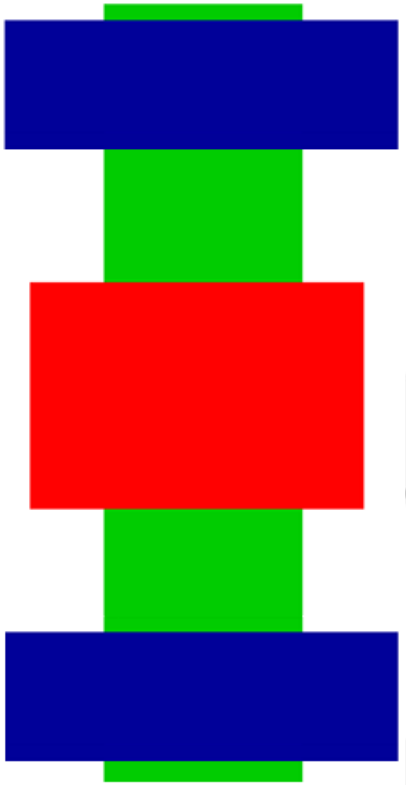
Leiaute Transistor MOS

Corte Transversal

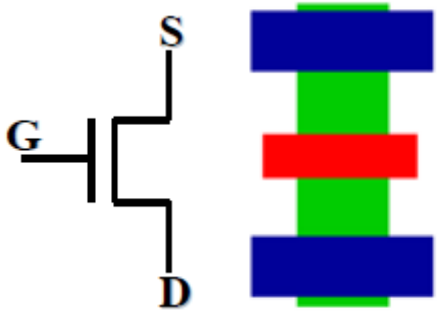


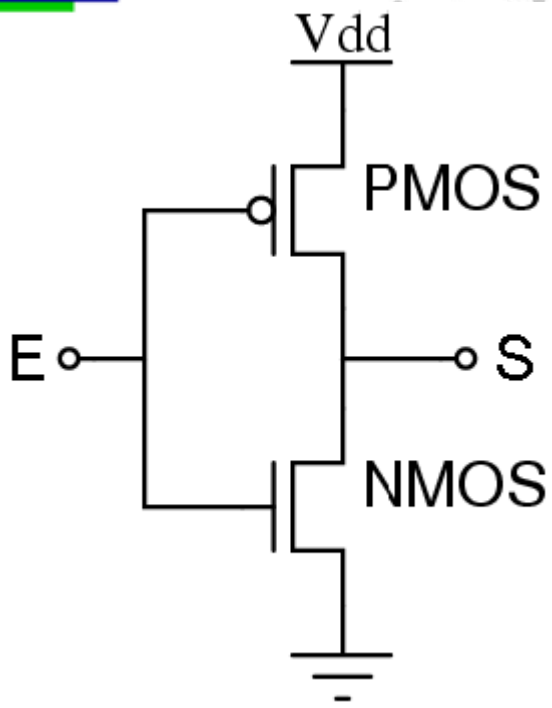
Leiaute

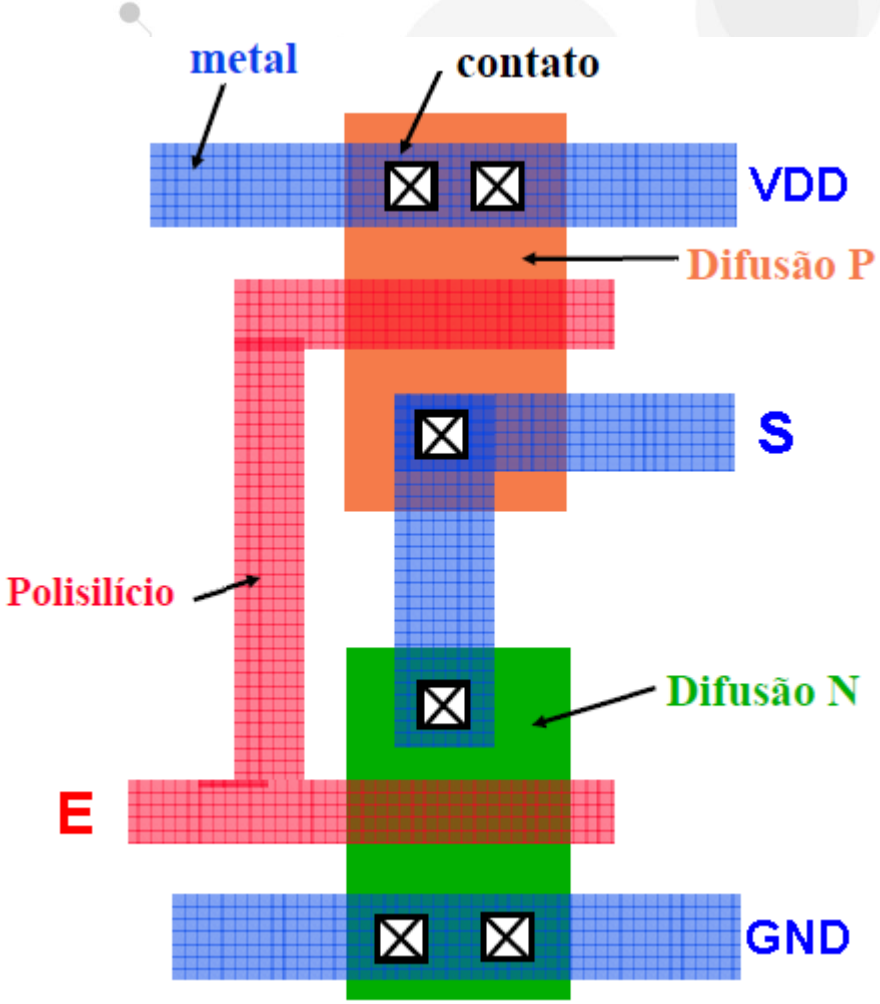




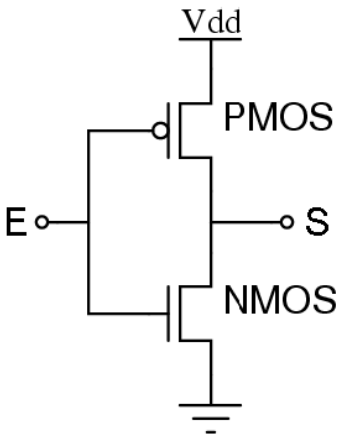
Inversor CMOS – Projeto Físico

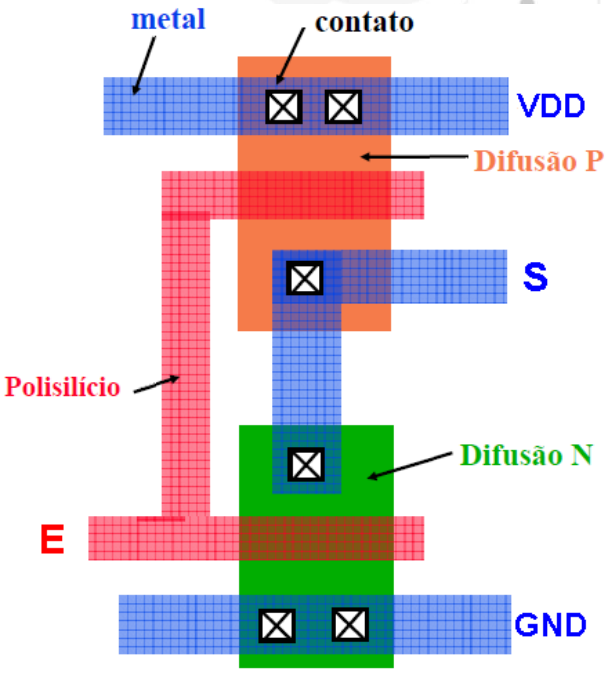


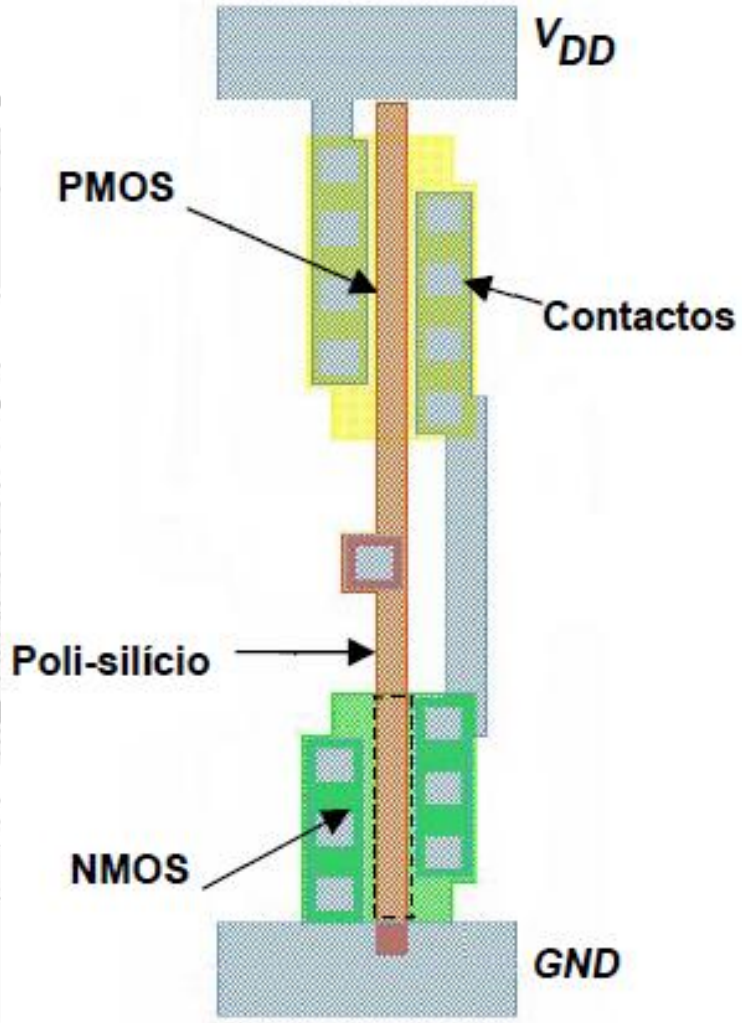




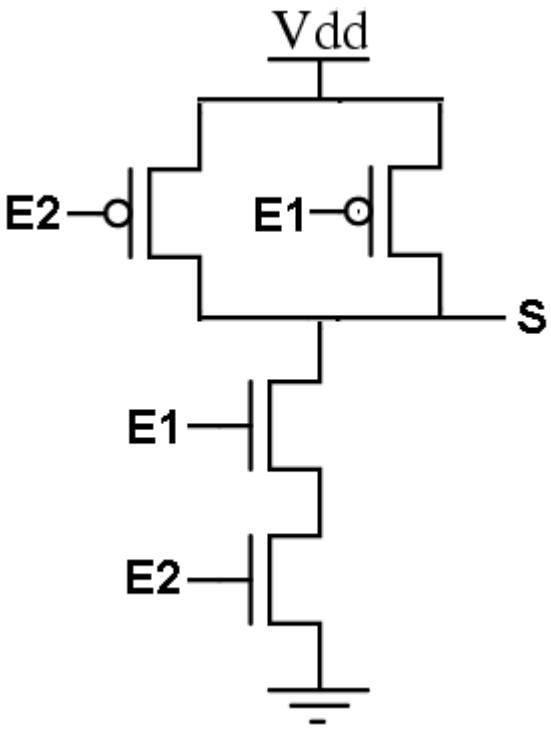
Inversor CMOS – Projeto Físico

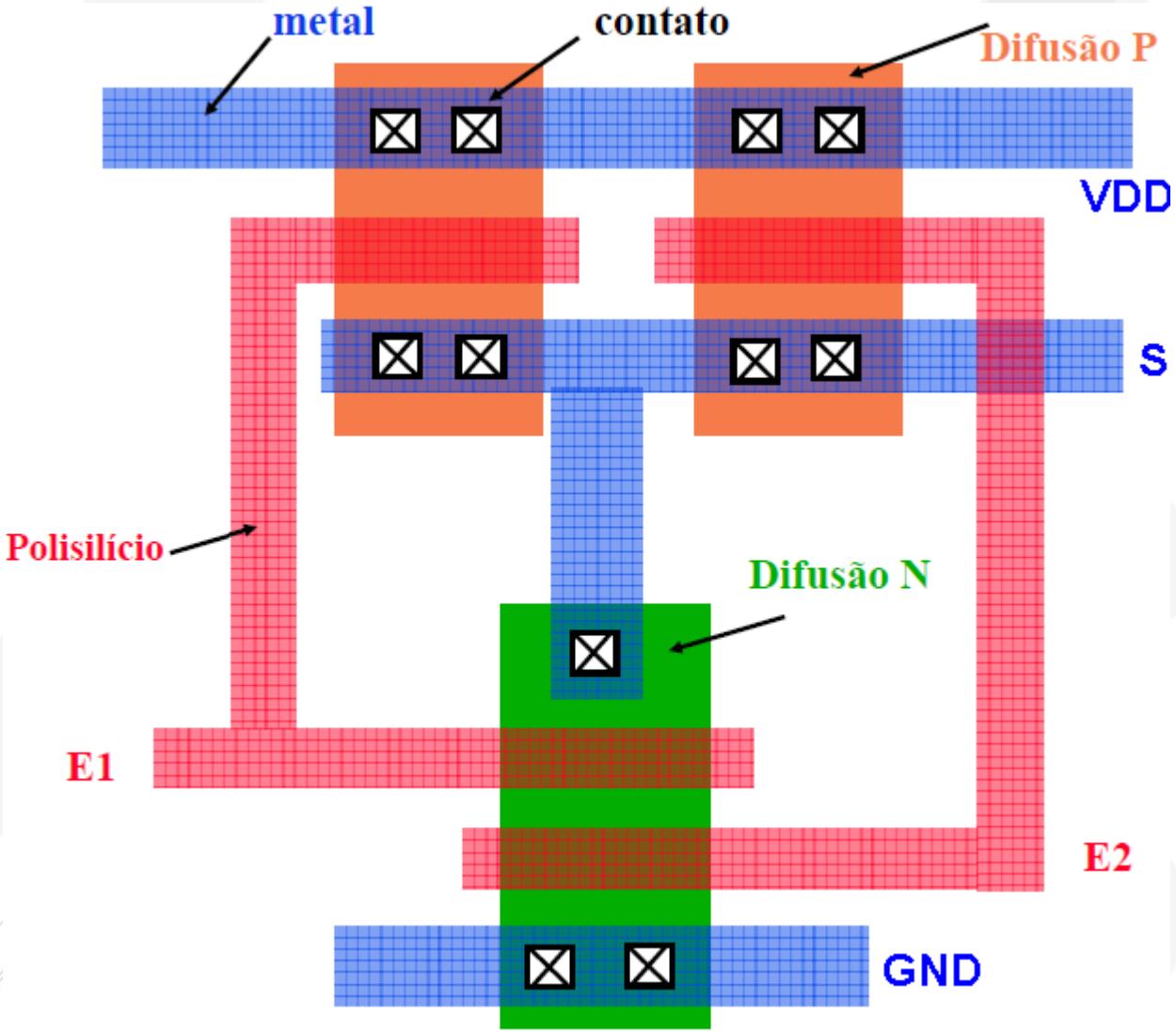






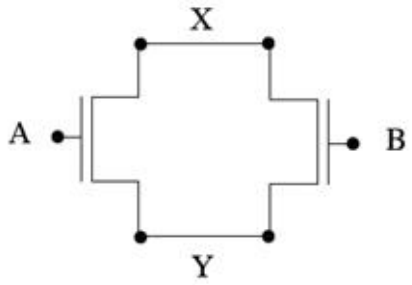
NAND CMOS – Projeto Físico

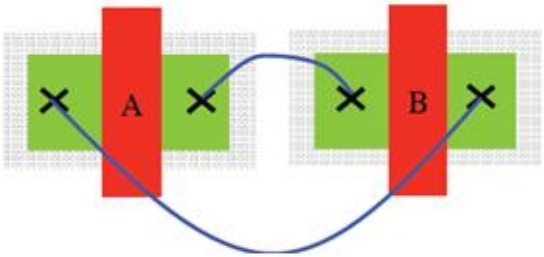


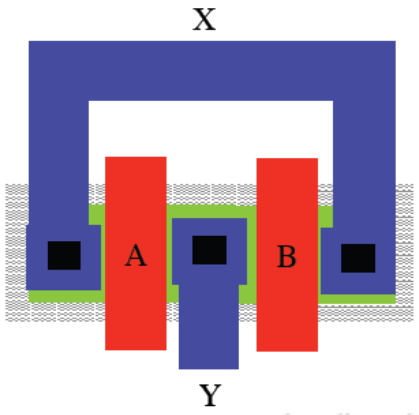


Compartilhamento de Difusão

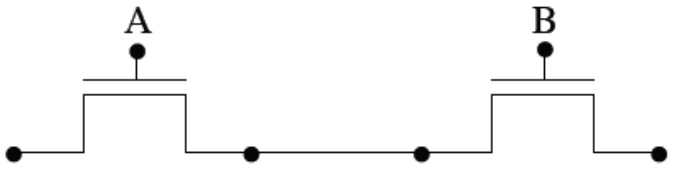
Transistores em Paralelo

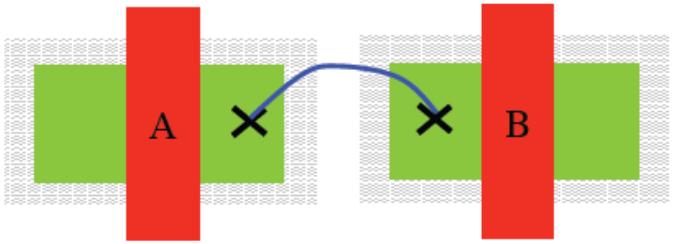


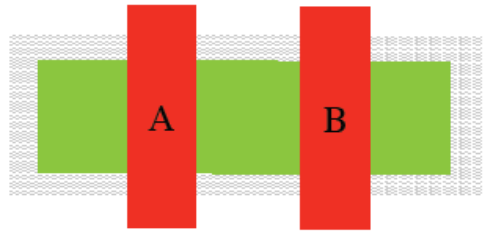




Transistores em Série



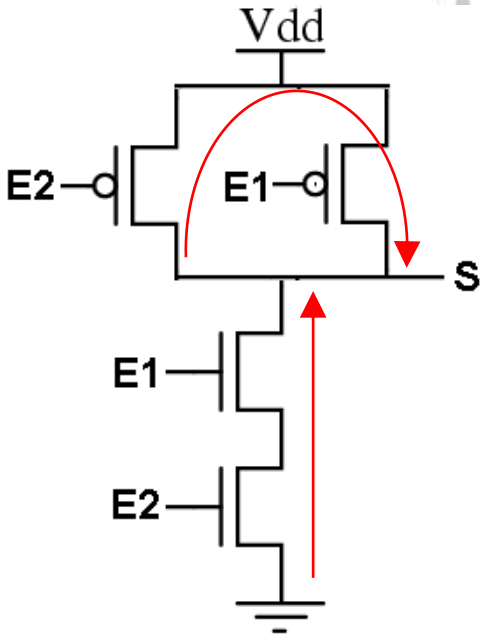


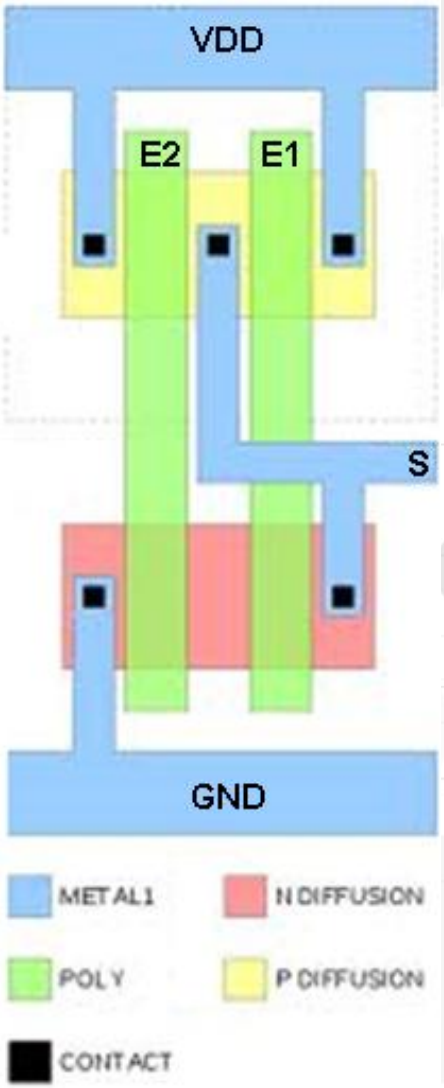


Fonte: José Guntzel, EMicro2010

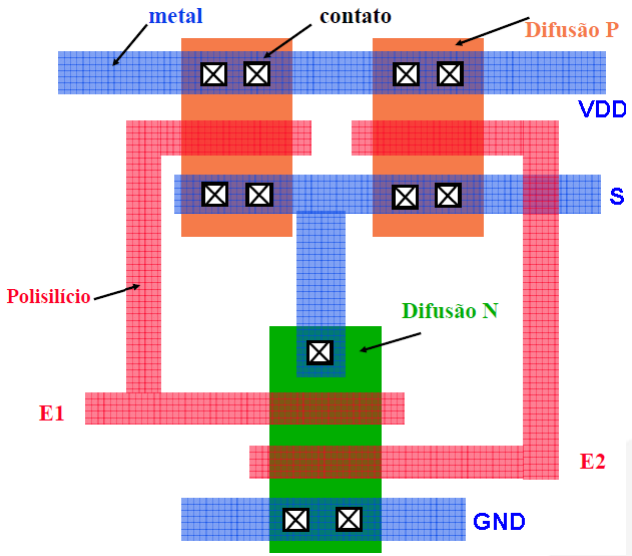
Caminho de Euler

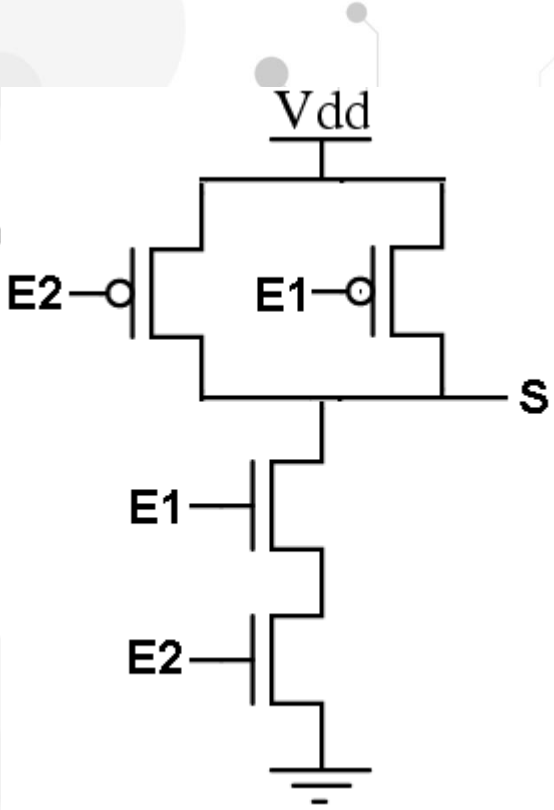
- É um caminho que passa por cada transistor do circuito exatamente um vez
  - # difusões = # caminhos
  - Casamento de Poli = Matching das entradas

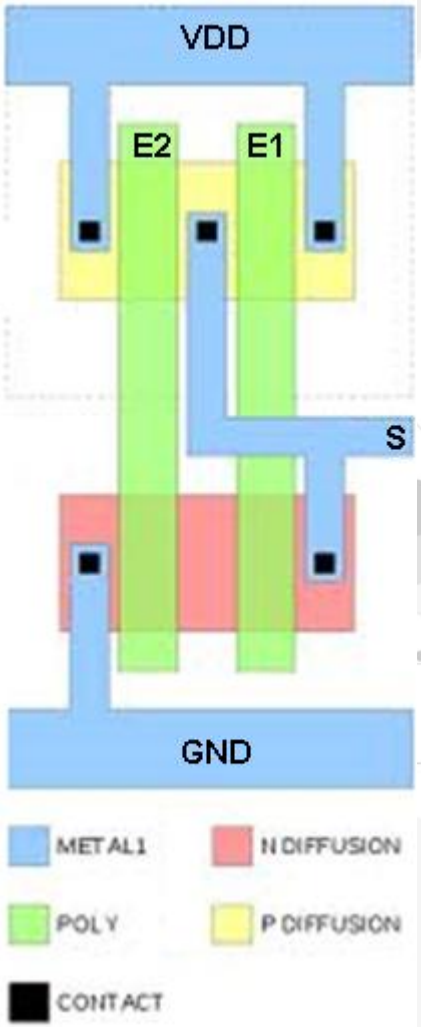




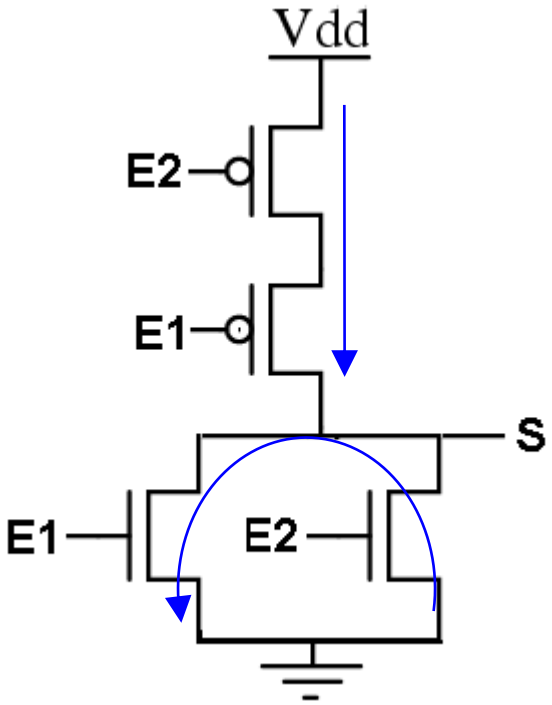
NAND CMOS – Projeto Físico

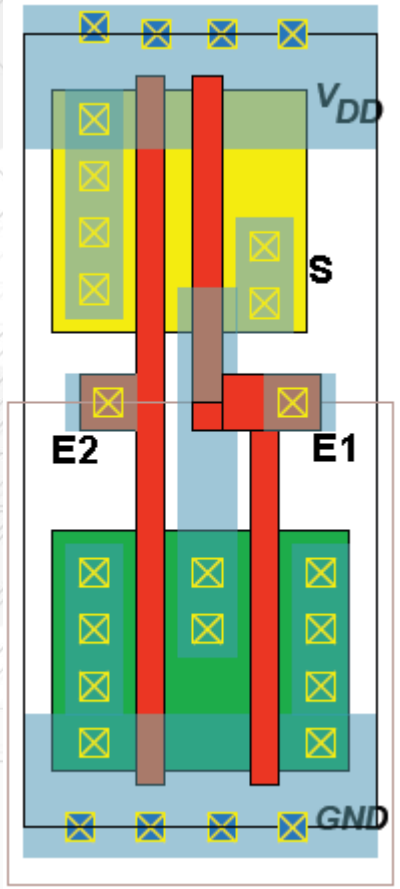




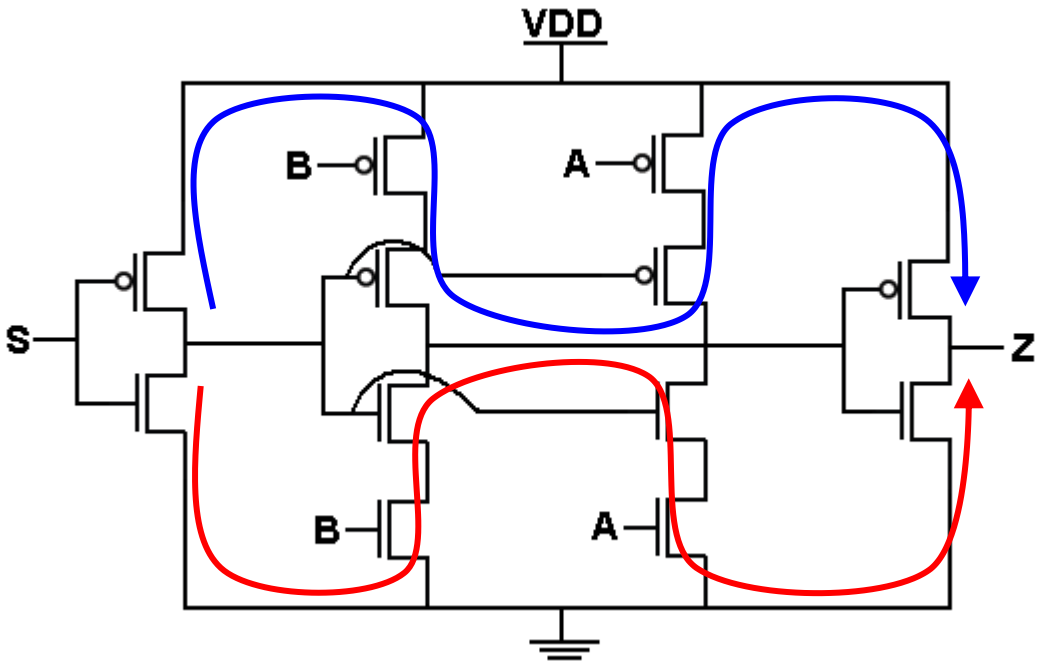


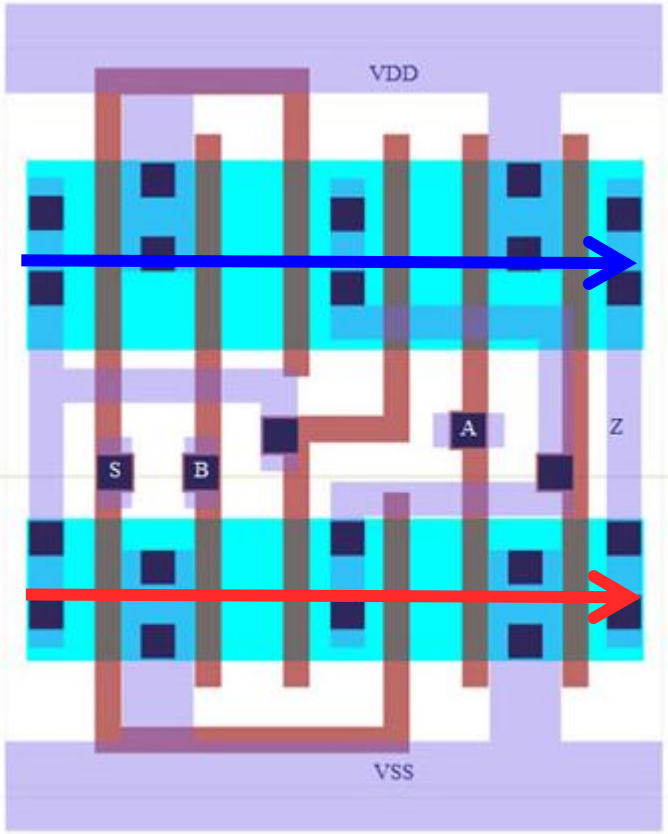
NOR CMOS – Projeto Físico



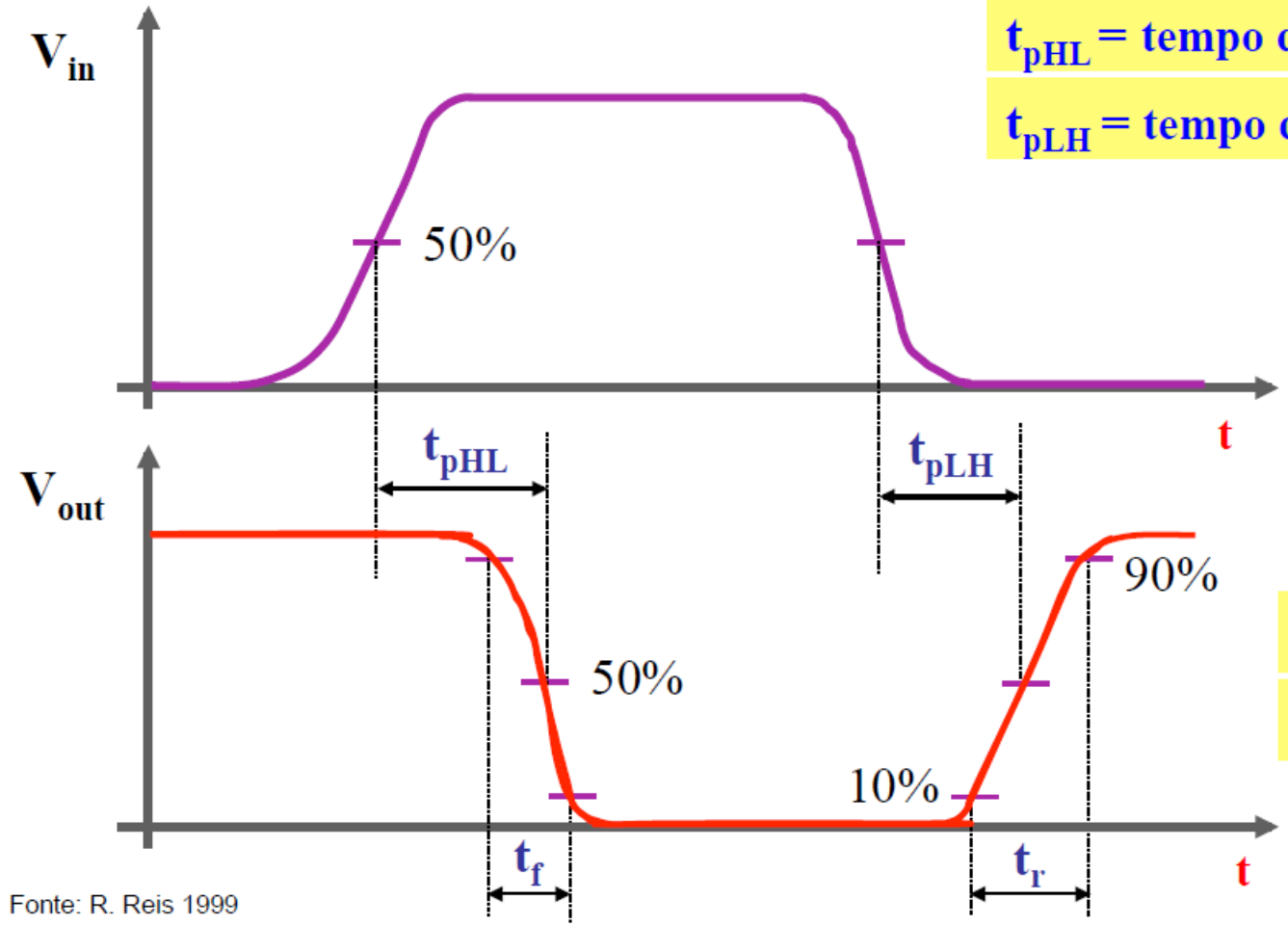


Porta Lógica Complexa





Características de Desempenho – Definição Atraso



Fonte: R. Reis 1999

t_{pHL} = tempo de propagação 1 ⇒ 0

t_{pLH} = tempo de propagação 0 ⇒ 1

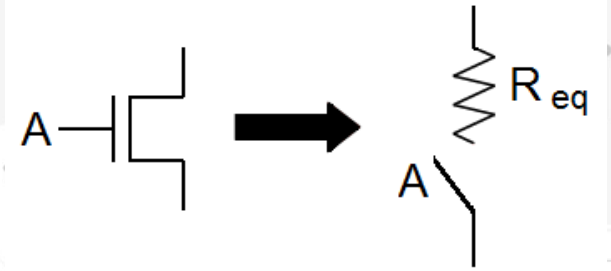
$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

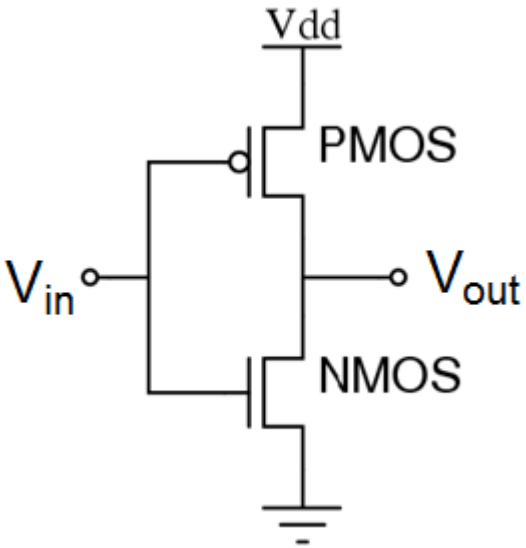
t_f = tempo de descida

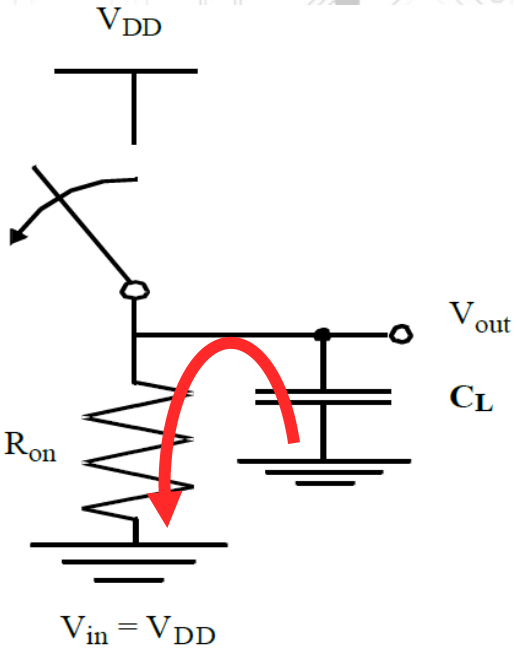
t_r = tempo de subida

Atraso de Propagação

- Aproximação por circuito RC

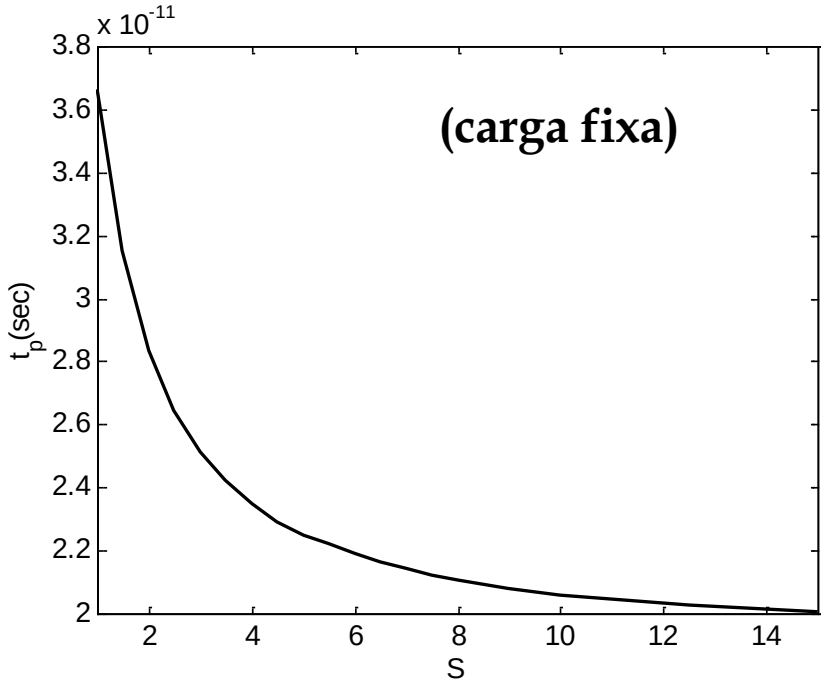






Atraso de Propagação

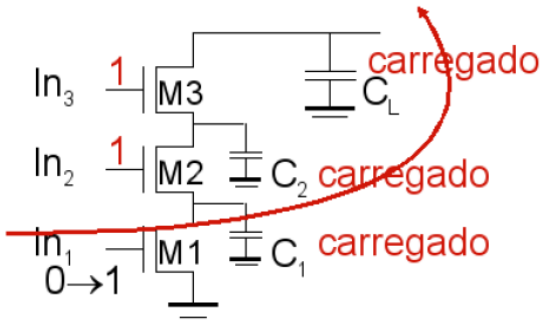
- Dependências do Atraso:
  - Tamanho dos transistores
    - Maior o W dos transistores → maior a capacidade de corrente → **Maior o desempenho**
      - Modelo RC: Maior o W → Menor R



Atraso de Propagação

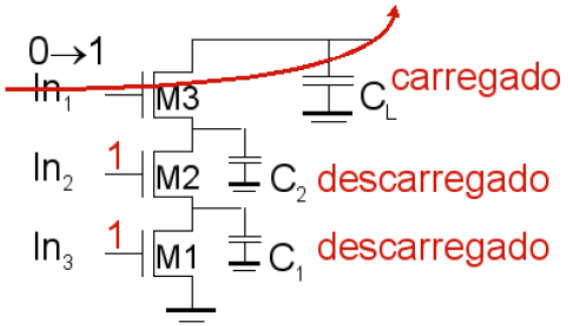
- Dependências do Atraso:
  - Capacitância de saída
    - Menor a capacitância de saída → Menor a quantidade de carga que deverá fluir pelos transistores → **Maior o desempenho**
      - Modelo RC: Maior Capacitancia de Saída → Maior C
  - Rede de transistores

caminho crítico



atraso determinado pela descarga de C_L, C_1 and C_2

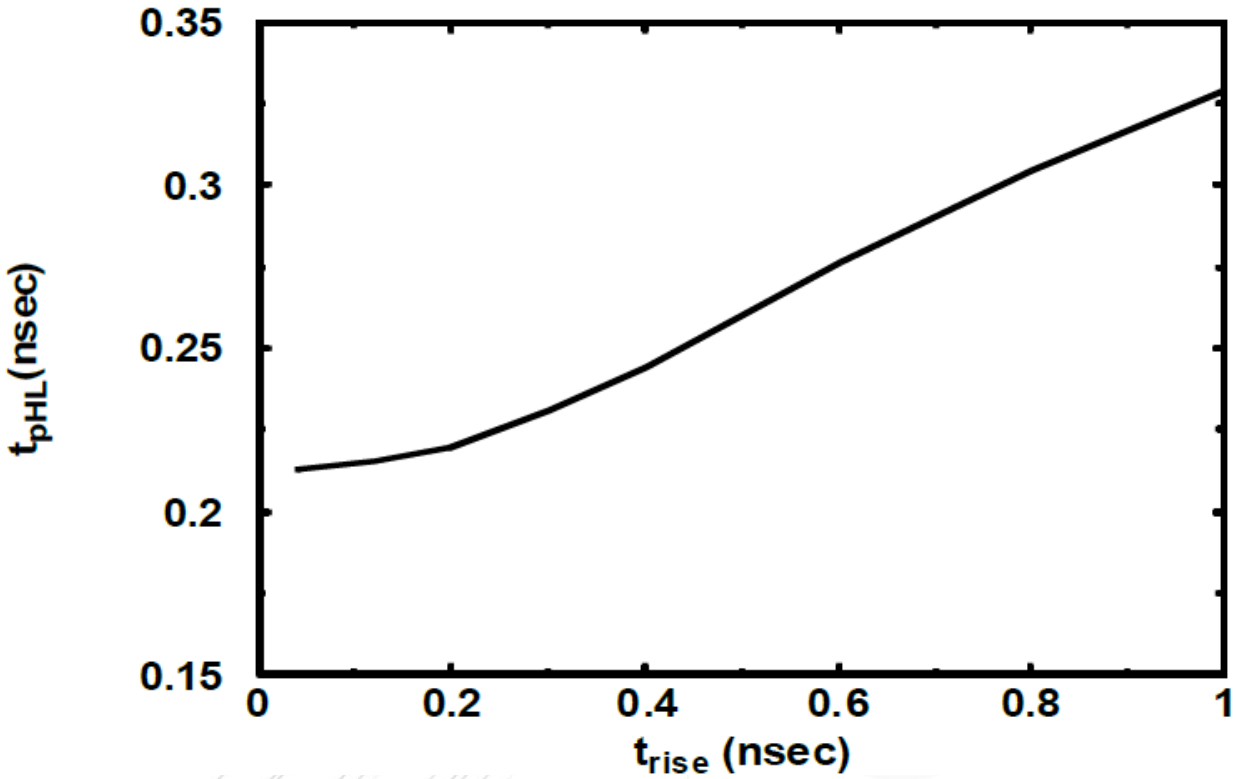
caminho crítico



atraso determinado pela descarga de C_L

Atraso de Propagação

- Dependência
  - Influência do slope do sinal de entrada
    - Desconsiderada na aproximação por circuito RC



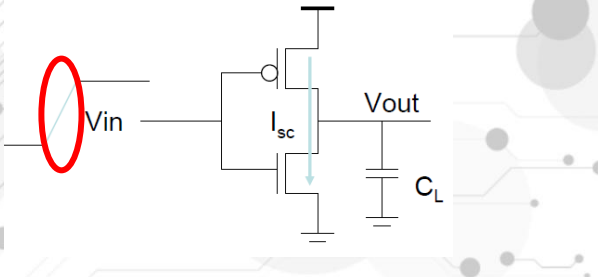
Característica de Potência – Definição de Potência

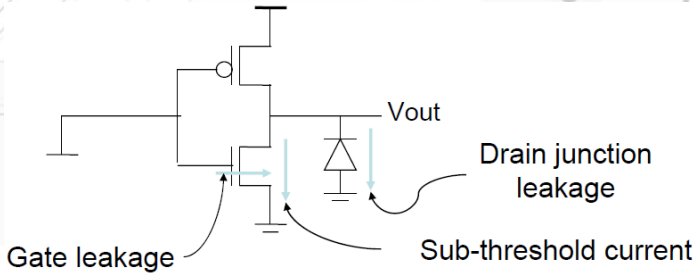
$$P_{total} = P_{dynamic} + P_{static}$$

$$P_{dynamic} = P_{switching} + P_{short\ circuit}$$

- $P_{switching}$ depende da carga e descarga das capacitâncias do circuito
- $P_{Short\text{-}circuit}$ ocorre quando ambas redes de transistores PMOS e NMOS estão parcialmente conduzindo durante uma transição
- P_{static} é o consumo indesejado quando o circuito não realiza nenhuma operação (dispositivo não ideal)

$$P_{switching} = \alpha C V_{DD}^2 f$$





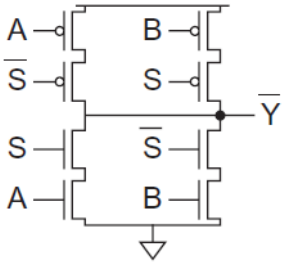
Característica de Potência – Low Power Design

- Redução da Potência Dinâmica
  - V_{DD}: utilizar a menor tensão de alimentação possível
  - α: evitar chaveamentos desnecessários
    - clock gating, sleep mode
  - C: transistores menores, fios de roteamento mais curtos
  - f: utilizar a menor frequencia possível

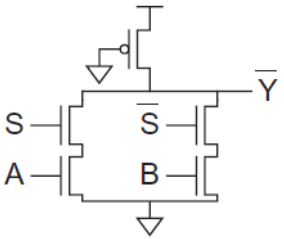
- Redução da Potência estática
  - Uso "seletivo" de transistores com baixa tensão de limiar (V_{th})
  - Explorar técnicas de redução:
    - Transistores em série (stack effect)
    - Polarização do substrato
    - Redução da temperatura

Outras Famílias Lógicas

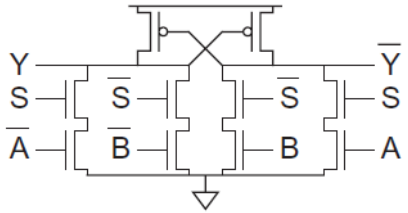
Static CMOS



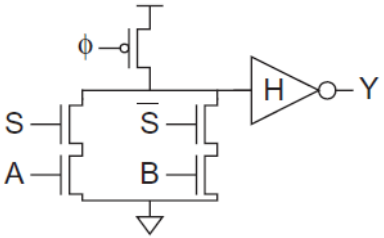
Pseudo-nMOS



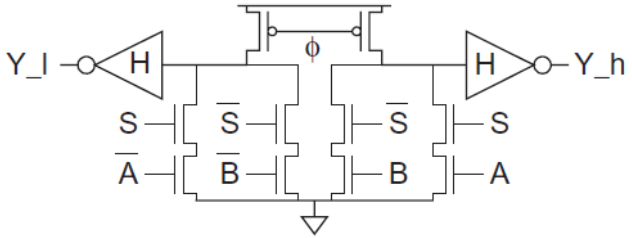
CVSL



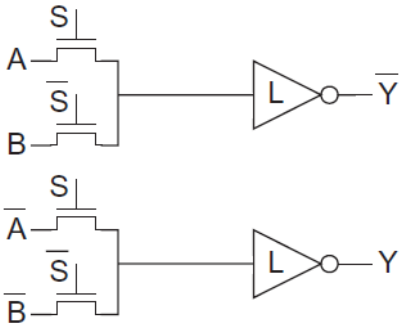
Domino



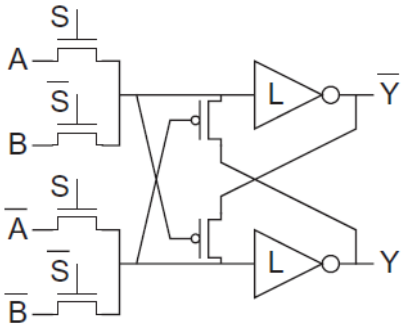
Dual-Rail Domino



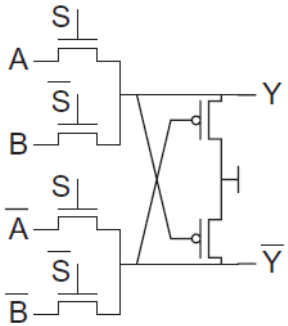
CPL



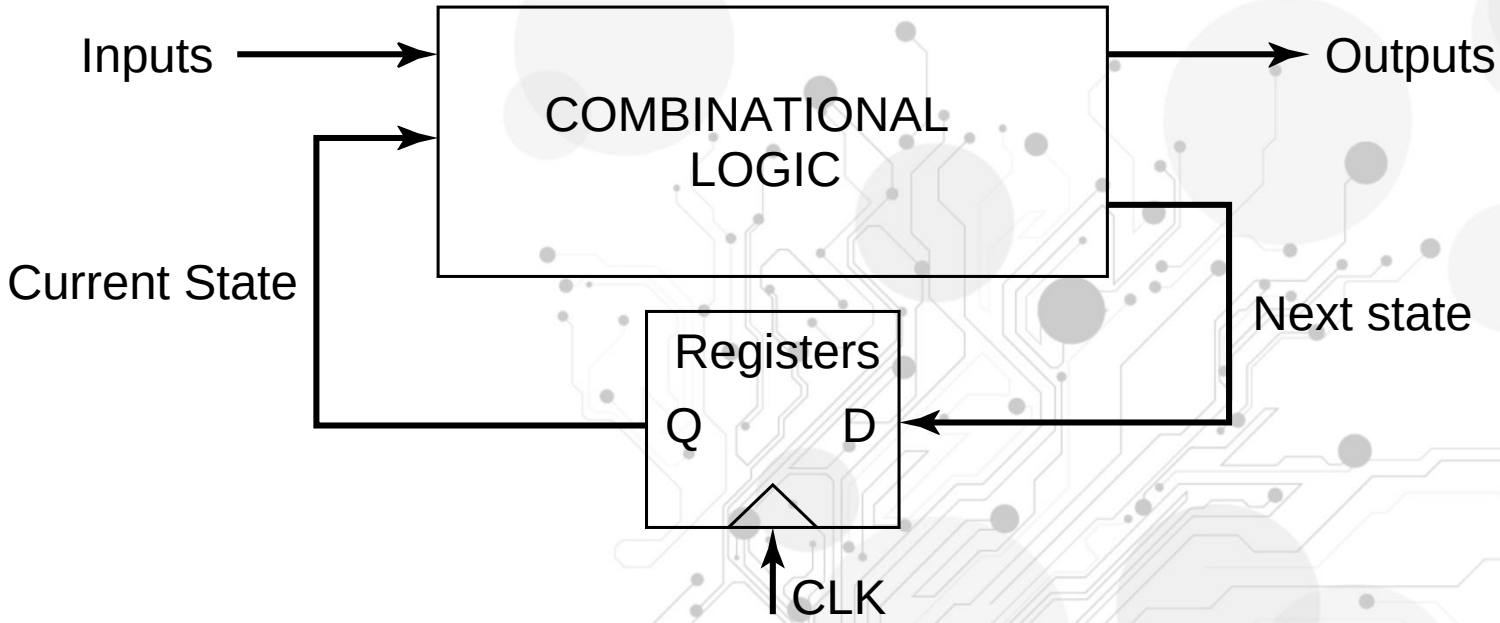
EEPL



DCVSPG

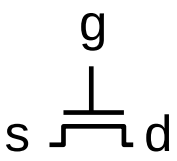


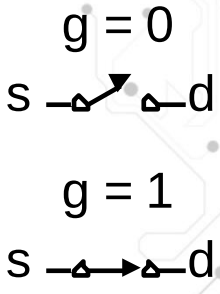
Circuitos Sequenciais

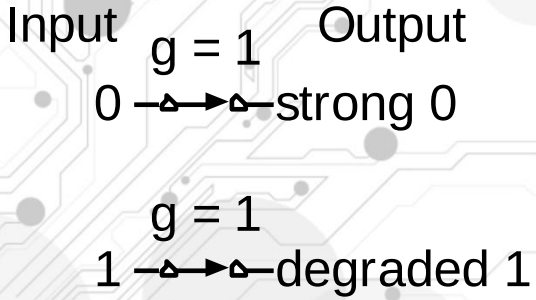


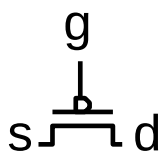
- Cruciais em circuitos síncronos
  - Desempenho / área / Potência
- 2 mecanismos de armazenamento
  - Feedback positivo (Inversor de realimentação)
  - "Charge-based" (Alta impedância)

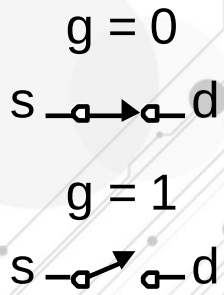
- Pass Transistors
  - Transistores (literalmente) utilizados como chaves

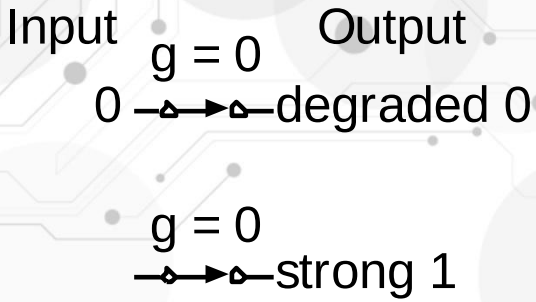




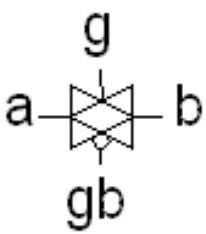


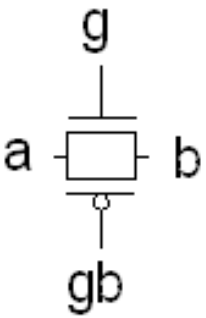




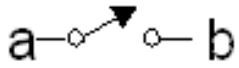


- Transmission gates

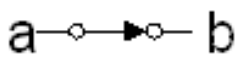




g = 0, gb = 1



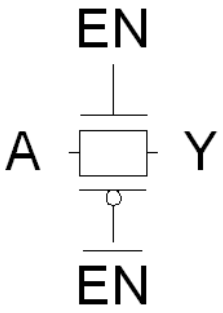
g = 1, gb = 0

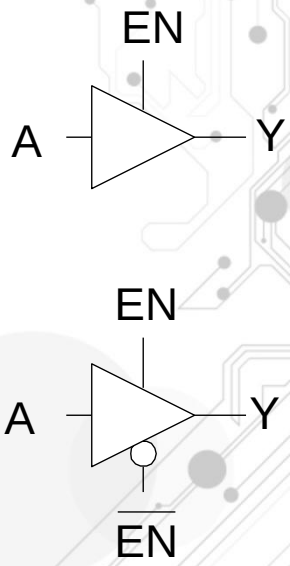


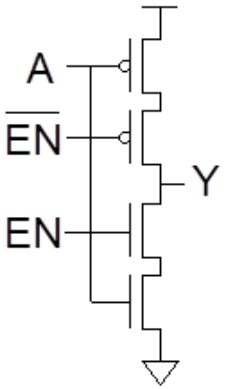
Input	Output
g = 1, gb = 0	
0	strong 0
g = 1, gb = 0	
1	strong 1

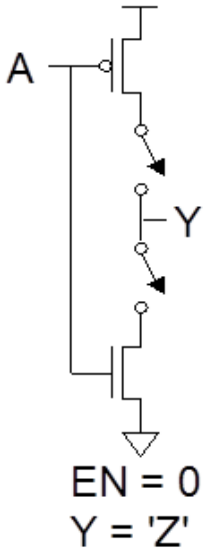
- Inversor Tri-State
  - Saída em Alta impedância quando EN = 0

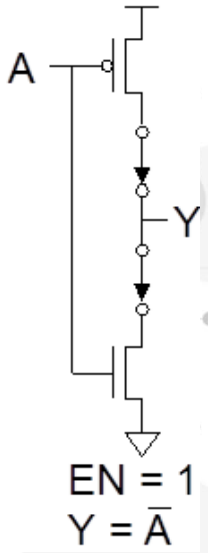
EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1







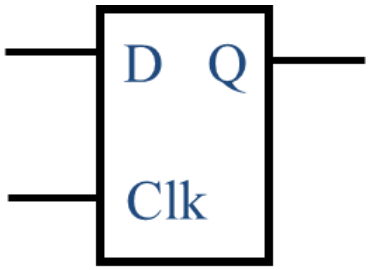


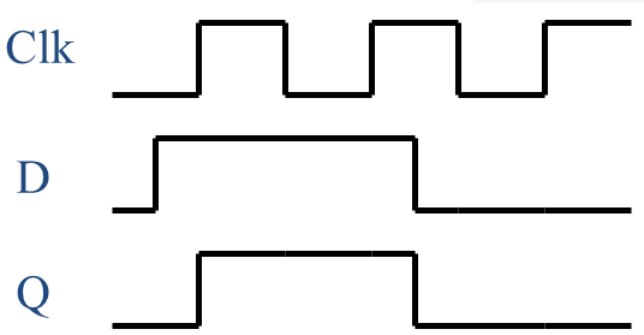


- Latch versus Register/Flip-Flop

Latch – Sensível a nível

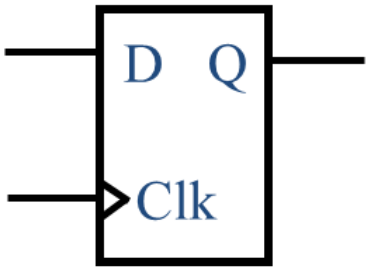
Positive Level Sensitive Latch

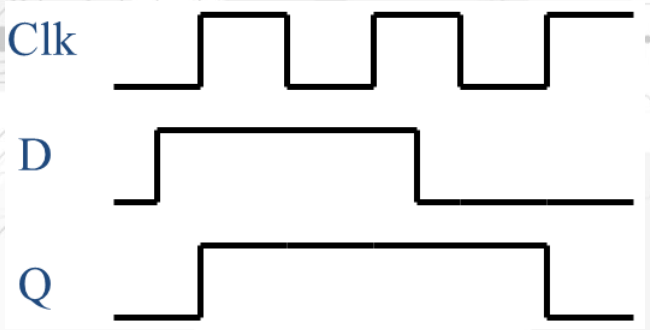




Flip-Flop – Sensível a borda

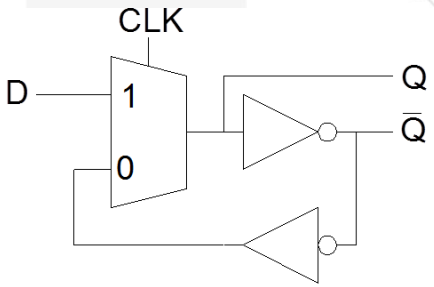
Positive Edge Sensitive Flip-Flop

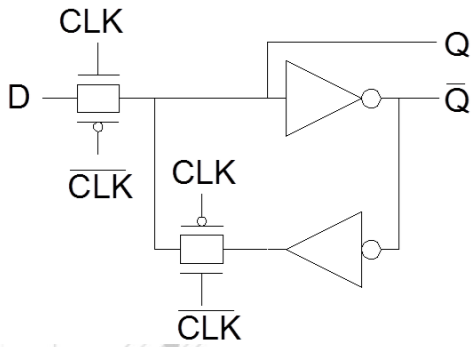




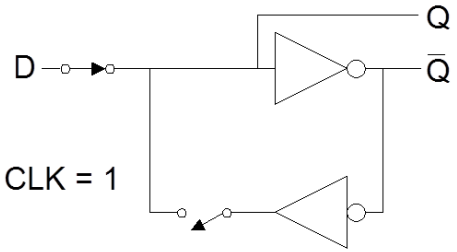
Circuitos Sequenciais

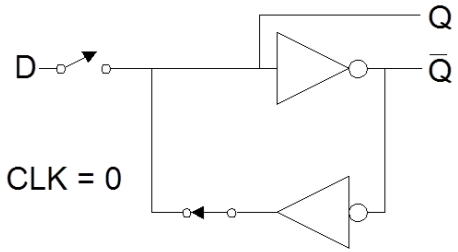
- Projeto Latch D

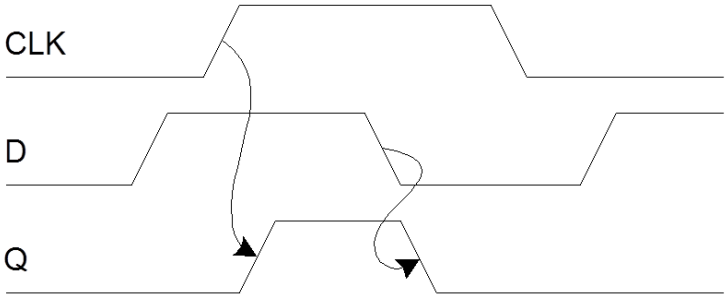




- Operação Latch

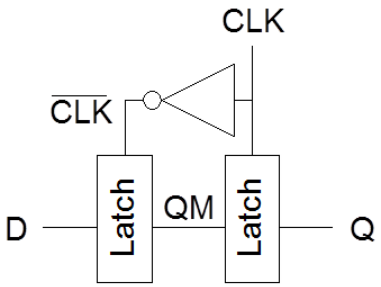


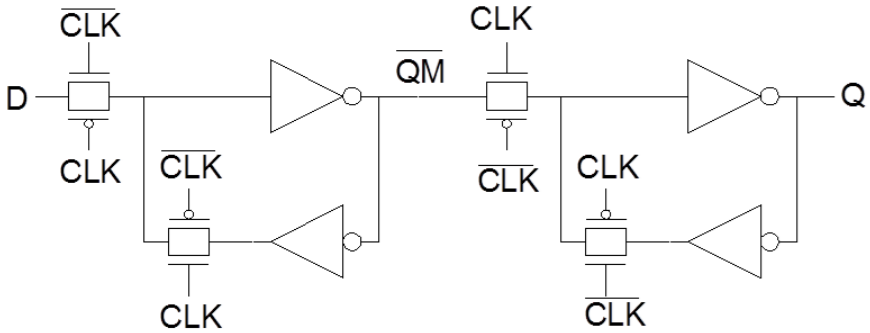




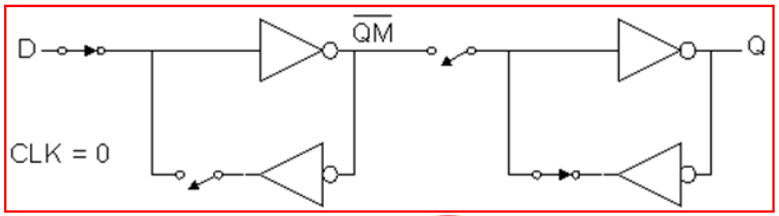
Circuitos Sequenciais

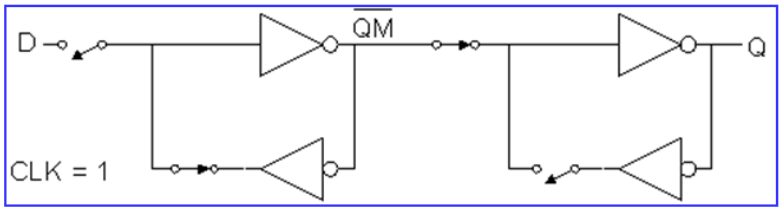
- Projeto Flip-Fl

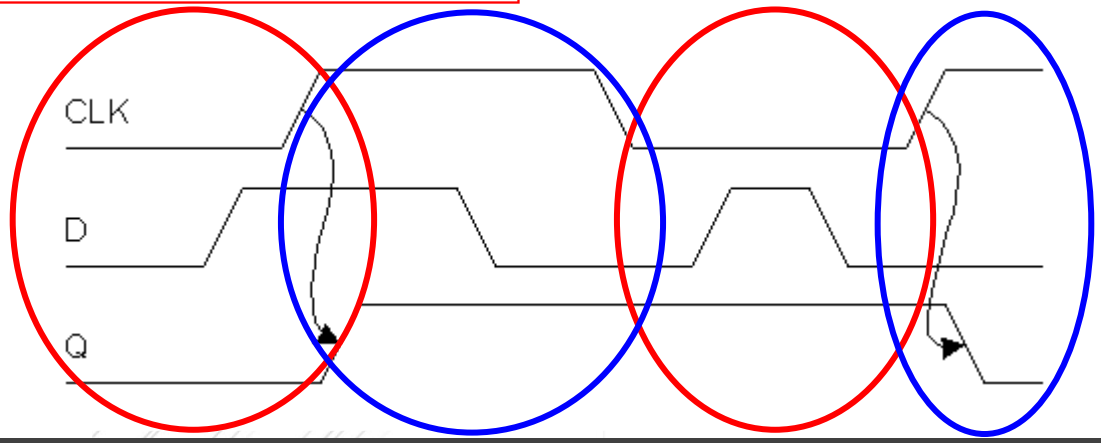




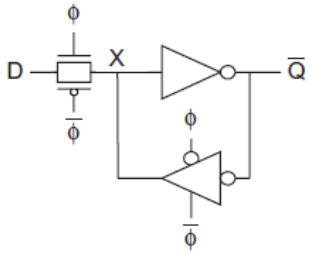
- Operação Flip-Flop

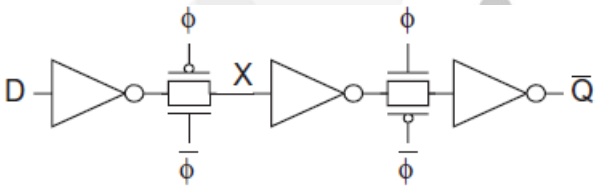


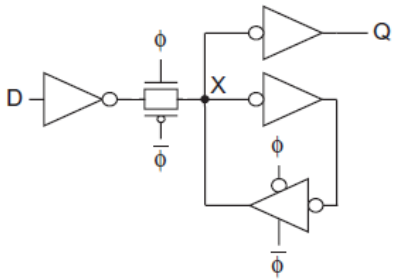


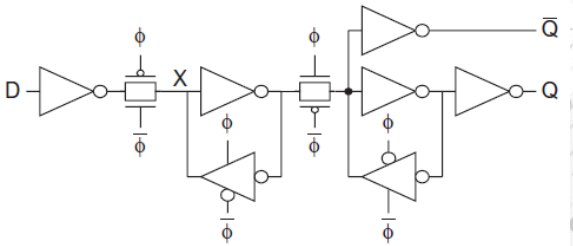


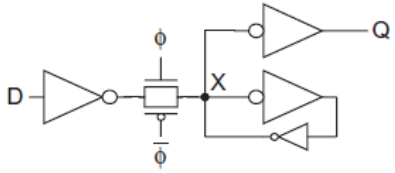
Circuitos Sequenciais

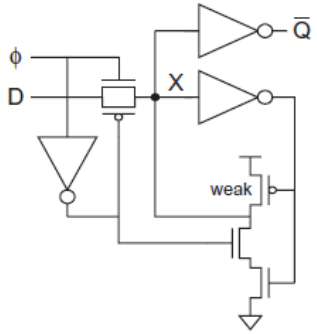


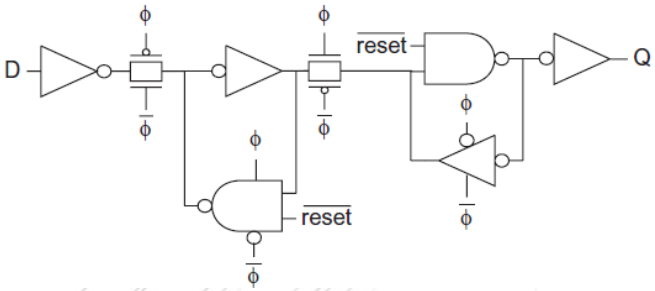


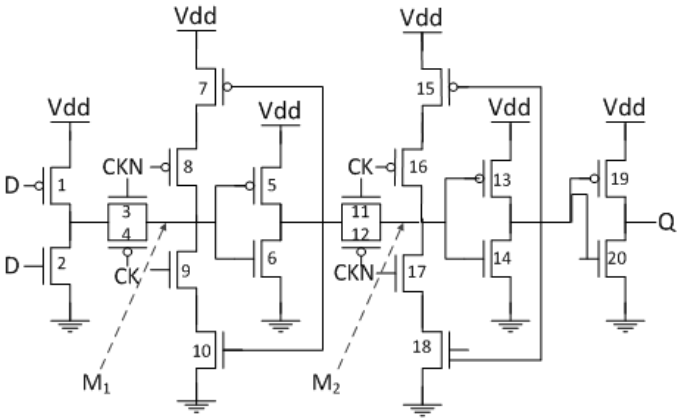


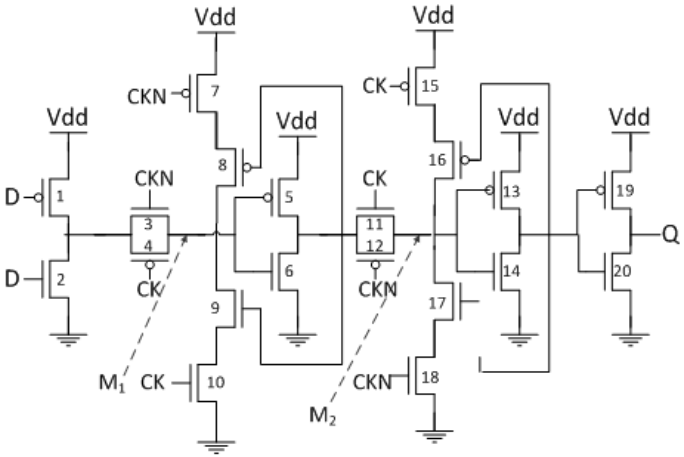












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- WESTE, Neil; HARRIS, David. CMOS VLSI Design: a circuits and systems perspective. Addison-Wesley, 3nd Edition, 2004.
- UYEMURA, John P. CMOS Logic Circuit Design. Kluwer Academic Publishers, February 1999.

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Porto Alegre, 29 de abril a 3 de maio de 2013

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