Parallel Characterization of Operational Amplifiers for Acceleration of Design Optimization

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1 - Analog Design Automation

- Analog circuit design is a time consuming task due to the complex relations between performance and circuit parameters
- A design have a set of variables W, L and V_{bias}/I_{bias} for a specific application that need to be find
- We can find the value of these variables in two ways:
  - Manual design; Optimization design
- The optimization tools use artificial intelligence to explore the design space in order to find optimized solutions
- The inputs of these tools are
  - Initial solution for the circuit; Design specifications; Fabrication technology
- Based in these inputs the optimization methodology provides values for the circuit variables. These values are design possible solutions

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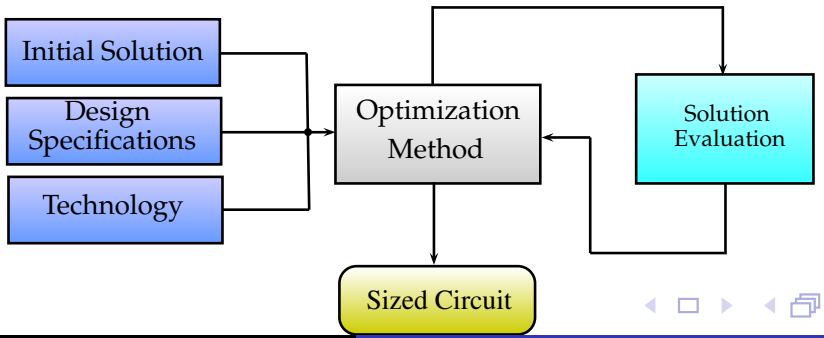

2.1 - Evaluation Process

- In the UCAF tool, the solution evaluation is made by means of a cost function

$$f_c = \sum_{i=1}^{n} P_{O_i}.S_i + \sum_{j=1}^{n} P_{R_j}.f(S_j)$$

- The first sum represents the objective part of the cost function and the second sum is the constraints part
  - S_i is the i^{th} specification of the circuit to be optimized
  - S_j is the j^{th} specification of the circuit that is constrained in a maximum or minimum value
  - P_{O_i} and P_{R_j} are values used as weighting purpose
  - $f(S_j)$ is the constraint function used to measure the distance between the required value and the reached value for the specifications

- The more important part of the solution evaluation is the specification estimation, because the metric to the heuristic design exploration is the values of the specifications

2.2 - Evaluation Process

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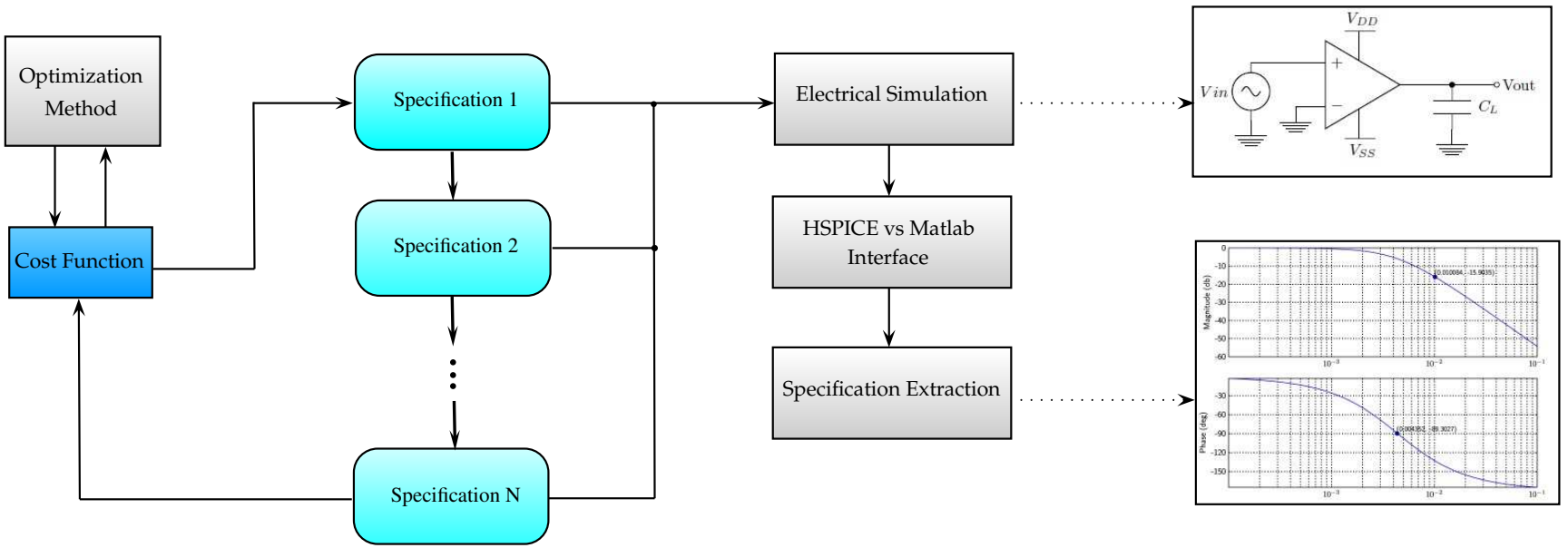
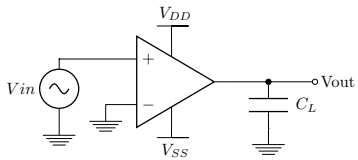


2.3 - Evaluation Process

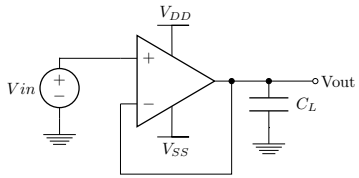
- It is necessary to perform electrical simulation and specification extraction for each testbench in order to measure the required specification
- This task is executed several times in the optimization process
- Most execution time is spent in the circuit characterization
- All specifications are dependent on the generated solution and independent on each other
- It allows the execution of all circuit simulations in each iteration in parallel form

3 - Testbench Implementations and Parallelization

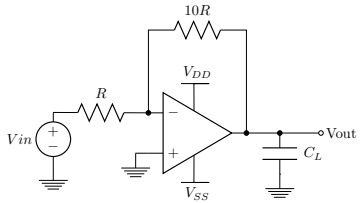
- In this context, this work proposes a set of standard characterization testbenches to evaluate circuit specifications in a automatic sizing tool
- Parallelization of circuit evaluation
- Time reduction of circuit simulation



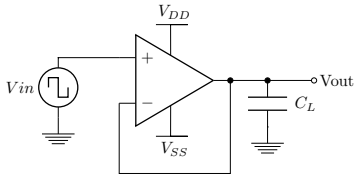
(a) AC open loop



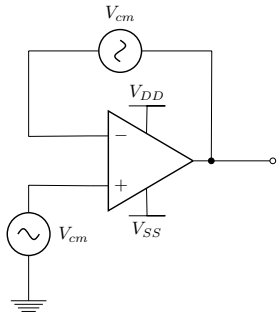
(b) ICMR



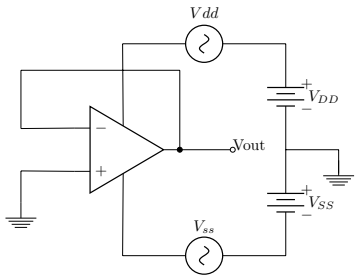
(c) Output Swing



(d) Slew Rate



(e) CMRR



(f) PSRR

4 - Design Analysis

- As an example of using the proposed characterization method, the design of a two-stage CMOS OTA Miller in 0.25 μm TSMC technology

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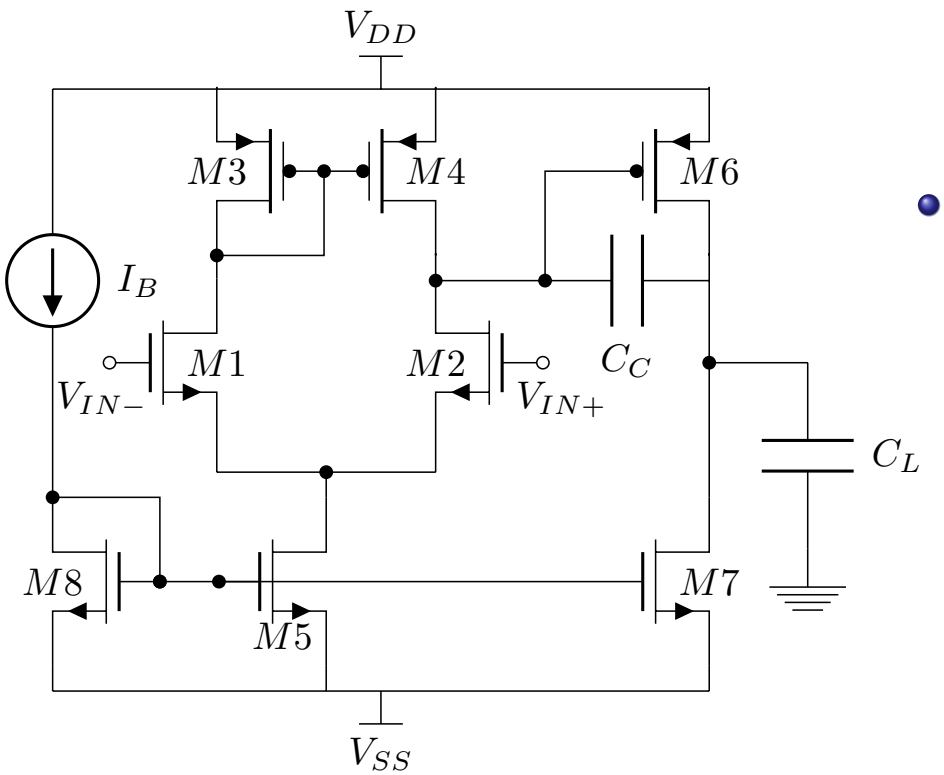

- Must be matched:
  - differential pair M1-M2
  - current mirror M3-M4 and M5-M8
- Free variables:
  - W_1, L_1, W_3, L_3, W_5, L_5, W_6, L_6, W_7, L_7, I_B and C_c

4.1 - Serial Results

- The proposed circuit is simulated in
  - 8 core Intel i7 processor
  - 8GB RAM
  - Simulated Annealing Algorithm as optimization heuristic
  - Serial

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- The obtained results

Table : Specifications of OTA Miller Design

Specifications	**Required Value**	**Obtained Value**
A_{v0} (dB)	$\geq$ 70.00	81.62
GBW (MHz)	$\geq$ 2.00	2.67
PM (^{o})	$\geq$ 50.00	78.01
OS (V)	$\geq$ 2.00	2.33
CMRR (dB)	$\geq$ 70.00	78.58
PSRR+ (dB)	$\geq$ 70.00	84.61
PSRR- (dB)	$\geq$ 70.00	80.60
SR (V/μs)	$\geq$ 1.50	4.35
P_{diss} (μW)	Minimize	744.50
Execution Time (min)	-	1194

4.2 - Parallel Results

- To analyze the influence of parallel execution in the optimization process, the previous design was repeated using parallel simulations
- The number of cores was set in 1, 2, 3, 4 and 6
- As the design needs a maximum of 6 testbenches to evaluate the solution the maximum number of cores is 6

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Table : Execution time and Speedup of the parallel simulations

Cores	Execution Time(min)	Speed up
1	1194	-
2	616	1.94
3	539	2.22
4	447	2.67
6	308	3.88

5 - Conclusions and Future Work

- The proposed method for operational amplifier automatic characterization presented good results when included in an automatic sizing tool.
- As the electrical simulations in each optimization iteration are independent, they can be executed in parallel
- The execution time is reduced up to 3.88 times in relation to the sequential version
- Saving more than 14 hours in the optimization design space exploration time
- As future work we intent
  - Insert new testbenches in the simulation environment
  - Expand the methodology to other analog circuits

Acknowledgment

Thank You for your attention !

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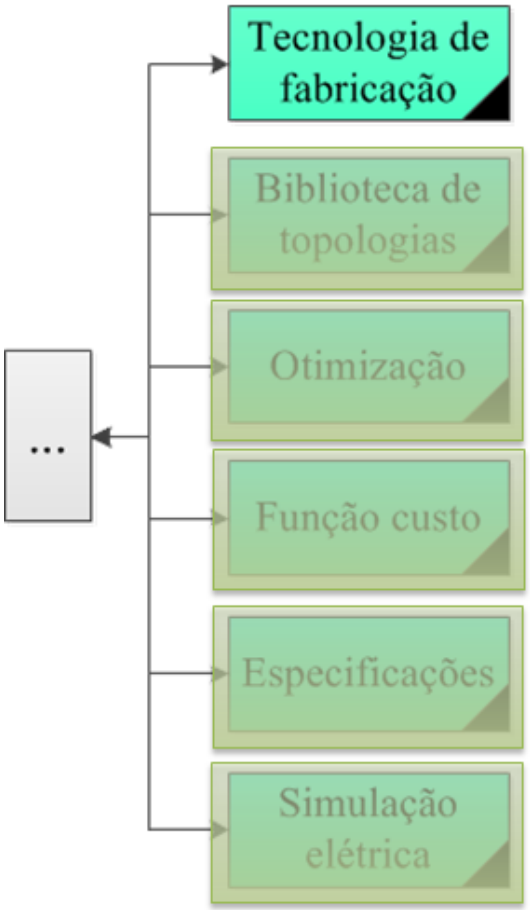
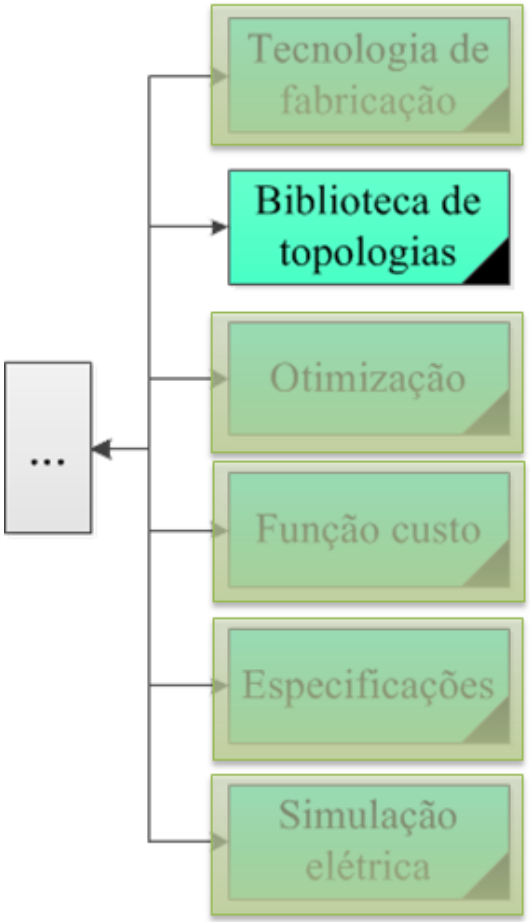


UCAF

- **Dados da tecnologia de fabricação:**
  - Parâmetros do modelo elétrico
  - Dimensões mínimas e máximas dos transistores
- **Ferramenta é capaz de trabalhar com qualquer modelo de tecnologia, desde que o simulador elétrico seja compatível.**

- **Dados:**

Diretório com os arquivos de parâmetros.



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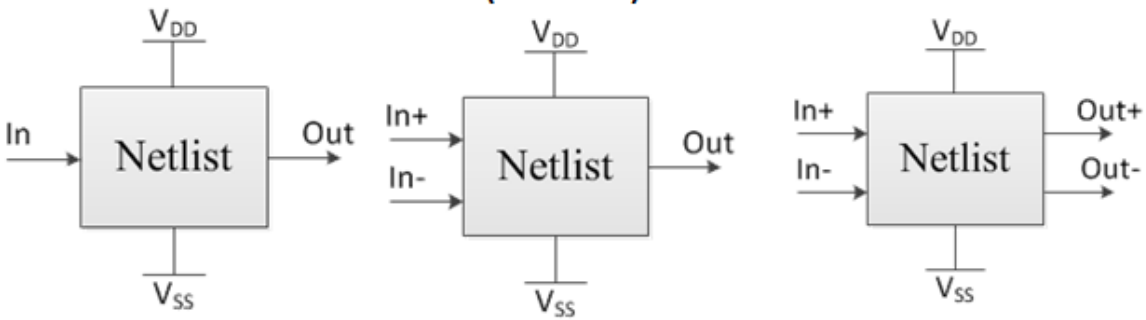
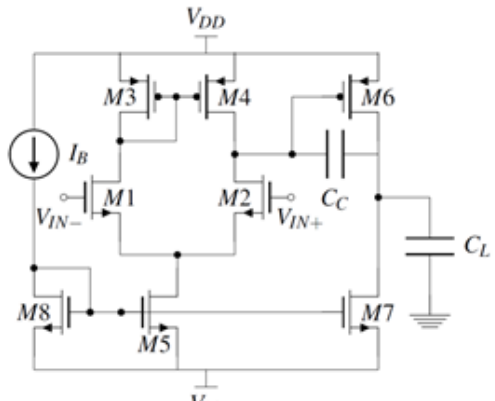
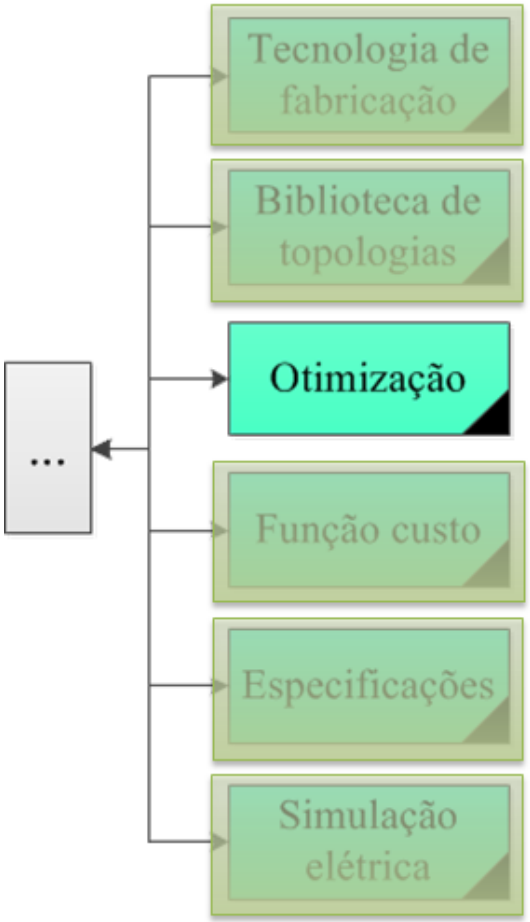
- **Topologias de circuitos que será projetado com a ferramenta:**
  - Inserção de novas topologias
  - Nível elétrico (Netlist)






```
1.  *NETLIST OTA MILLER
2.    .lib 'xh018/lp3mos/xh018.lib' tm
3.    .subckt OTA_miller vp vn vdd vss vout
4.    X1 2 vn 3 3 ne w='W1*1e-6' l='L1*1e-6'
5.    X2 5 vp 3 3 ne w='W1*1e-6' l='L1*1e-6'
6.    X3 2 2 vdd vdd pe w='W3*1e-6' l='L3*1e-6'
7.    X4 5 2 vdd vdd pe w='W3*1e-6' l='L3*1e-6'
8.    X5 3 4 vss vss ne w='W5*1e-6' l='L5*1e-6'
9.    X6 vout 5 vdd vdd pe w='W6*1e-6' l='L6*1e-6'
10.   X7 vout 4 vss vss ne w='W7*1e-6' l='L7*1e-6'
11.   X8 4 4 vss vss ne w='W5*1e-6' l='L5*1e-6'
12.   Ibias vdd 4 'IB*1e-6'
13.   Cc 5 vout 0.3p IC=0
14.   Cl vout 0 3p IC=0
```



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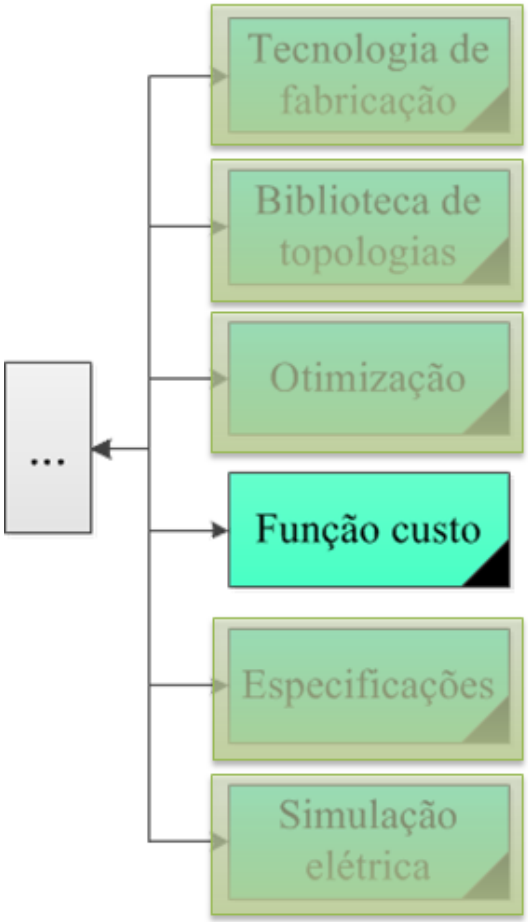
- **Técnicas de inteligência artificial de otimização para exploração do espaço de projeto**
- **Técnicas aplicadas na ferramenta:**
  - **Algoritmos Genéticos**
    - *GAOT* (Genetic Algorithms Optimization Toolbox)[1]
  - **Simulate Annealing**
    - Matlab Optimization Toolbox®
  - ***fmincon* (Busca Local)**
    - Matlab Optimization Toolbox®
    - Método de Pontos Interiores[2]

[1]HOUCK, C.; JOINES, J.; KAY, M. A genetic algorithm for function optimization: A matlab implementation. NCSU-IE TR 95-09, 1995.
[2] PRESS, W. et al. Numerical recipes: The art of scientific computing. In: . 3. ed. New York: Cambridge University Press, 2007. cap. Section 10.11. Linear



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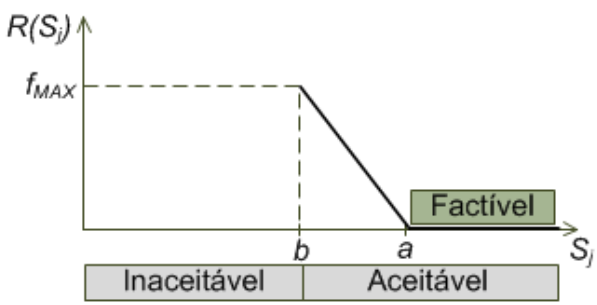
- Avaliação da solução
- Alvo de otimização

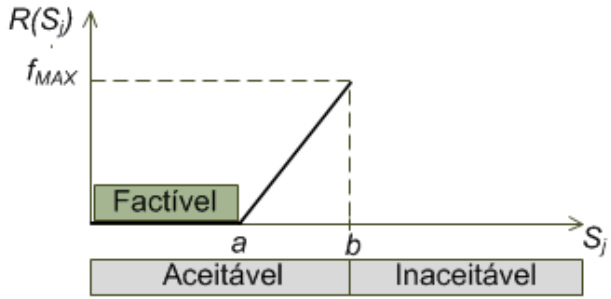
Fc = E_Otimização + E_Restrições

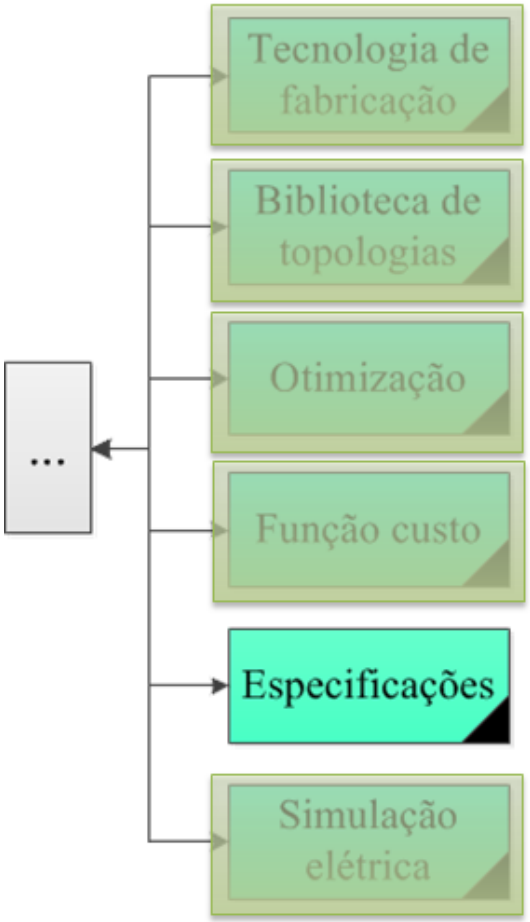
$$f_c(X) = \sum_{i=1}^{n} P_{O_i} . S_i(X) + \sum_{j=1}^{n} P_{R_j} . R(S_j(X), S_{jref})$$

Valor Mínimo



Valor Máximo





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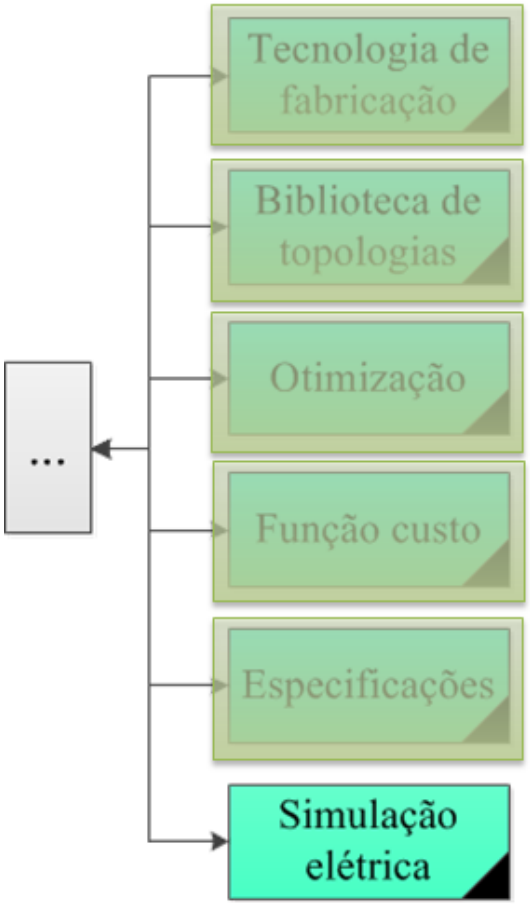
- **As especificações da ferramenta dividem-se em dois tipos:**
  - Restrições:
    - Valor mínimo ou máximo
  - Objetivos do projeto:
    - Minimizar ou maximizar.
- **Valores para as especificações são obtidos com simulação SPICE**



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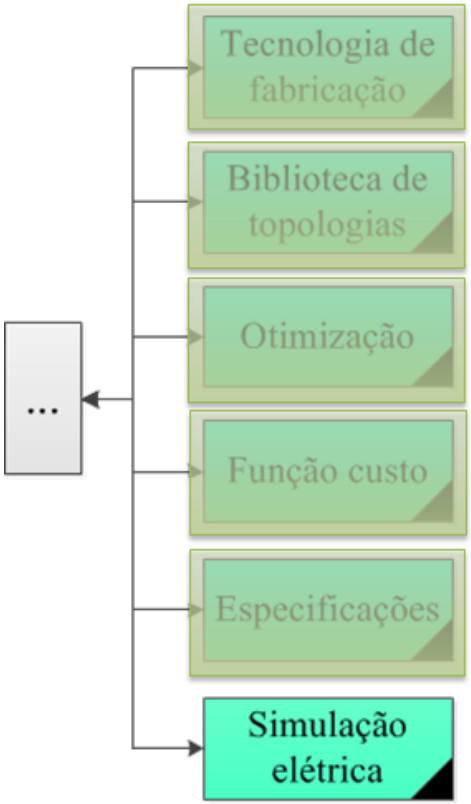
- **Interface com os simuladores elétricos comerciais:**
  - Análise DC
  - Análise AC
  - Análise TRAN
- **Escolha do simulador:**
  - Modelo de tecnologia disponível
  - Técnica de convergência de simulação
- **Neste ferramenta foi utilizado o simulador elétrico Synopsys HSPICE®.**
- ***Testbenches* de simulação.**
  - Avo, GBW, PM (AC em malha aberta)
  - Slew rate (TRAN)
  - ICMR (DC)
  - OS (DC)
  - Potência (OP)
  - Área de gate (diretamente com as variáveis)



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Ex. Análise AC em malha aberta