

Federal University of Pelotas – UFPel Group of Architectures and Integrated Circuits Pelotas – Brasil

A VLSI Architecture for Reference Frame Compression on High Definition Video Coding Systems

Guilherme Povala, Lívia Amaral, Dieison Silveira, Júlio Mattos, Marcelo Porto, Luciano Agostini







Apoio:













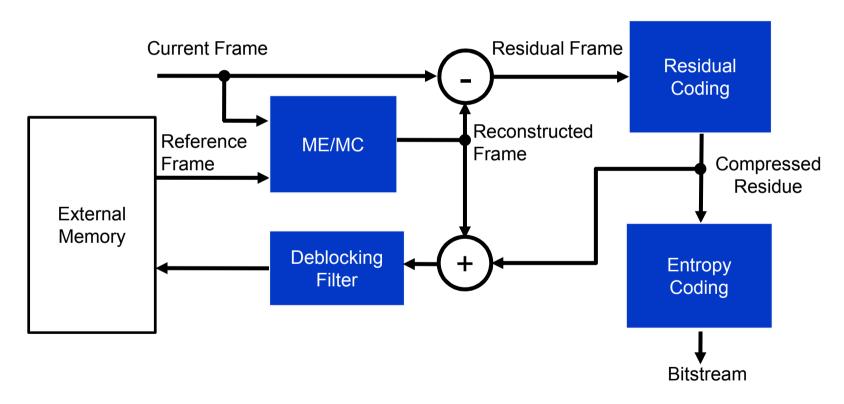








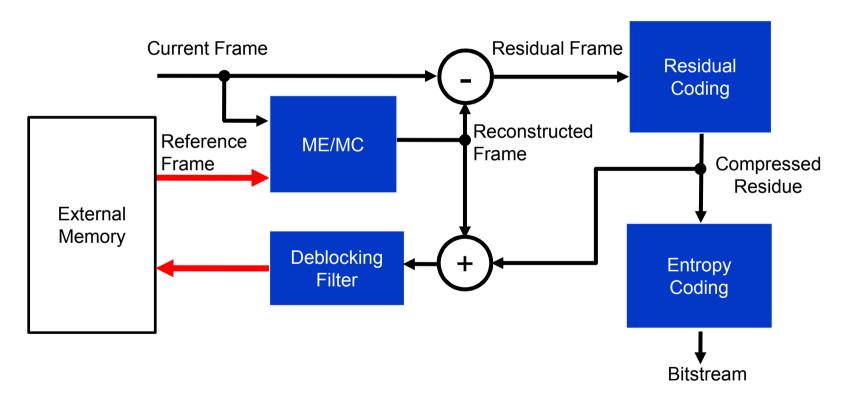
☐ Block diagram of a typical video coding system







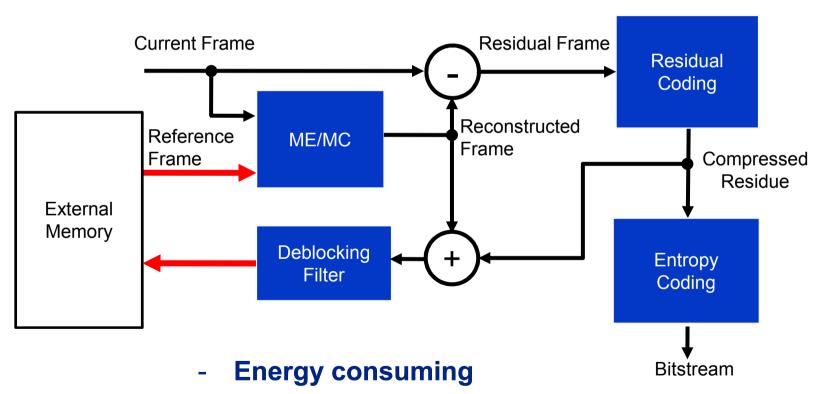
■ Memory issues in a video coding system







■ Memory issues in a video coding system







- Bottleneck of many digital systems

Memory Issues in Video Coding

- Known Solutions for memory issues
 - Data reuse
 - Reduces reading operations
 - Requires a cache
 - Reference frame compression
 - Compresses reference frames before they are stored in the external memory (DRAM)
 - Reduces reading and writing operations
 - It can be lossy or lossless quality





Memory Issues in Video Coding

- **□** Lossless reference frame compression:
 - Reduces reading and writing operations
 - Keeps video quality unaltered
 - Requires a lossless compression algorithm
 - It can be used by the current video encoders, like
 H.264/AVC and HEVC





Goals

- ☐ The main goals of the designed RFCAVLC were:
 - Lossless to avoid quality degradation
 - Achieve good compression rates
 - Decode one sample per cycle
 - Provide a throughput enough to process high resolution videos in real time





RFCAVLC8t

RFCAVLC8t (Reference Frame Context Adaptive Variable-Length Compressor with 8 tables);
 It uses 4x4 blocks during the coding process;
 It reaches a compression rate of more than 31% on average;
 Compresses the frame before it is stored in the external memory;

Decompresses the frame when it is required by ME;

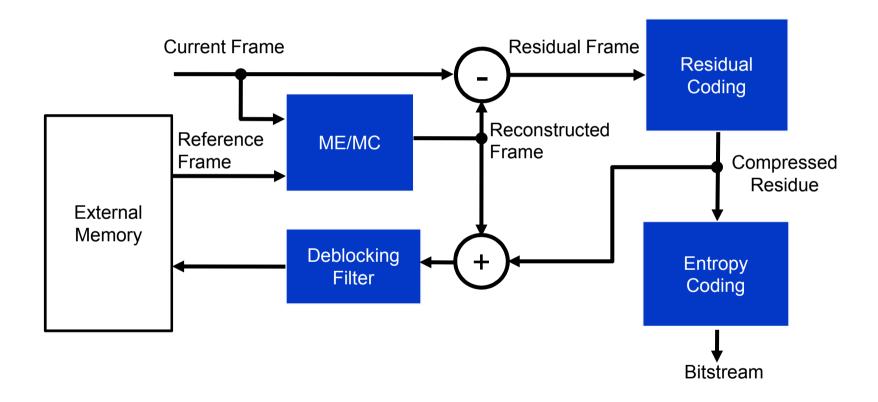
Uses eight static Huffman tables.





RFCAVLC8t

□ Video coding system

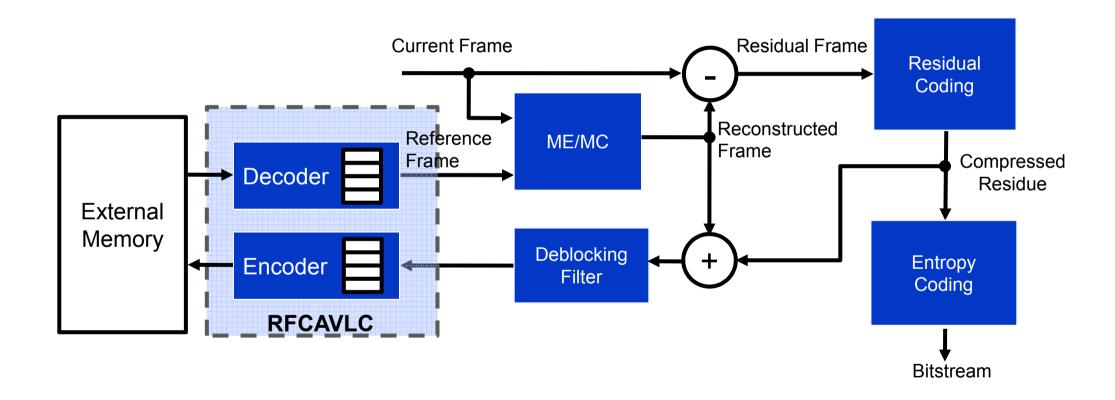






RFCAVLC8t

☐ Video coding system + RFCAVLC8t

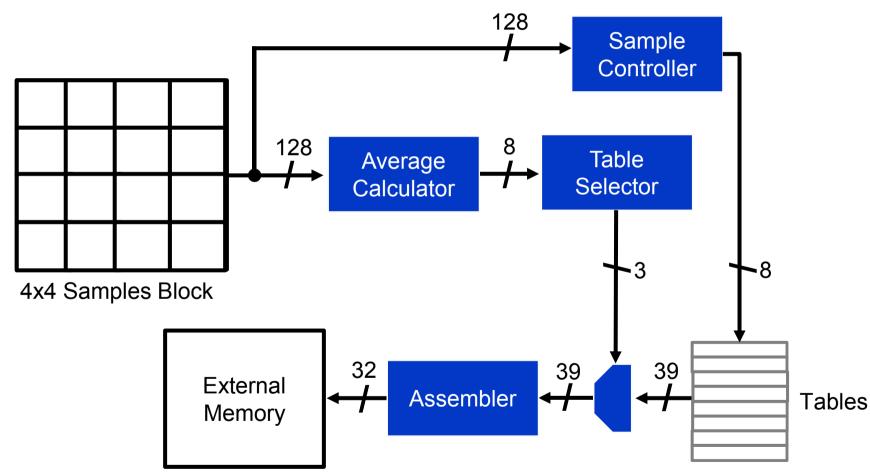






RFCAVLC Architecture

□ Architecture of the RFCAVLC Encoder

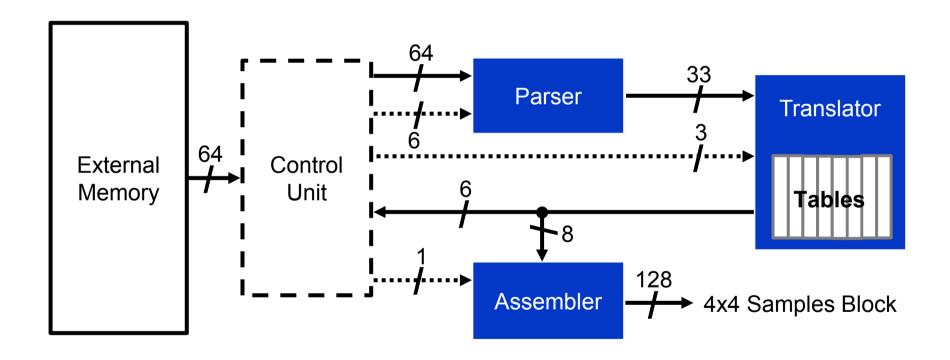






RFCAVLC Architecture

□ Architecture of the RFCAVLC Decoder







Results

□ The architecture was described in VHDL and synthesized to the EP4S40G2F40I2 Altera Stratix 4 FPGA device

Results	Encoder	Decoder	RFCAVLC
ALUTs	1.563	5.056	6.516
Registers	169	852	1.147
Frequency	295,62 MHz	198,89 MHz	198,30 MHz
Throughput	45 fps (WQSXGA)	30 fps (WQSXGA)	30 fps (WQSXGA)

- ☐ It is able to encode one sample per cycle
- ☐ Throughput: 30 frames per second in WQSXGA (3200x2048) resolution.





Conclusions

- □ This work presented the RFCAVLC8t, a solution for memory bandwidth reduction in video coding systems through lossless reference frames compression.
- □ This design presented a very low hardware cost and reached a high throughput, processing more than 198 millions of samples per second
- □ The best architecture performance among the related works
- □ This solution is compliant with state-of-the-art coding standards, such as the H.264/AVC and the emerging HEVC





Future Works

- Implementing a memory solution that uses both RFCAVLC and Data Reuse to improve bandwidth reduction
- Obtaining and analyzing power and energy results







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Thank you!

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