Federal University of Pelotas - UFPel
Center of Technological Development - CDTec
Post-Graduate Program in Computer - PPGC
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A Hardware Solution for the HEVC Fractional Motion Estimation Interpolation

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Support:

Outline

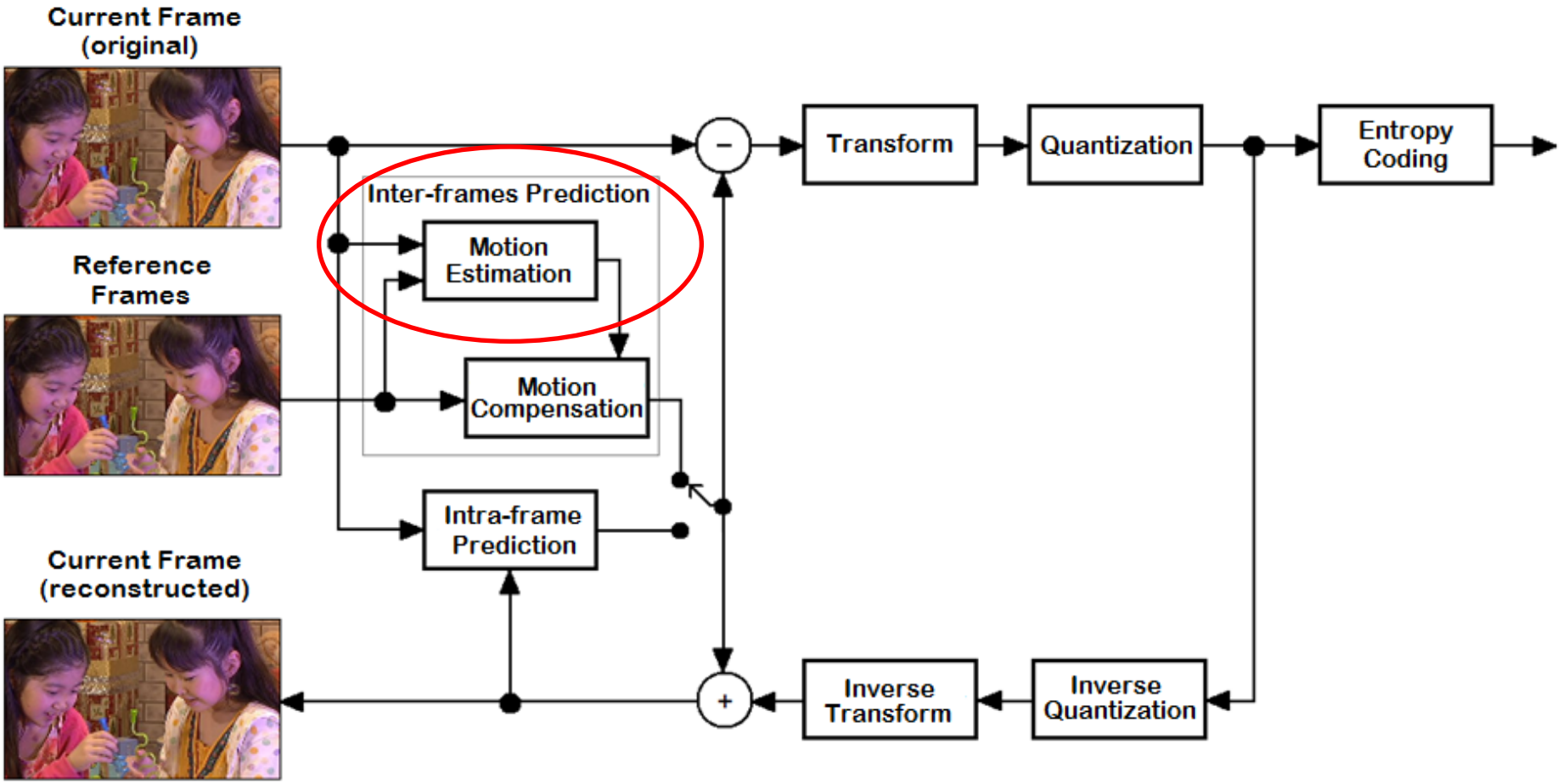
- Introduction
  - Digital Videos
  - Motion Estimation
- Evaluation Using the Reference Software
- Designed Architecture
- Synthesis Results
- Conclusions
- Future Works

Digital Videos

- What is the problem related with high definition digital videos in real time applications?
- Why develop specific integrated circuits for video coding area?
- What is the expected result in coding of sequences?

Video Coding

- How is built a video encoder?



Motion Estimation

- What is the objective of Motion Estimation (ME)?

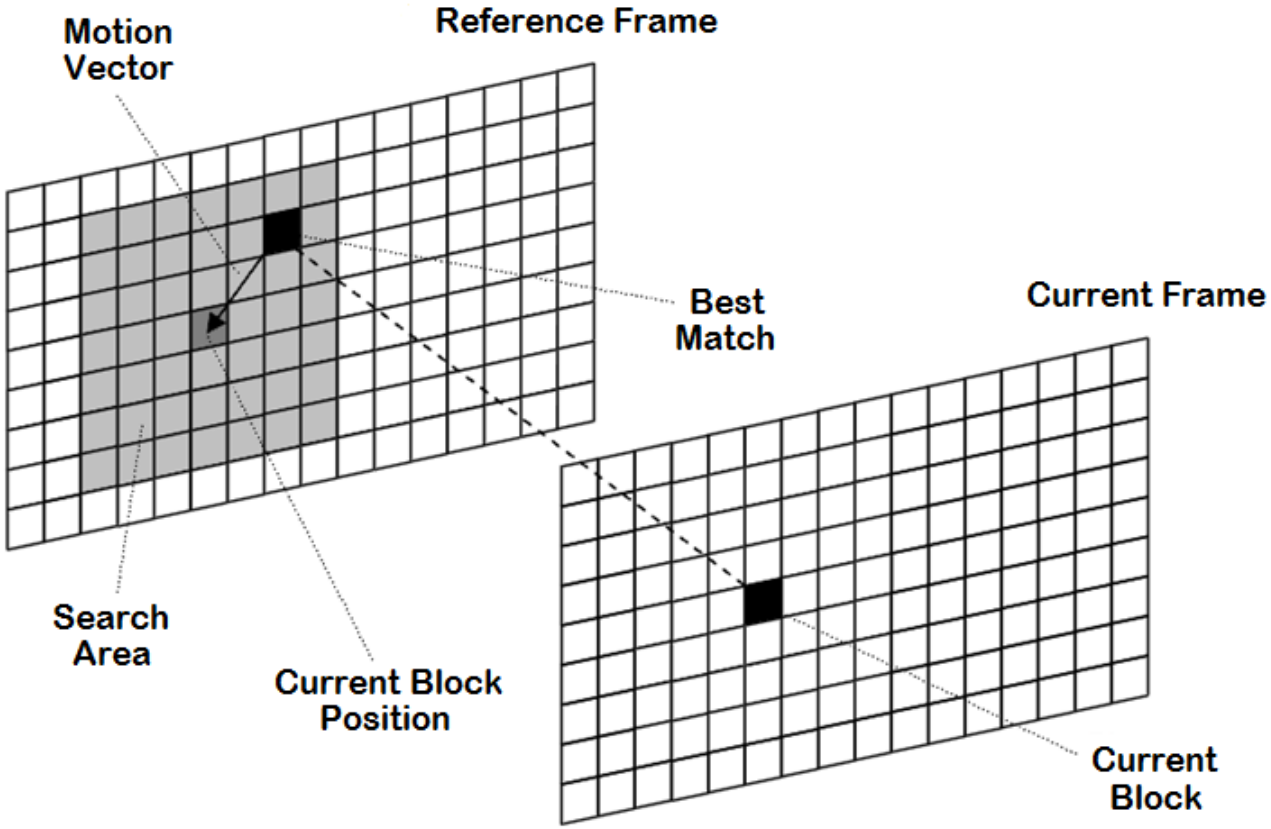
T_n

T_{n+1}

T_{n+2}

Motion Estimation

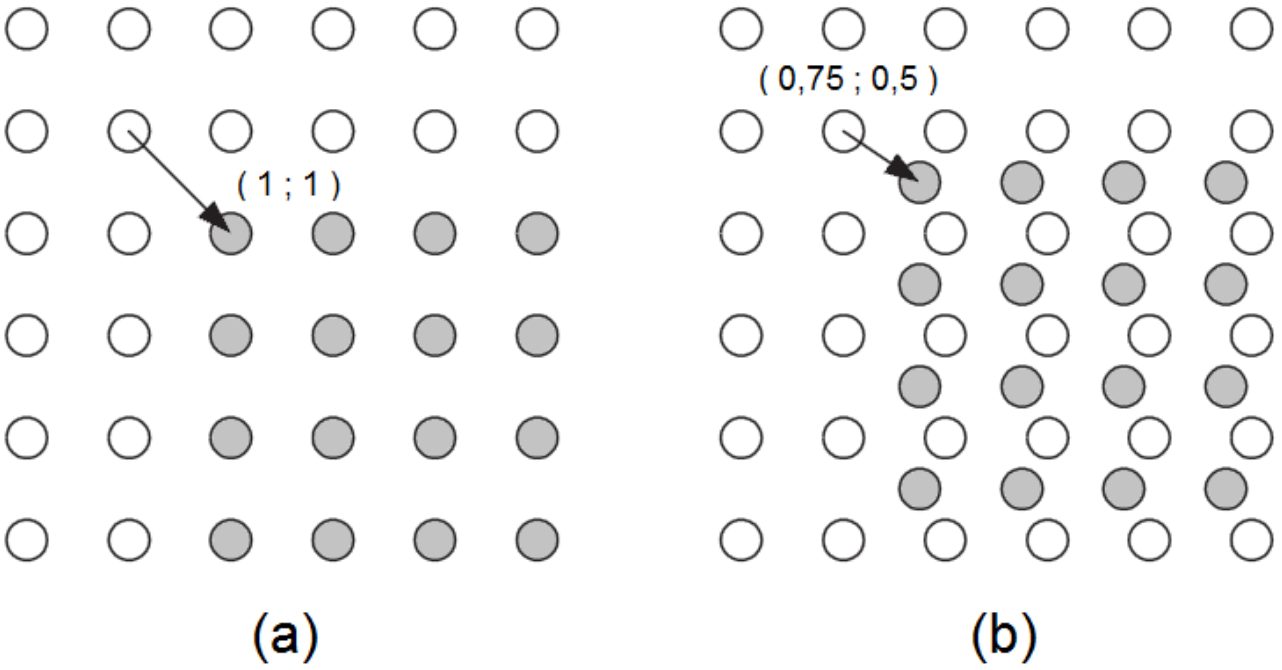
- How is applied the ME?



Motion Estimation

- Is it possible to improve the results in compression rates obtained with the ME?

- How is applied the Fractional Motion Estimation (FME)?



Evaluation Using the Reference Software

- **Evaluation with the reference software of the HEVC video coding standard**
  - It was possible to verify that the FME is a very important tool in the HEVC encoder.
  - FME brings gains in terms of image quality and compression rates.
  - The PU size most selected by the HM (HEVC Model – Reference Software) was 8x8.
  - When only one PU size is evaluated, the global encoder complexity is drastically reduced.
  - The losses in image quality and compression are justified, especially for applications with processing and energy consumption restrictions.

Designed Architecture

- Objective:
  - Design an architecture able to interpolate the luma samples according the HEVC standard targeting high definition digital videos with real time processing.

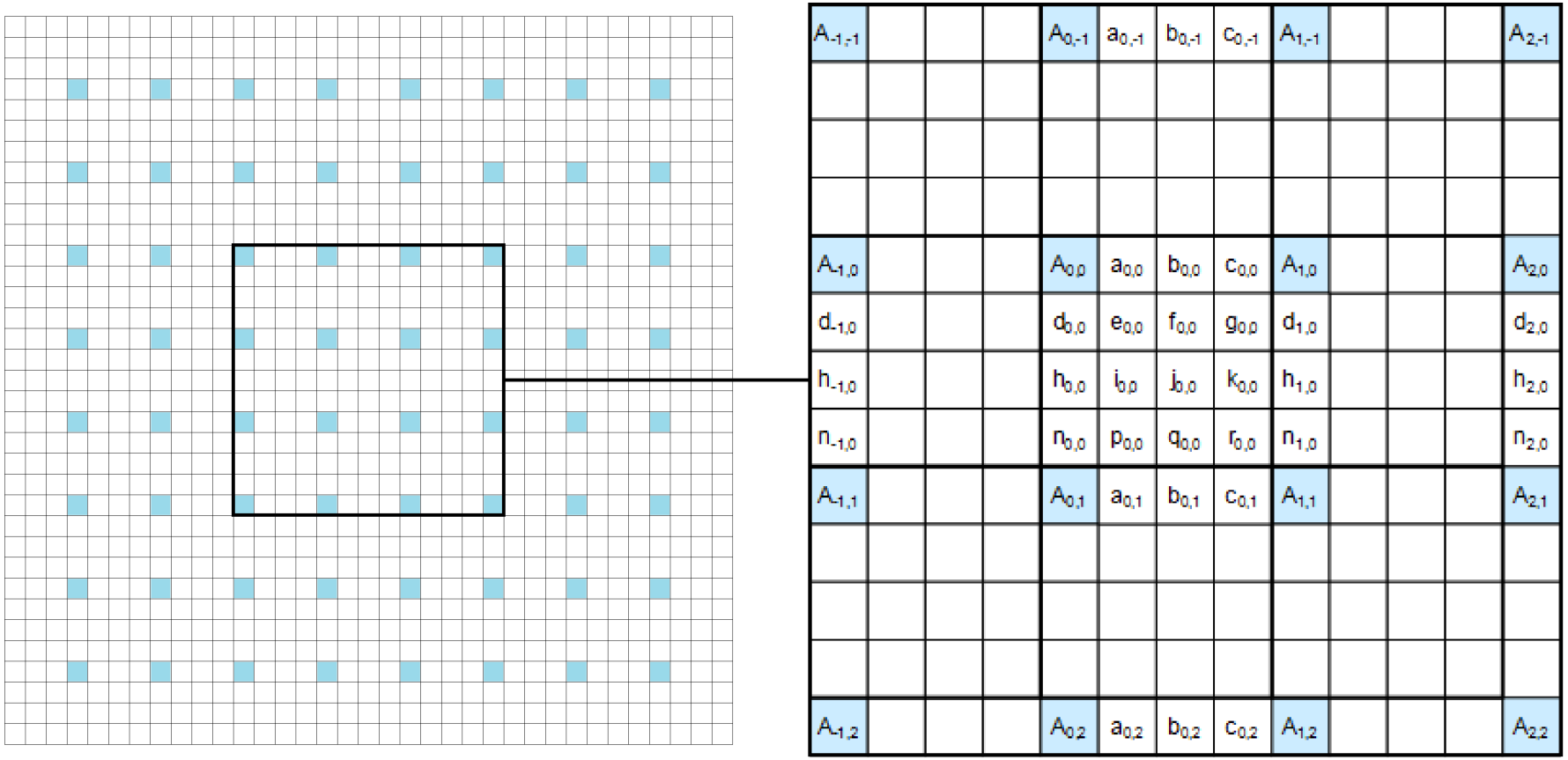
- Principal References Used in the Project:
  - HEVC Test Model 8 Encoder Description
  - HEVC Text Specification Draft 8
  - HEVC Reference Software

- Needed Hardware:
  - An input memory to store values of luma samples in integer positions.
  - Interpolation filters to generate values of luma samples in sub-pixel positions.
  - An output memory to store values of luma samples in sub-pixel positions.

- Specification:
  - Fixed PU block size of 8x8 samples.
  - Luma samples of 8 bits.

Designed Architecture

- Luma samples in integer and fractional positions considering an 8x8 block.



Designed Architecture

- Algorithmic used to determine the sub-pixel values.

$$a_{0,0} = (-A_{-3,0} + 4*A_{-2,0} - 10*A_{-1,0} + 58*A_{0,0} + 17*A_{1,0} - 5*A_{2,0} + A_{3,0}) >> shift1 \quad (1)$$

$$b_{0,0} = (-A_{-3,0} + 4*A_{-2,0} - 11*A_{-1,0} + 40*A_{0,0} + 40*A_{1,0} - 11*A_{2,0} + 4*A_{3,0} - A_{4,0}) >> shift1 \quad (2)$$

$$c_{0,0} = (A_{-2,0} - 5*A_{-1,0} + 17*A_{0,0} + 58*A_{1,0} - 10*A_{2,0} + 4*A_{3,0} - A_{4,0}) >> shift1 \quad (3)$$

$$d_{0,0} = (-A_{0,-3} + 4*A_{0,-2} - 10*A_{0,-1} + 58*A_{0,0} + 17*A_{0,1} - 5*A_{0,2} + A_{0,3}) >> shift1 \quad (4)$$

$$h_{0,0} = (-A_{0,-3} + 4*A_{0,-2} - 11*A_{0,-1} + 40*A_{0,0} + 40*A_{0,1} - 11*A_{0,2} + 4*A_{0,3} - A_{0,4}) >> shift1 \quad (5)$$

$$n_{0,0} = (A_{0,-2} - 5*A_{0,-1} + 17*A_{0,0} + 58*A_{0,1} - 10*A_{0,2} + 4*A_{0,3} - A_{0,4}) >> shift1 \quad (6)$$

$$e_{0,0} = (-a_{0,-3} + 4*a_{0,-2} - 10*a_{0,-1} + 58*a_{0,0} + 17*a_{0,1} - 5*a_{0,2} + a_{0,3}) >> shift2 \quad (7)$$

$$f_{0,0} = (-b_{0,-3} + 4*b_{0,-2} - 10*b_{0,-1} + 58*b_{0,0} + 17*b_{0,1} - 5*b_{0,2} + b_{0,3}) >> shift2 \quad (8)$$

$$g_{0,0} = (-c_{0,-3} + 4*c_{0,-2} - 10*c_{0,-1} + 58*c_{0,0} + 17*c_{0,1} - 5*c_{0,2} + c_{0,3}) >> shift2 \quad (9)$$

$$i_{0,0} = (-a_{0,-3} + 4*a_{0,-2} - 11*a_{0,-1} + 40*a_{0,0} + 40*a_{0,1} - 11*a_{0,2} + 4*a_{0,3} - a_{0,4}) >> shift2 \quad (10)$$

$$j_{0,0} = (-b_{0,-3} + 4*b_{0,-2} - 11*b_{0,-1} + 40*b_{0,0} + 40*b_{0,1} - 11*b_{0,2} + 4*b_{0,3} - b_{0,4}) >> shift2 \quad (11)$$

$$k_{0,0} = (-c_{0,-3} + 4*c_{0,-2} - 11*c_{0,-1} + 40*c_{0,0} + 40*c_{0,1} - 11*c_{0,2} + 4*c_{0,3} - c_{0,4}) >> shift2 \quad (12)$$

$$p_{0,0} = (a_{0,-2} - 5*a_{0,-1} + 17*a_{0,0} + 58*a_{0,1} - 10*a_{0,2} + 4*a_{0,3} - a_{0,4}) >> shift2 \quad (13)$$

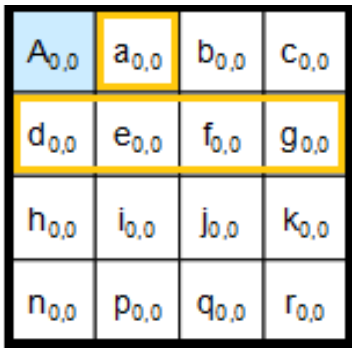
$$q_{0,0} = (b_{0,-2} - 5*b_{0,-1} + 17*b_{0,0} + 58*b_{0,1} - 10*b_{0,2} + 4*b_{0,3} - b_{0,4}) >> shift2 \quad (14)$$

$$r_{0,0} = (c_{0,-2} - 5*c_{0,-1} + 17*c_{0,0} + 58*c_{0,1} - 10*c_{0,2} + 4*c_{0,3} - c_{0,4}) >> shift2 \quad (15)$$

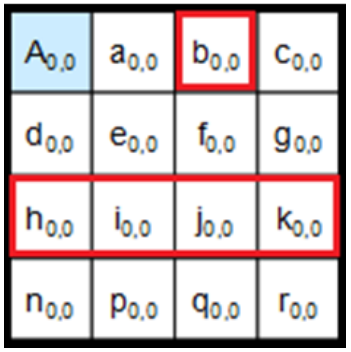
Designed Architecture

- Interpolation filter types developed.

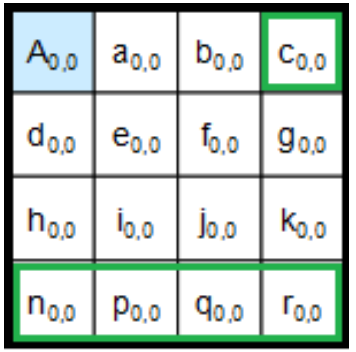
Filter Type	Fractional Positions	Constants Used in the Multiplications
Up	$a_{i,j}$; $d_{i,j}$; $e_{i,j}$; $f_{i,j}$; $g_{i,j}$	{-1, 4, -10, 58, 17, -5, 1, 0}
Middle	$b_{i,j}$; $h_{i,j}$; $i_{i,j}$; $j_{i,j}$; $k_{i,j}$	{-1, 4, -11, 40, 40, -11, 4, -1}
Down	$c_{i,j}$; $n_{i,j}$; $p_{i,j}$; $q_{i,j}$; $r_{i,j}$	{0, 1, -5, 17, 58, -10, 4, -1}



(a)



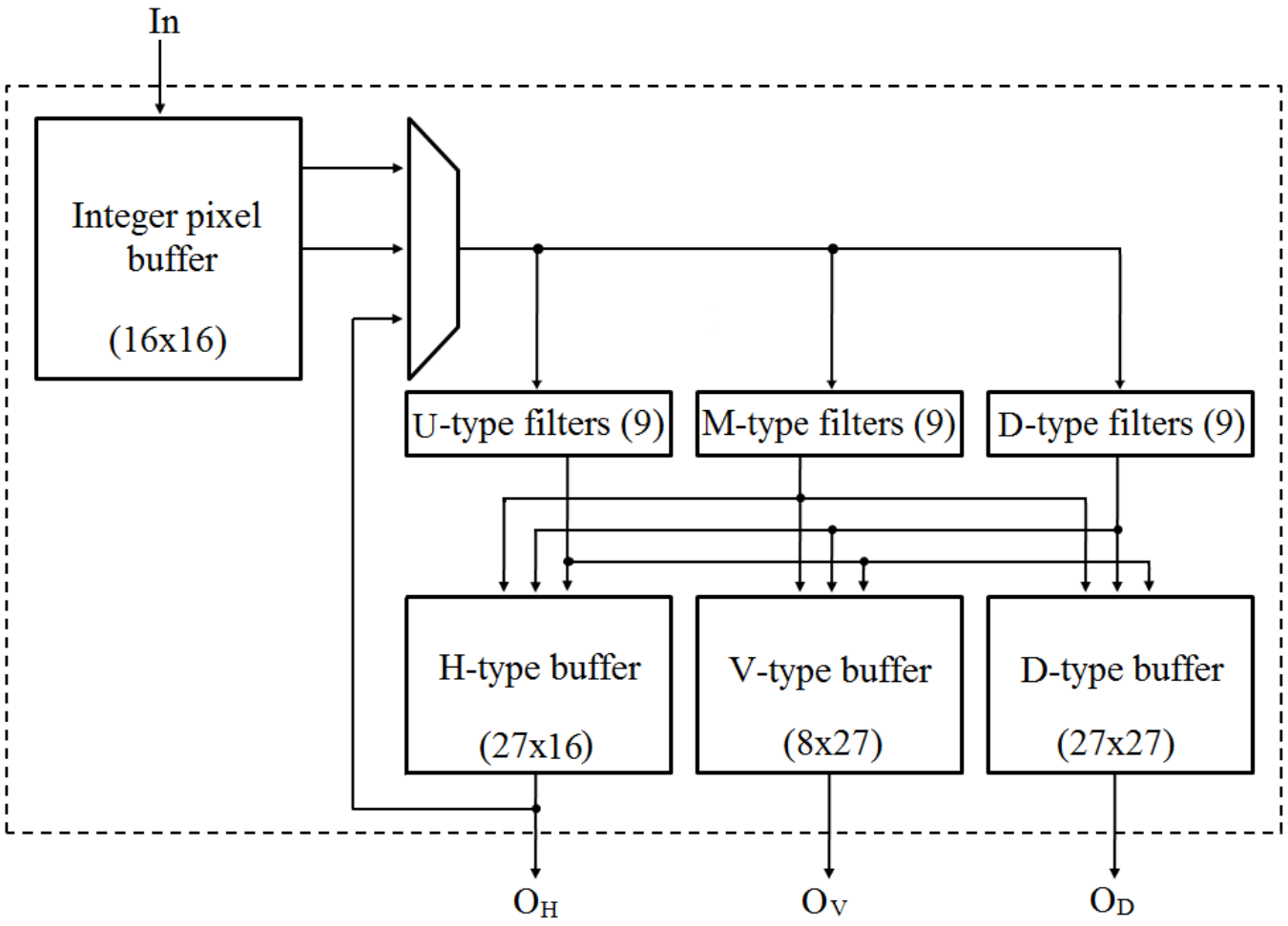
(b)



(c)

Designed Architecture

- Hardware architecture for the FME interpolation unit.



$A_{0,0}$	$a_{0,0}$	$b_{0,0}$	$c_{0,0}$
$d_{0,0}$	$e_{0,0}$	$f_{0,0}$	$g_{0,0}$
$h_{0,0}$	$i_{0,0}$	$j_{0,0}$	$k_{0,0}$
$n_{0,0}$	$p_{0,0}$	$q_{0,0}$	$r_{0,0}$

(a)

$A_{0,0}$	$a_{0,0}$	$b_{0,0}$	$c_{0,0}$
$d_{0,0}$	$e_{0,0}$	$f_{0,0}$	$g_{0,0}$
$h_{0,0}$	$i_{0,0}$	$j_{0,0}$	$k_{0,0}$
$n_{0,0}$	$p_{0,0}$	$q_{0,0}$	$r_{0,0}$

(b)

$A_{0,0}$	$a_{0,0}$	$b_{0,0}$	$c_{0,0}$
$d_{0,0}$	$e_{0,0}$	$f_{0,0}$	$g_{0,0}$
$h_{0,0}$	$i_{0,0}$	$j_{0,0}$	$k_{0,0}$
$n_{0,0}$	$p_{0,0}$	$q_{0,0}$	$r_{0,0}$

(c)

Synthesis Results

- **Synthesis results for the FME interpolation unit.**

Interpolation Filter Version	Combinational ALUTs	Total Registers	Frequency (MHz)
Combinational	10,327	16,534	131.91
Pipeline and 2 steps	10,327	17,764	208.42
Pipeline and 4 steps	10,327	19,130	317.36
Altera Stratix III EP3SE50F484C2 FPGA device			

- **Estimation of frames per second using the architectures developed.**

Interpolation Filter Version	Full HD (1920x1080) fps	QFHD (3840x2160) fps
Combinational	79	19
Pipeline and 2 steps	126	31
Pipeline and 4 steps	192	48

Conclusions

- **This work presented a hardware design for the FME interpolation process defined in the HEVC emerging video coding standard.**

- **Based on evaluations using the reference software, the hardware design considered PU blocks with a fixed size of 8x8 samples to reduce the global encoder complexity.**

- **The synthesis results show that the designed hardware is able to interpolate QFHD (3840 x 2460) frames in real time.**

Future Works

- The interpolation architecture presented in this work is been integrated with a search and comparison architecture to obtain a complete FME architecture according the HEVC standard.

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Support:

References

[1] A. Puri, X. Chen and A. Luthra, “Video Coding Using the H.264/MPEG-4 AVC Compression Standard,” *Elsevier Signal Processing: Image Communication*, n. 19, pp. 793–849, 2004.

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