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FPGA Prototyping and Validation of an EPC Gen 2 RFID Tag

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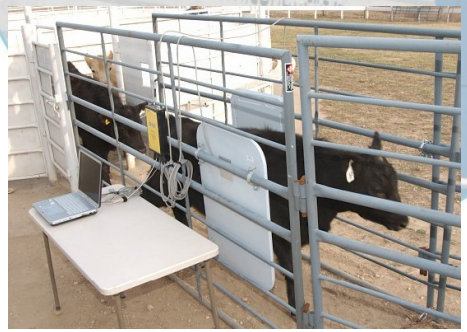
Outline

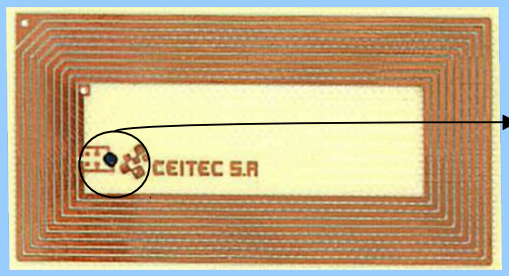
- Introduction
  - RFID ICs
  - RFID Applications
  - RFID Architecture
  - EPC Gen 2 Protocol
- Prototyping
  - Objectives
  - Techniques & Tools Used
- Results
  - Xilinx Synthesis Results
- Conclusions

RFID Applications



RFID Applications

What is Behind these systems:



RFID IC

- Analog Section
- Digital Section

RFID Tag

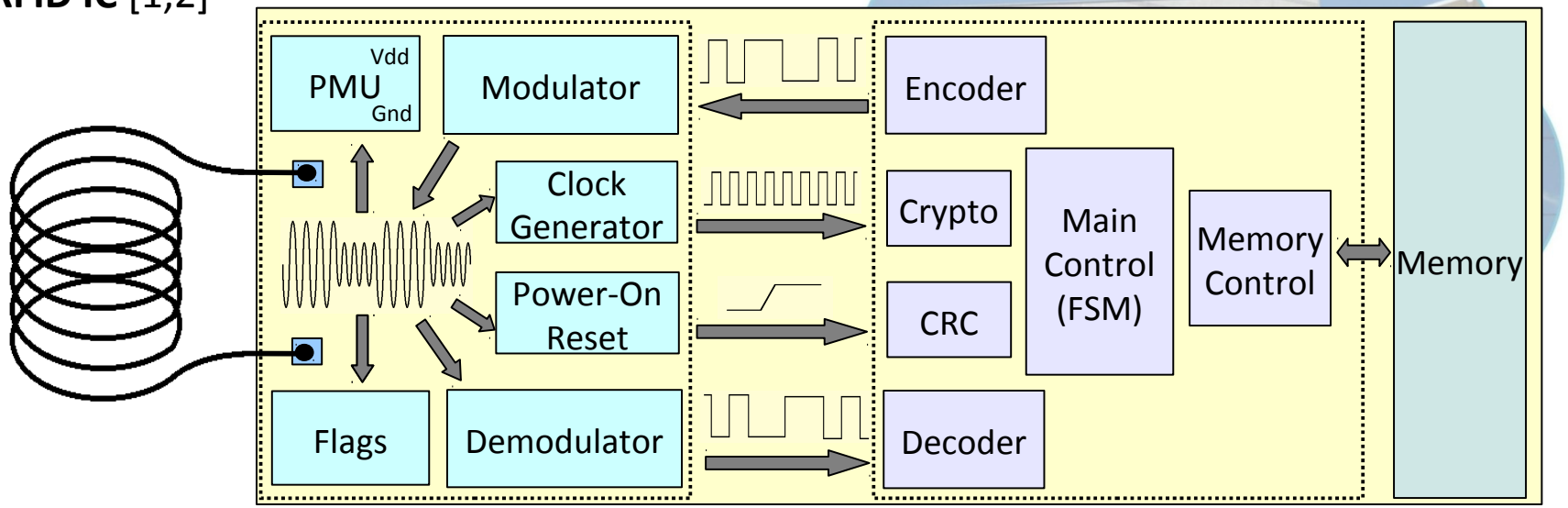
ITF (Interrogator Talks First)

RFID Architecture

- Supply energy for the tag
- Reception and Demodulation of commands
- Generate clock for digital section

- Decoding of command
- Response to the interrogator
- Memory Control

RFID IC [1,2]



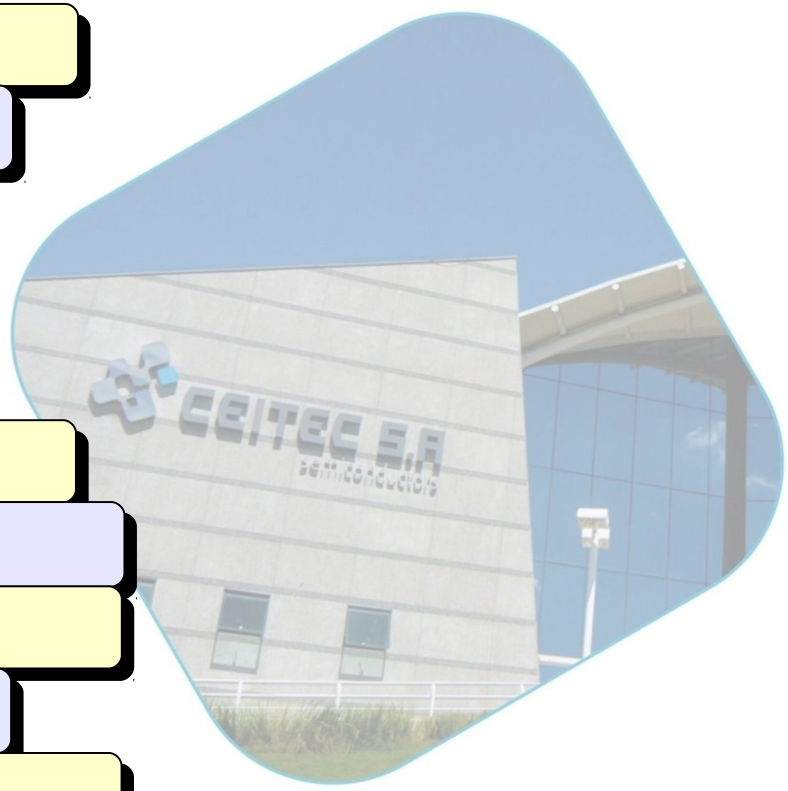
Analog Domain
Digital Domain
Memory

[1] Finkenzeller, K. **"RFID Handbook: Fundamentals and Applications in Contactless Smart Cards and Identification."** 2nd ed. ; Wiley (2003)

[2] Lehpamer, H. **"RFID Design Principles."** ; Boston: Artech House (2003)

EPC Gen 2

- UHF 915 MHz RFID Protocol
  - Most Used Pattern in Industry
  - Long Read Range



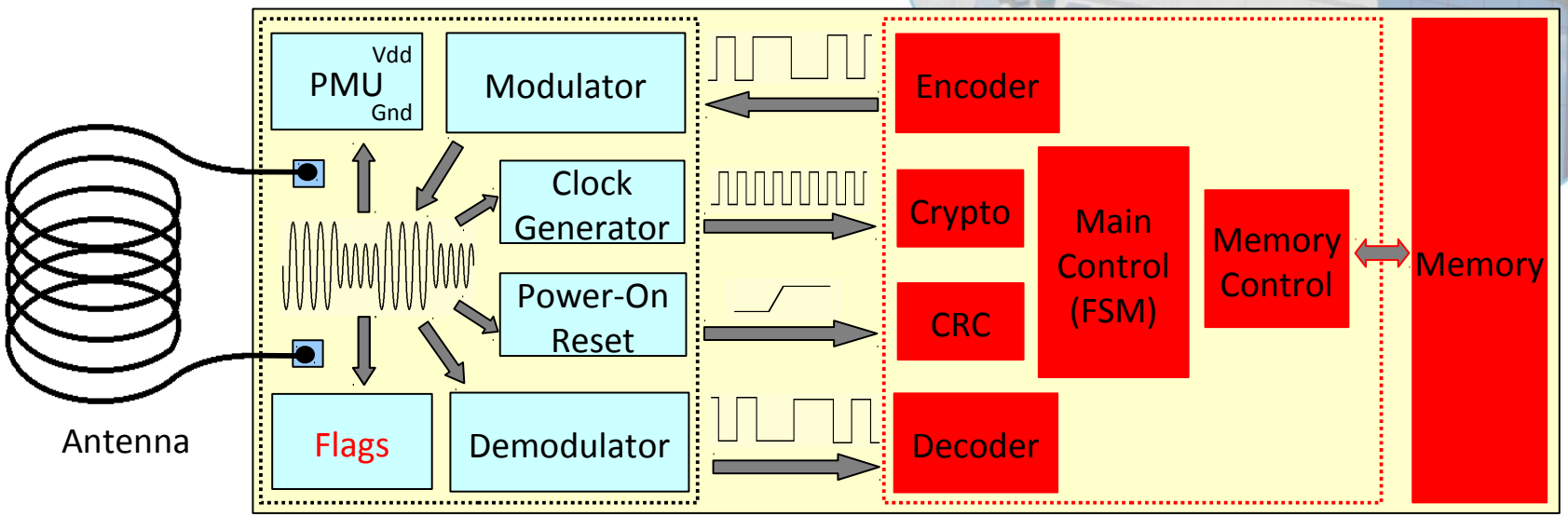
- Finite State Machine
  - Input:
    - Current State
    - Command Received
  - Output:
    - Tag's Response

FPGA Prototyping

- Objectives
- Techniques and Tools used
- Results

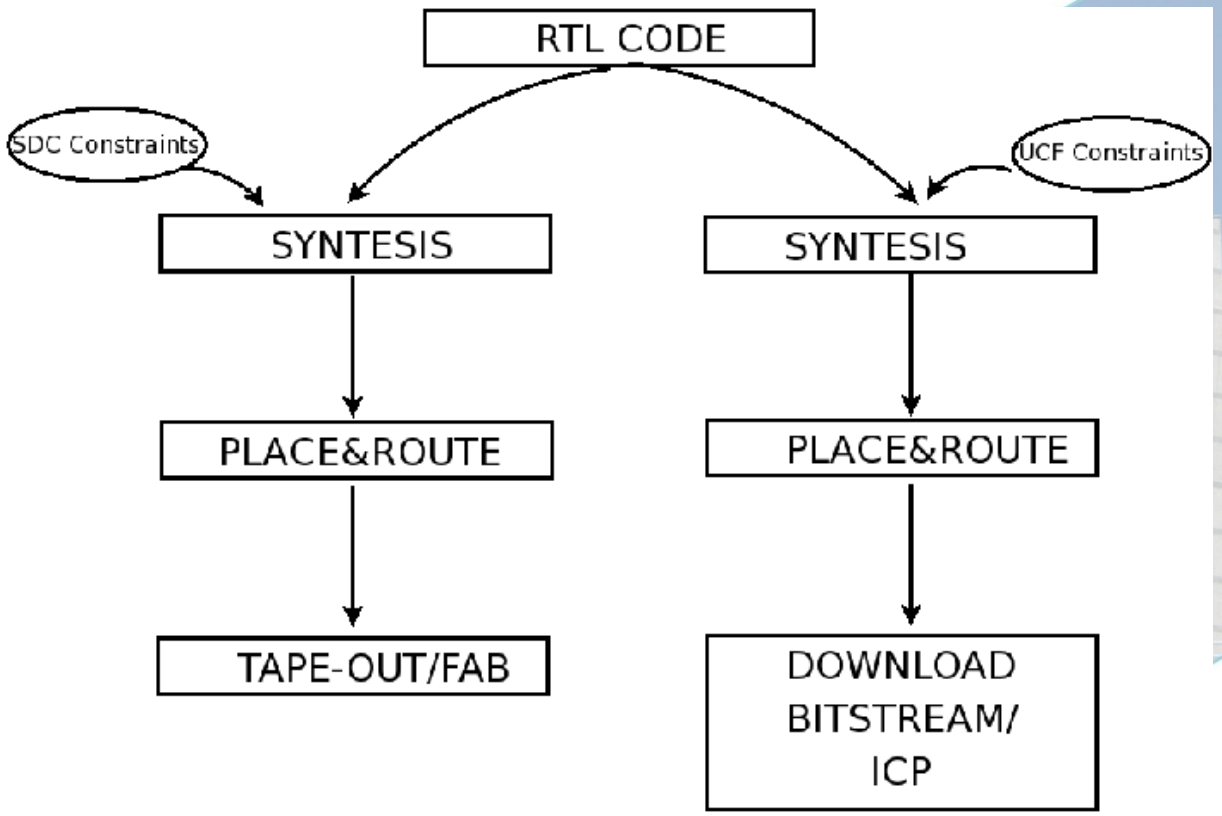
FPGA Prototyping

- Objectives
  - Validate the digital section of a RFID tag
  - Find and fix RTL errors not detected by functional verification
  - Save time and money
  - Avoid rework



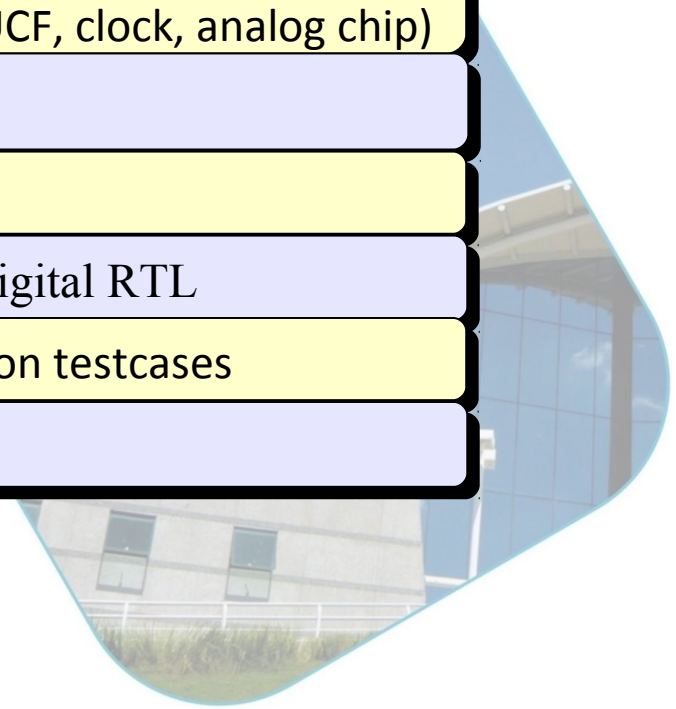
FPGA Prototyping

ASIC x FPGA FLOW



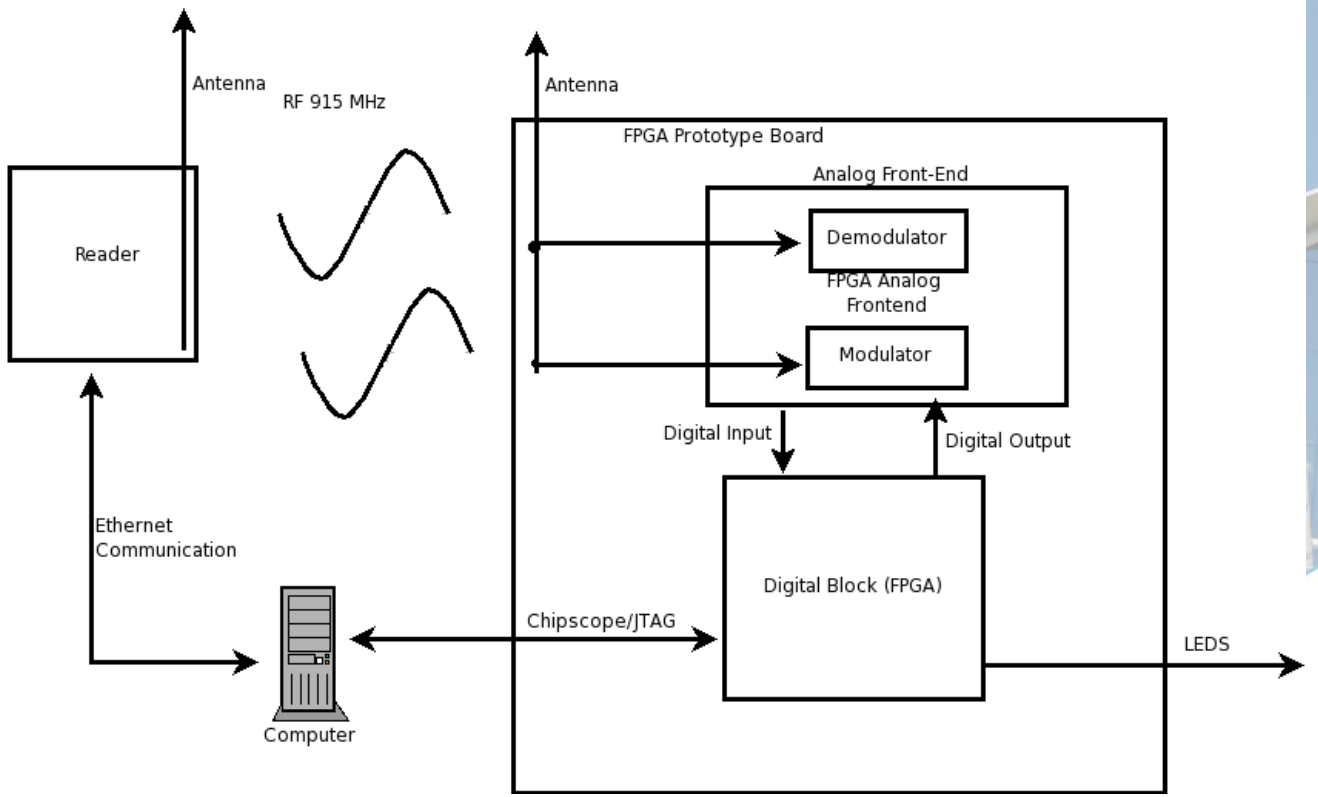
FPGA Prototyping

- Techniques Used
  - Create a FPGA Top Module to adapt its constraints and IC's specifications (Buttons, leds, UCF, clock, analog chip)
  - Change of Memory IP Module
  - Synthesize Digital Blocks into FPGA
  - Creation of scripts to update FPGA's Digital RTL
  - Compare the results with the verification testcases
  - Creation of scripts to the reader tests



FPGA Prototyping

Hardware and Tools Used



Conclusions

The Digital Section of RFID was successfully validated

Saved significant time in the Bringup phase

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Thank You

Questions?

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Xilinx Synthesis Results

Logic Utilization	Used	Available	Utilization
Total number Slice Registers	1686	15360	10%
Number used as Flip-Flop	1683		
Number used as Latches	3		
Number of 4 input LUTs	4965	15360	32%
Number of occupied Slices	3074	7680	40%
Number of Slices containing only related logic	3074	3074	100%
Number of Slices containing only unrelated logic	0	3074	0%
Total Number of 4 input LUTs	5278	15360	34%
Number used as logic	4965		
Number used as a route-thru	313		
Number of Bonded IOBs	13	173	7%
Number of RAMB16s	3	24	12%
Number of BUFGMUXs	3	8	37%
Avarege Fanout of Non-Clock Nets	4.16		

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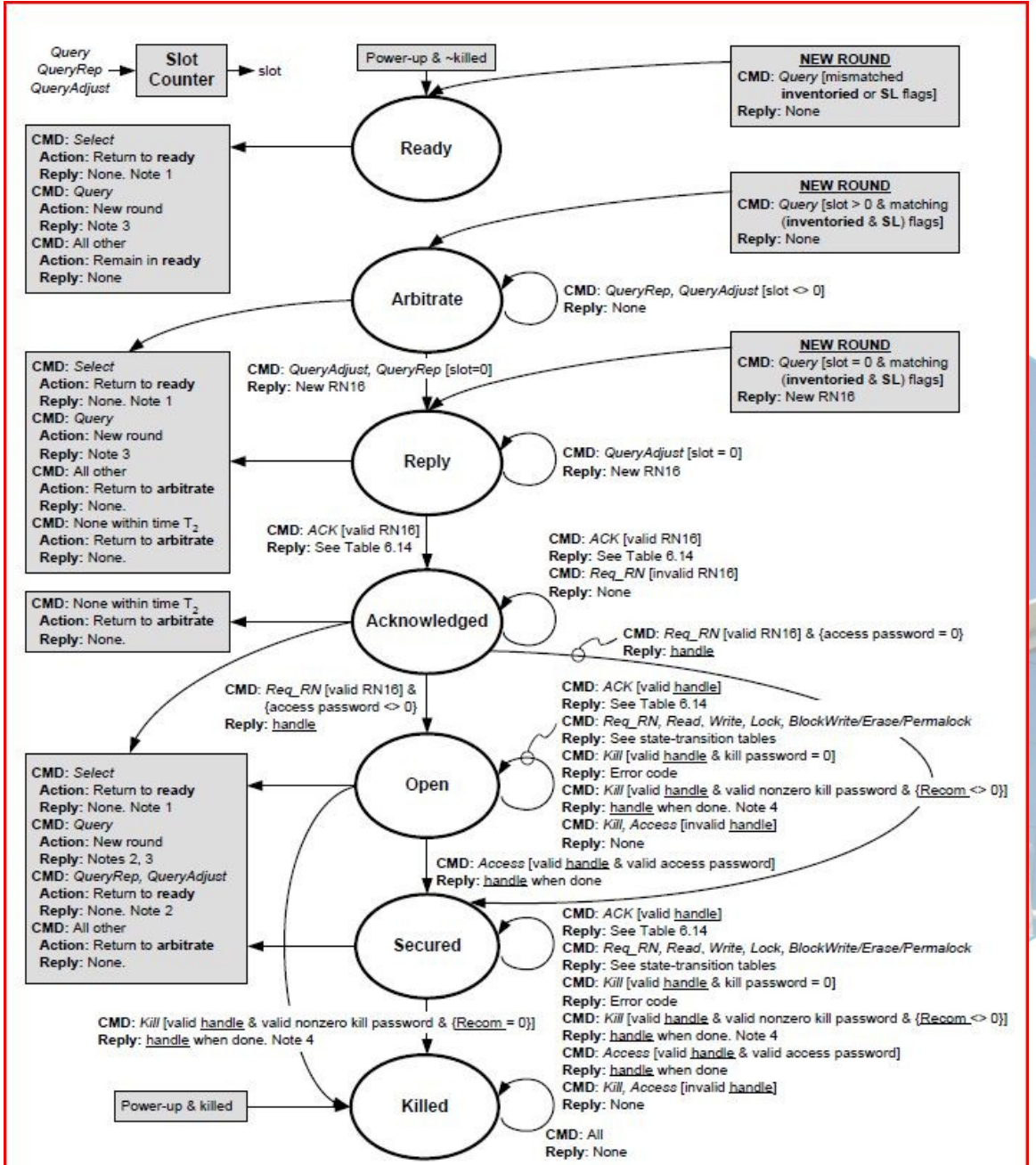
Current State



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EPC Gen 2

Commands

Command	Code	Length (bits)	Mandatory?	Protection
QueryRep	00	4	Yes	Unique command length
ACK	01	18	Yes	Unique command length
Query	1000	22	Yes	Unique command length and a CRC-5
QueryAdjust	1001	9	Yes	Unique command length
Select	1010	> 44	Yes	CRC-16
Reserved for future use	1011	–	–	–
NAK	11000000	8	Yes	Unique command length
Req_RN	11000001	40	Yes	CRC-16
Read	11000010	> 57	Yes	CRC-16
Write	11000011	> 58	Yes	CRC-16
Kill	11000100	59	Yes	CRC-16
Lock	11000101	60	Yes	CRC-16
Access	11000110	56	No	CRC-16
BlockWrite	11000111	> 57	No	CRC-16
BlockErase	11001000	> 57	No	CRC-16
BlockPermalock	11001001	> 66	No	CRC-16
Reserved for future use	11001010 … 11011111	–	–	–
Reserved for custom commands	11100000 00000000 … 11100000 11111111	–	–	Manufacturer specified
Reserved for proprietary commands	11100001 00000000 … 11100001 11111111	–	–	Manufacturer specified
Reserved for future use	11100010 00000000 … 11101111 11111111	–	–	–

EPC Gen 2

FM0 Encoding