Automatic Generation of Processors Dedicated to Simulation of Quantum Algorithms on FPGA

Calebe Conceição *

Ricardo Reis

SIM-2013

INF INSTITUTO DE INFORMÁTICA UFRGS PPGC

UFRGS PGMICRO

Outline

Introduction and Motivation

Details of the tool

The Network of Butterflies model

The Generated Processor

Results

Conclusions

Introduction and Motivation

Scenario

- Finding better computing models and technologies
- Silicon technologies approaching physical limits

Quantum Computing:

- Improves complexity of some widely used problems
- ~~Promising emerging technology~~ → Reality

Simulation of Quantum Algorithms

- Classical Computers → Slow! (Original Feynman's motivation)

NIELSEN, M. A.; CHUANG, I. L. Computação Quântica e Informação Quântica. [S.l.]: Bookman, 2003.

D-WAVE. D-wave systems inc. official page. [Online].(2013, Jan.) Available on: http://www.dwavesys.com

Introduction and Motivation

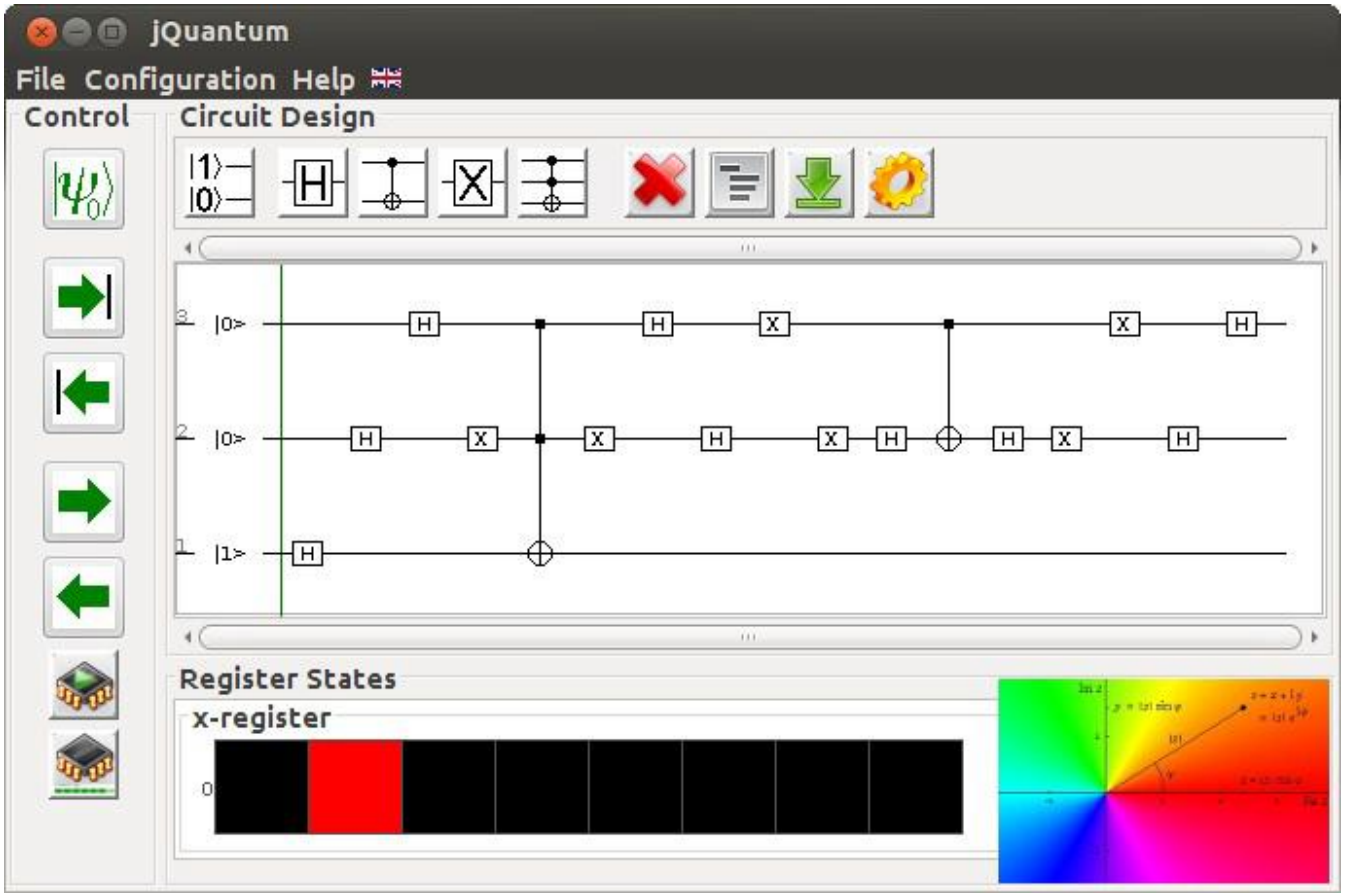
Simulation on FPGA

- Parallelize basic operations
- Simulation time about 10^3 faster than sequential computer

Problems:

- Scalability
  - Complexity: TIME → SPACE
- ✓ Harder work
- ✓ Re-synthesis time

Details of the tool

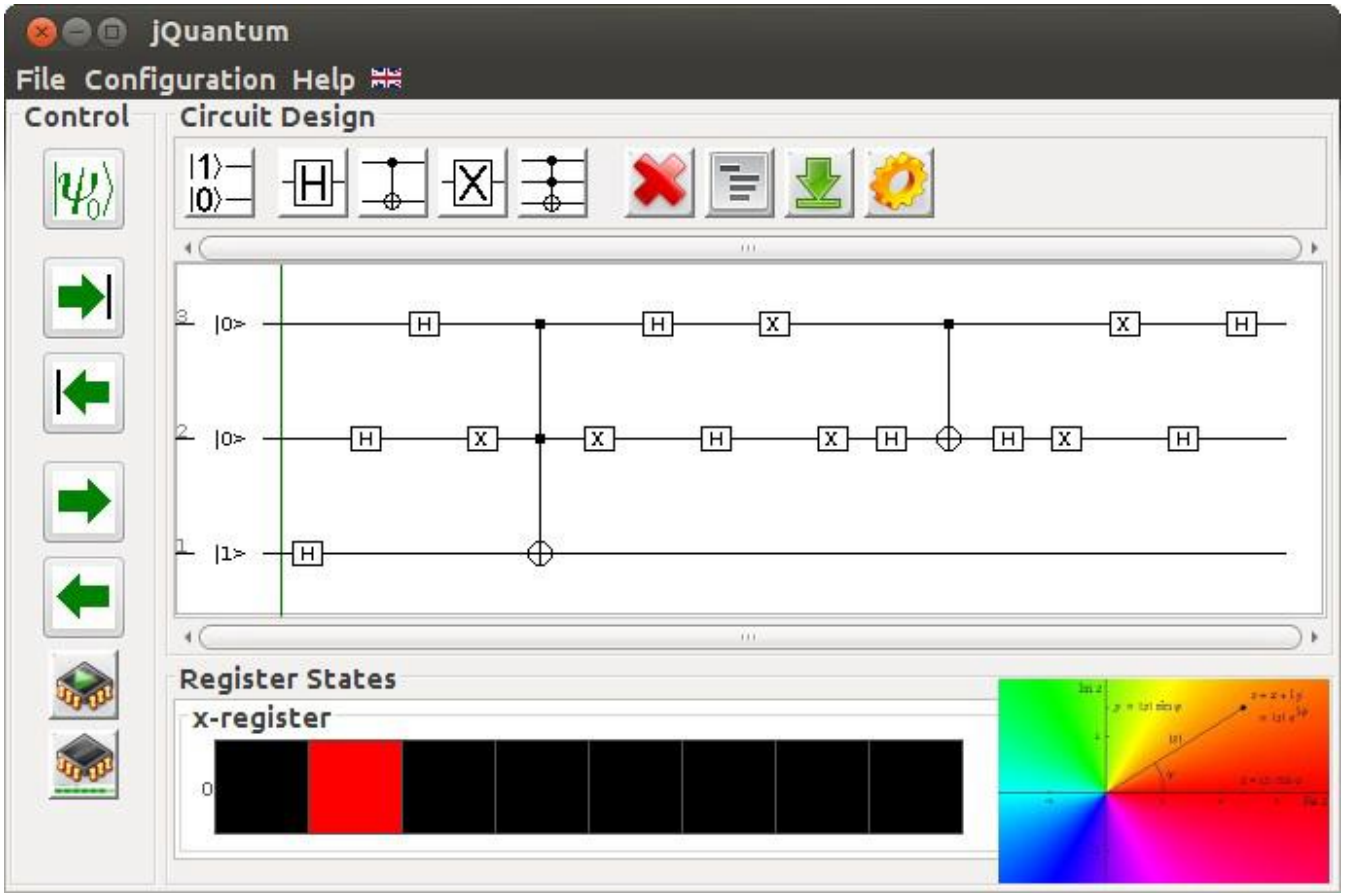


JQuantum interface

Color map for complex values

Circuit Model of description

Details of the tool



SystemVerilog code

Synthsizable RTL

Library independent

Network of Butterflies Model

Pauli X behavior : 1 qubit system

$$|\psi_0\rangle = \alpha|0\rangle + \beta|1\rangle$$

$$X|\psi_0\rangle$$

$$|\psi_1\rangle = \beta|0\rangle + \alpha|1\rangle$$

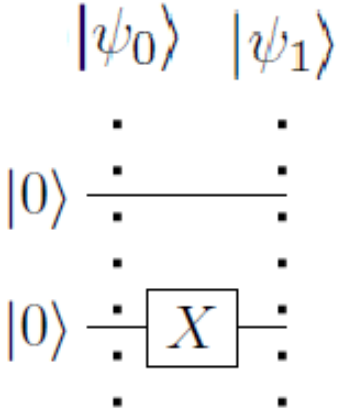
$$X|0\rangle = |1\rangle$$

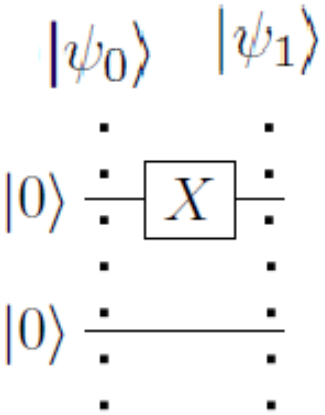
$$X|1\rangle = |0\rangle$$

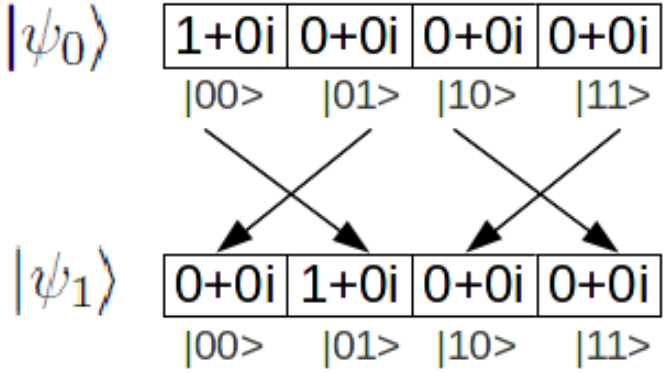
G. NEGOVETIC, M. PERKOWSKI, M. LUKAC, A. BULLER, "*Evolving Quantum Circuits and an FPGA-Based Quantum Computing Emulator*", International Workshop on Boolean Problems, 2002.

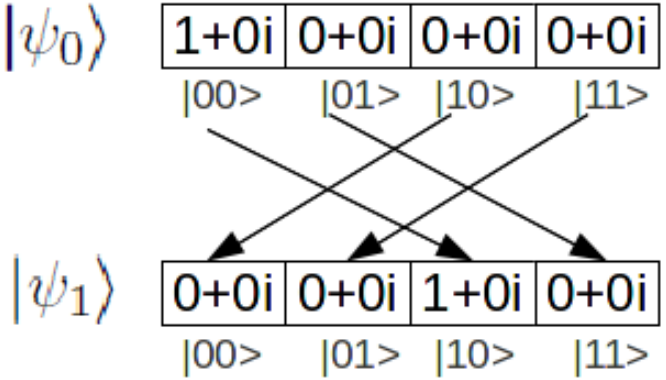
Network of Butterflies Model

Pauli X behavior : 2 qubits system





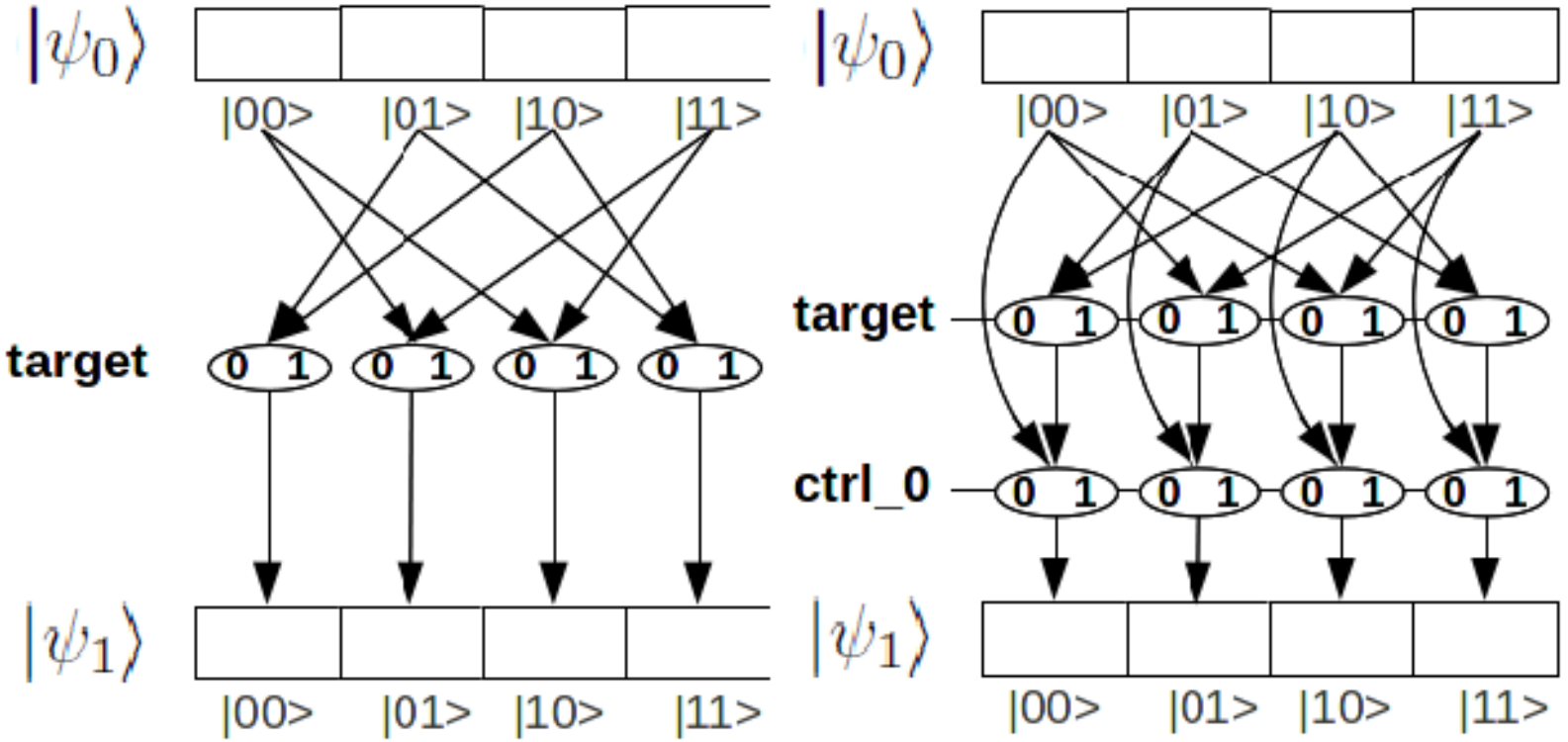




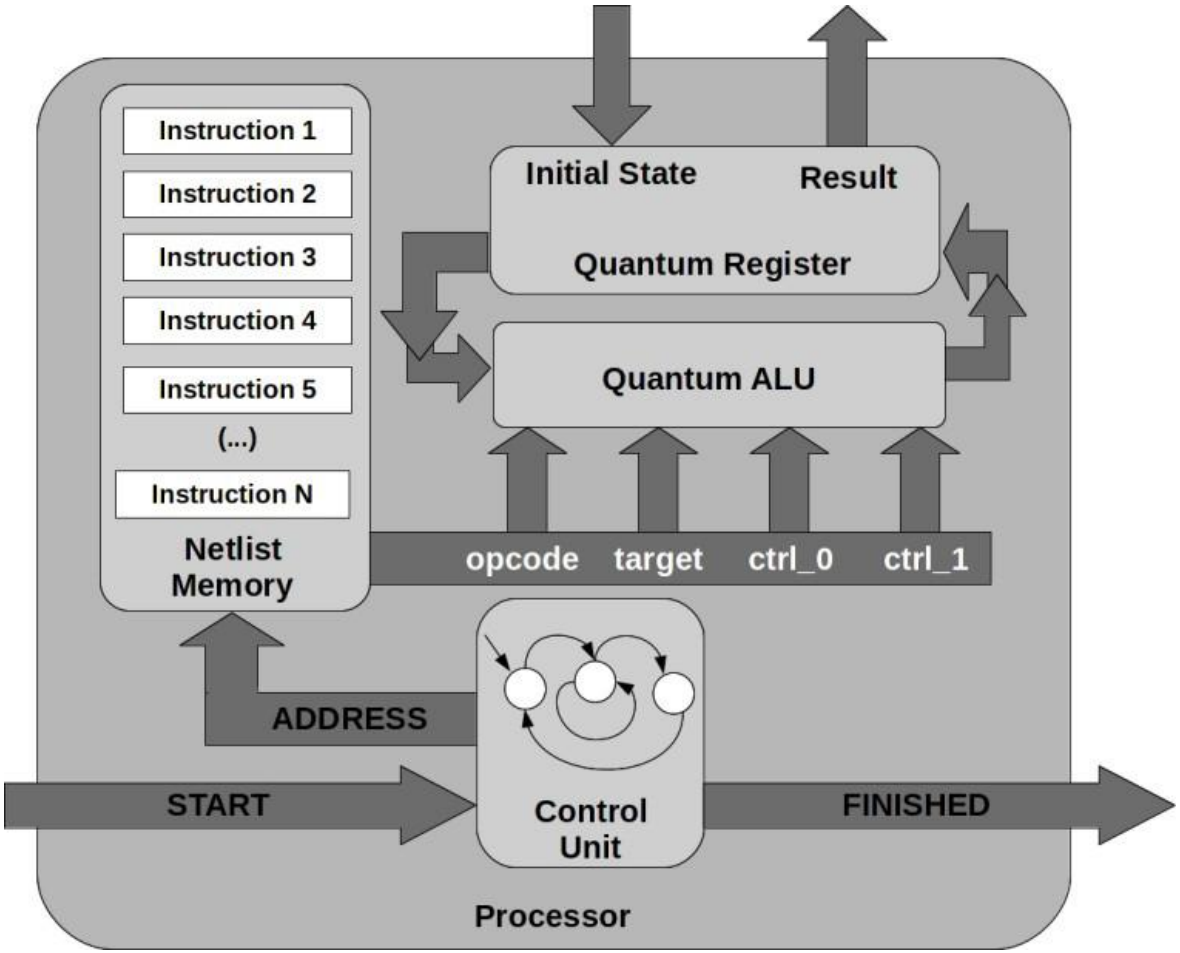
G. NEGOVETIC, M. PERKOWSKI, M. LUKAC, A. BULLER, "*Evolving Quantum Circuits and an FPGA-Based Quantum Computing Emulator*", International Workshop on Boolean Problems, 2002.

Network of Butterflies Model

The way we do:



Co-processor blocks



Format of Instruction:

Data	$ctrl_1$	$target$	$ctrl_0$	$opcode$
Size (bits)	$\lceil log_2 N \rceil$	$\lceil log_2 N \rceil$	$\lceil log_2 N \rceil$	2

Results

TABLE I. LC USAGE OF MODULES WITH THE NUMBER OF QUBITS AND SIZE OF MANTISSA

Unity	1 qubit	2 qubits	3 qubits			4 qubits	5 qubits
			8 bits	*16 bits*	*32 bits*		
Q. ALU	229	531	1402	3526	9408	2982	6869
Q. Reg	32	64	128	256	512	256	512

Mantissa fixed on 8 bits where it is not mentioned. Q. Reg values are expressed in number of flip-flops

TABLE II - Comparison of execution time of some circuits

Circuit	No. Gates	JQuantum	FPGA (link)	FPGA
3_17tc	6	4.7 ms	5.6 ms	0.12 us
Ham3tc	5	3.1 ms	5.5 ms	0.1 us
Hwb4-11-23	11	3.4 ms	7.1 ms	0.22 us
Rd32	4	3.1 ms	7.9 ms	0.08 us

Results

TABLE II. LOGIC CELLS USAGE FOR BENCHMARK CIRCUITS

Circuit	Ours		[Aminian et al]		[Khalid et al]	
	8 bits	*16 bits*	*8 bits*	*16 bits*	*8 bits*	*16 bits*
3_17tc	150	150	24	24	960	1728
ham3tc	140	140	24	24	800	1440
rd32	191	191	48	48	1280	2304
hwb4-11-23	230	230	64	64	3520	6336
xor5d1	416	409	128	128	2560	4608
Mod5d1	571	573	224	224	5120	9216
greycode6	903	905	320	320	6400	11520
rd53d2	4019	4019	3072	3072	-	-

The results of [Khalid] are shown on paper [Aminian].

Conclusions

Scalability is still a problem in FPGA approach

Our solution is invariable to the number of gates in the algorithm.

No need of re-synthesis (Programmable)

Easy of use

Communication can be a bottleneck

Automatic Generation of Processors Dedicated to Simulation of Quantum Algorithms on FPGA

Calebe Conceição *
Ricardo Reis

?

SIM-2013 questions

INF INSTITUTO DE INFORMÁTICA UFRGS PPGC
UFRGS PGMICRO