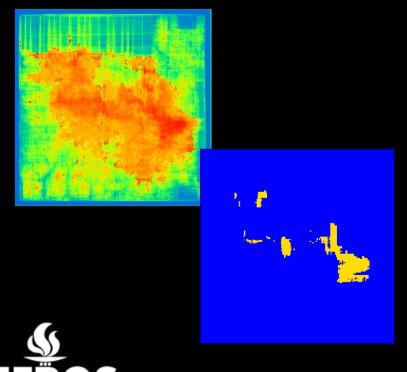
# Global Routing Congestion Reduction with Cost Calibration Look-ahead



**PGMICRO** 

Leandro Nunes, Ricardo Reis leandron85@gmail.com, reis@inf.ufrgs.br SIM 2013 Porto Alegre/RS

#### **Problem Statement**

- Grid based global routing is an exercise of cost calibration
  - There is a set of networks to be routed through the routing area
  - Interconnection will race by the routing region
  - Each tile has an associated capacity
  - Each tile has an associated COSt

#### Global Routing Goals

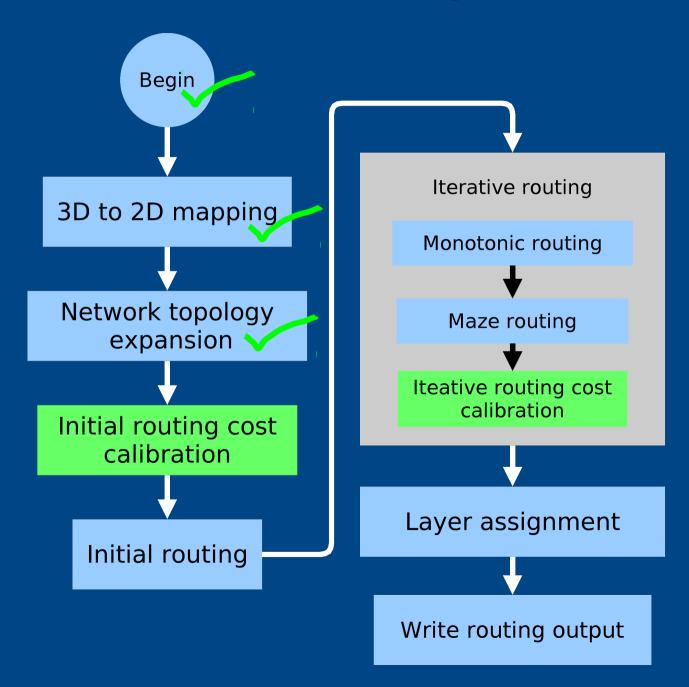
- Try to find lower costs paths as possible
- Route all nets and do not exceed the capacity of any tile
  - Some nets will need to deviate

#### Objectives of this work

- Apply cost pre-allocation techniques to
  - speed up the global routing process
  - reduce overflow and
  - avoid side effects

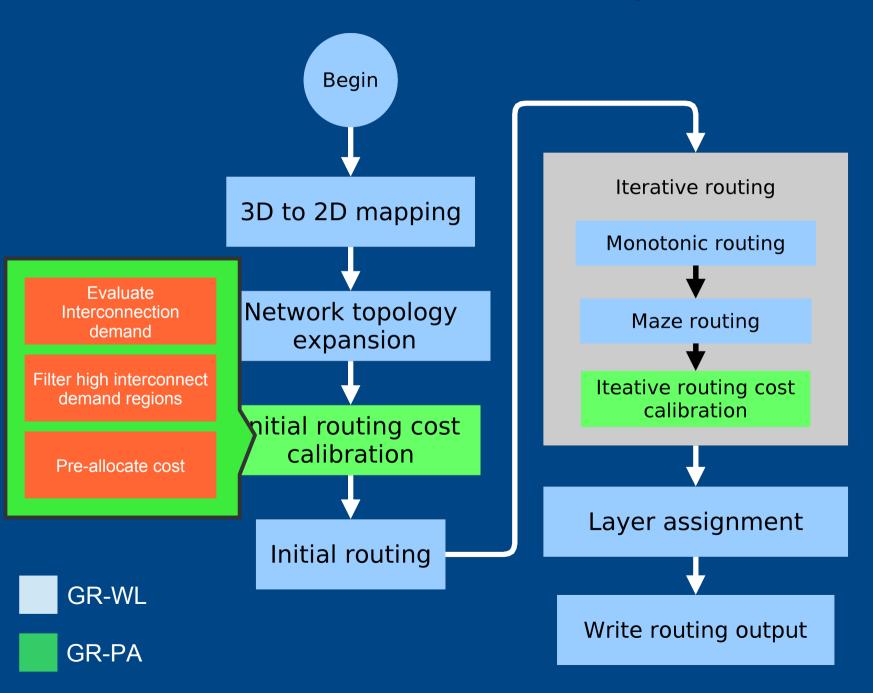
#### GR-WL

- Used as a reference implementation
- Grid based 2D router
- Network topology using MST or FLUTE
- Iterative routing based on Ripup-and-reroute
  - Monotonic routing
  - Maze routing

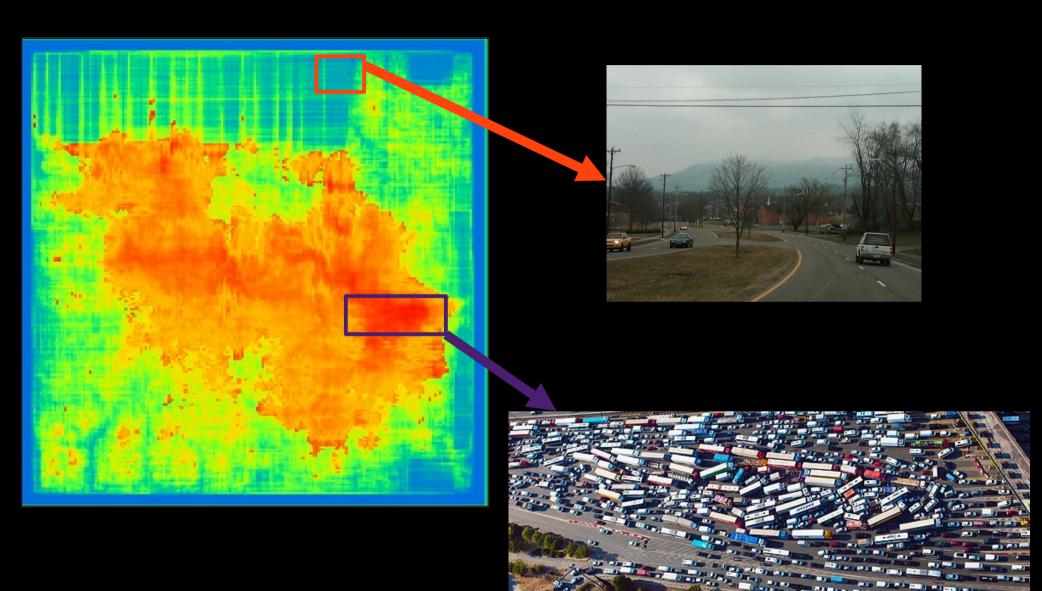


**GR-WL** 

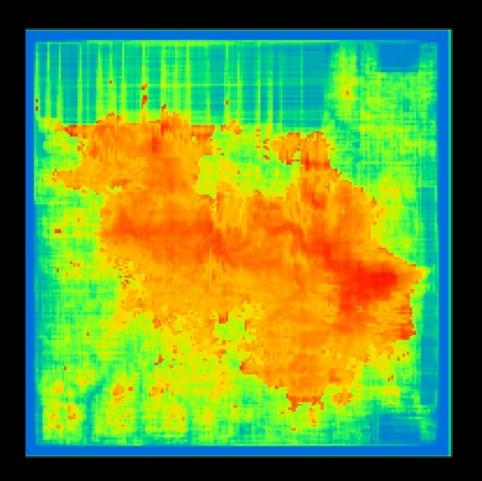
**GR-PA** 

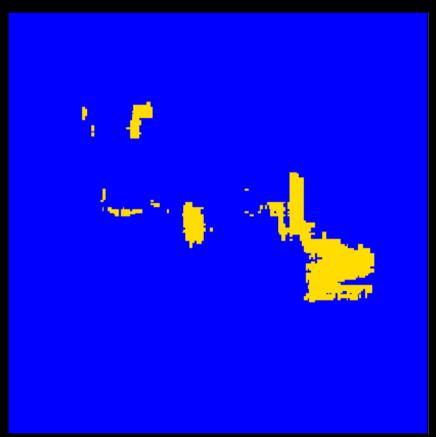


## Interconnection Demand Evaluation



### Interconnection Demand Evaluation





 $Cn / (Dn \times 100) > \beta$ 

Cn = capacity of the tile
Dn = demand of the tile
β = threshold

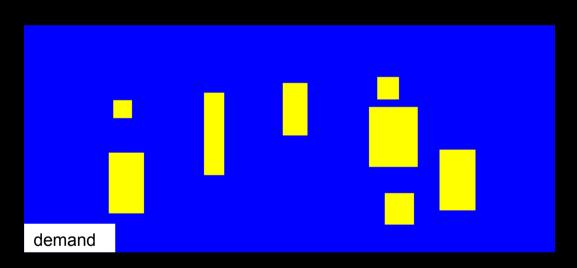
#### Cost Pre-allocation Functions

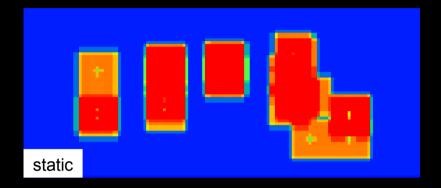
#### **Parameters**

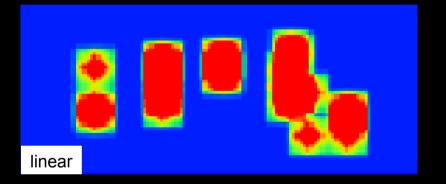
 $\psi \hbox{: Max increment}$ 

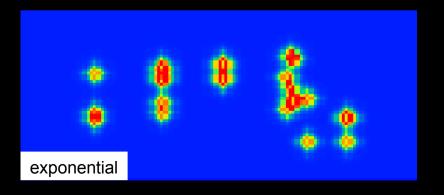
α: increment amplitude;

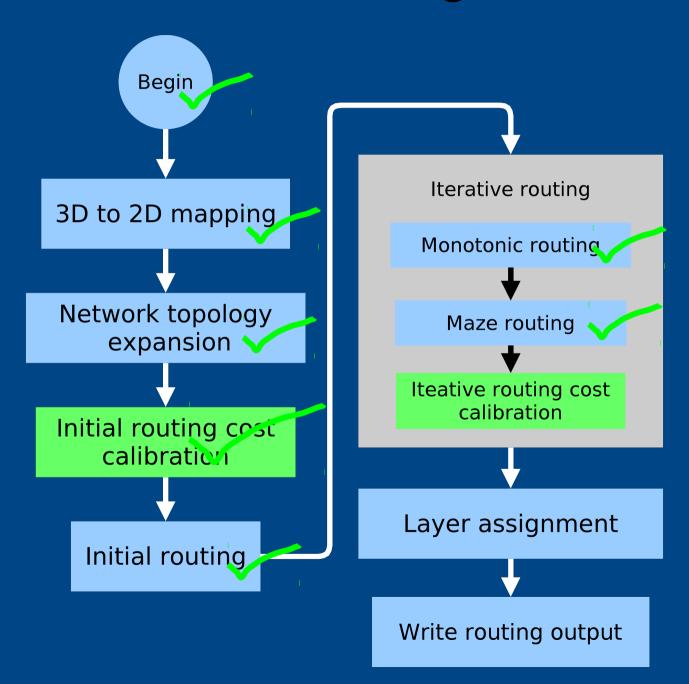
f: cost distribution function.





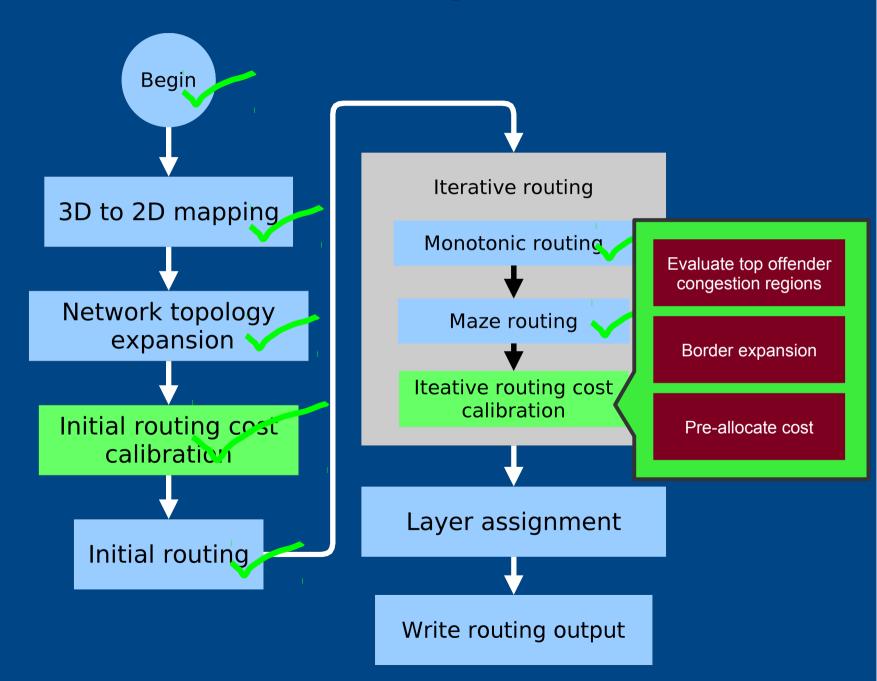






**GR-WL** 

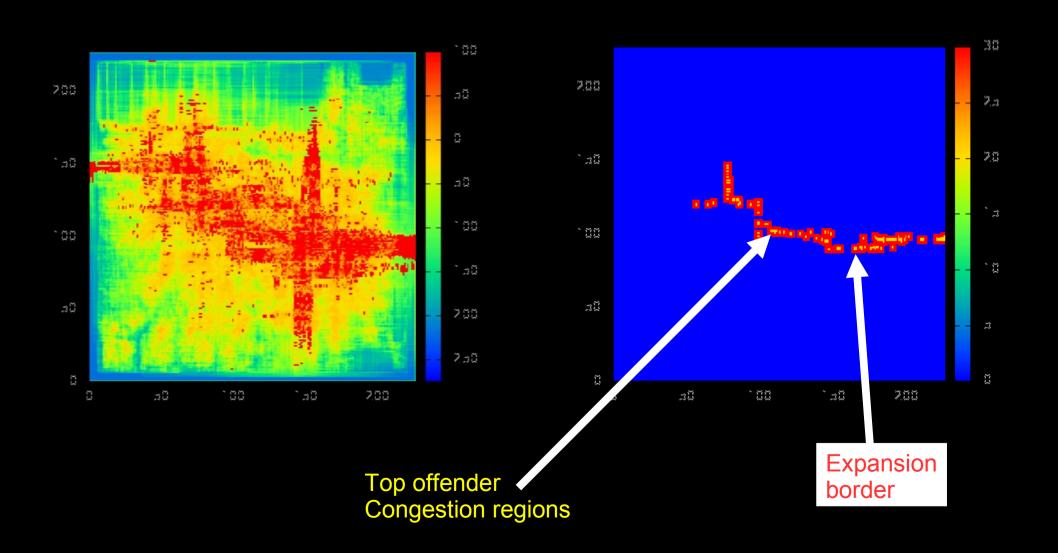
**GR-PA** 

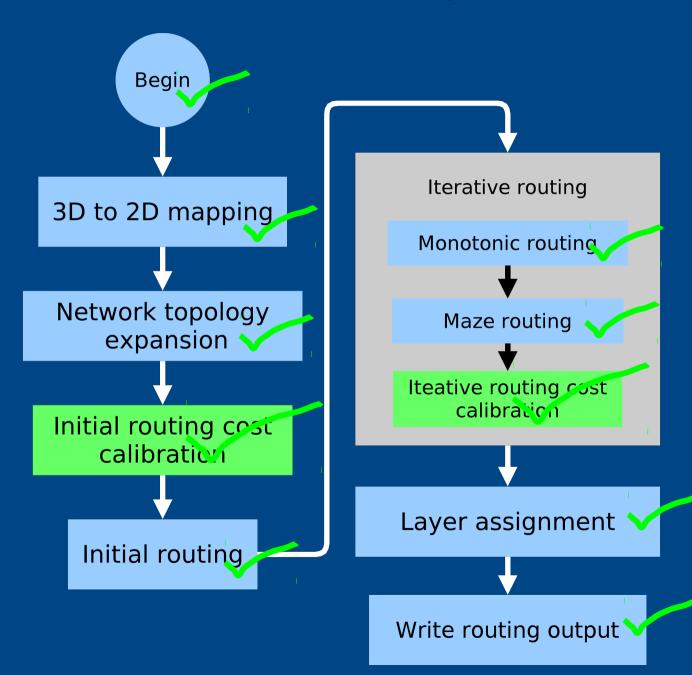


GR-WL



#### Iterative Routing Cost Calibration





**GR-WL** 

**GR-PA** 

#### Experiments

- ISPD 2008 benchmark suite
- MST was used to generate network topologies
- Exponential function for cost pre-allocation
  - **■** Ψ = 10;
  - $\bullet \alpha = 5$  and
  - $\beta = 50$

#### Results – TOF and MOF

	GR-WL		Ours	
Circuit	TOF	MOF	TOF	MOF
bb2	122	2	138 (+12%)	2
bb4	780	6	1090 (+28%)	6
nb1	588	2	504 (-16%)	2
nb3	36280	1194	37382 (+2%)	608
nb4	462	2	460 (-0.4%)	2
nb7	5172	4	4620 (-11%)	4

# Results - Wirelenght

	GR-WL	Ours	
Circuit	Wirelength	Wirelength	Difference
ad1	6380538	6418268	+0.59
ad2	6084400	6101664	+0.28
ad3	15155118	15182090	+0.17
ad4	13981761	13992148	+0.07
ad5	18102395	18149818	+0.26
bb1	6685407	6741135	+0.83
bb2	11204002	11181906	-0.2
bb3	15594684	15688085	+0.59
bb4	27602838	27481693	-0.56
nb1	5437199	5495484	+1.07
nb2	9245356	9266090	+0.22
nb3	13316366	13218553	-0.73
nb4	15329779	15410331	+0.52
nb5	26983599	27360317	+1.39
nb6	20708074	20769146	+0.29
nb7	42224489	42503107	+0.65

# Results - Execution Time (min)

	GR-WL	Ours	
Circuit	Exec. Time (min)	Exec. Time (min)	Difference (%)
ad1	46.2	41.7	-9.7
ad2	15.3	13.1	-14.4
ad3	45.4	47.5	+4.6
ad4	9.4	10.5	+11.7
ad5	120.9	103.1	-14.7
bb1	165.9	182.1	+9.8
bb2	281.3	229.6	-18.4
bb3	56.3	61.5	+9.2
bb4	197.1	161.7	-18.0
nb1	89.8	108.3	+20.6
nb2	5.4	3.5	-35.2
nb3	141.6	140.6	-0.7
nb4	323.5	213.2	-34.1
nb5	283.8	182.5	-35.7
nb6	164.6	176.4	+7.2
nb7	974.2	1138.2	+16.8

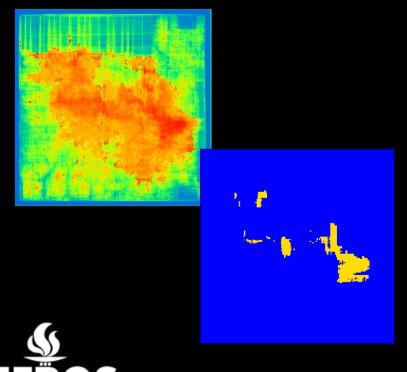
#### Conclusions

- Positive impact on execution time
  - Reduction in exec. time up to 35.7%
  - Average 6.30%
- 1.39% of maximum wirelength impact
- For the benchmarks that do not have a valid solution
  - TOF has negative impact (up to 28%) in three of six cases
  - MOF was reduced in one case and equals in all other cases

#### References

- [1] H.-Y. Chen, C.-H. Hsu, and Y.-W. Chang, High-Performance Global Routing with Fast Overflow Reduction. Asia and South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, pp. 582-587, January 2009.
- [2] Yue Xu, Yanheng Zhang and Chris Chu. "FastRoute 4.0: Global Router with Efficient Via Minimization. Asian and South Pacific Design Automation Conference, pages 576-581, 2009.
- [3] J. Westra, P. Groeneveld, Y. Tan, P. H. Madden. Global Routing: Metrics, Benchmarks and Tools, 2008.
- [4] M. D. Moffitt. Global Routing Revisited. In Proceedings of the 2009 International Conference on Computer-Aided Design (ICCAD '09). ACM, New York, NY, USA, 805-808, 2009.
- [5] T. J. Reimann. Roteamento Global de Circuitos VLSI, Microelectronics master thesis, PGMicro/UFRGS, Porto Alegre, Nov. 2011
- [6] Minsik Cho, Katrina Lu, Kun Yuan, David Z. Pan, "BoxRouter 2.0: Architecture and Implementation of a Hybrid and Robust Global Router", Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November, 2007.
- [7] Yiu-Chung Wong and Chris Chu. A Scalable and Accurate Rectilinear Steiner Minimal Tree Algorithm. In Proc. International Symposium on VLSI Design, Automation and Test, 2008.
- [8] T.-H. Wu, A. Davoodi, and J. T. Linderoth, "GRIP: Global Routing via Integer Programming", IEEE Trans. on CAD of Integrated Circuits and Systems (TCAD'11), Vol. 30, No. 1, pp. 72-84, January 2011.
- [9] Michael D. Moffitt, "MaizeRouter: Engineering an Effective Global Router", IEEE Trans. on CAD

# Global Routing Congestion Reduction with Cost Calibration Look-ahead



**PGMICRO** 

Leandro Nunes, Ricardo Reis leandron85@gmail.com, reis@inf.ufrgs.br SIM 2013 Porto Alegre/RS

# Images

- (1) http://4.bp.blogspot.com/-LudJ3cWq5nk/UTv2yQzHJpI/AAAAAAAAAAAzc/jNOmc4qKmYQ/s1600/photo-6.JPG
- (2) http://cdncms.todayszaman.com/todayszaman/2012/07/13/fsm.jpg