Federal University of Pelotas – UFPel
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Design of an 8 Points 1-D IDCT of the Emerging HEVC Video Coding Standard

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Introduction

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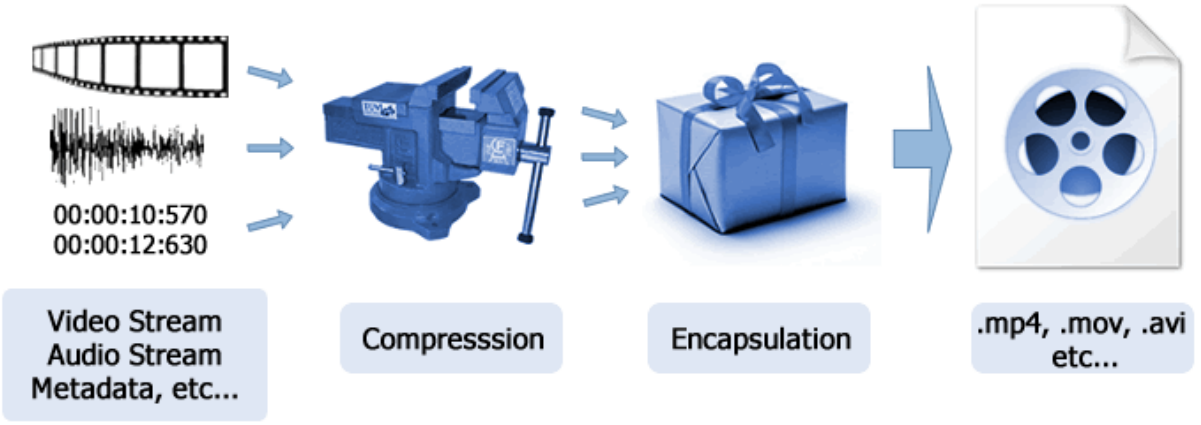
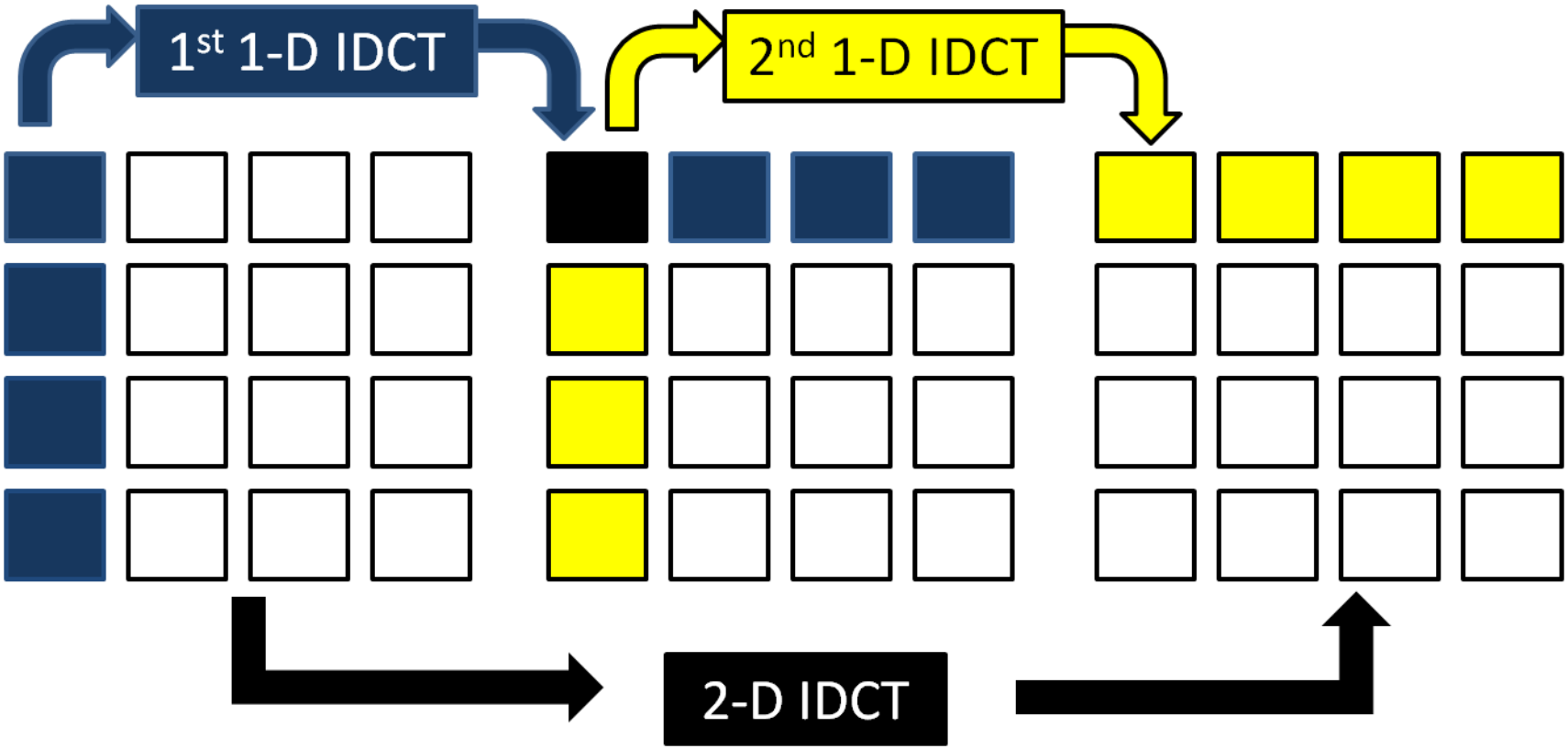
- Video Coding



IDCT 2-D

- Process to perform IDCT 2-D



IDCT 1-D

- Process to perform IDCT 1-D
  - 1º stage: Multiplications
  - 2º stage: Butterfly Operations
  - 3º stage: Rounding

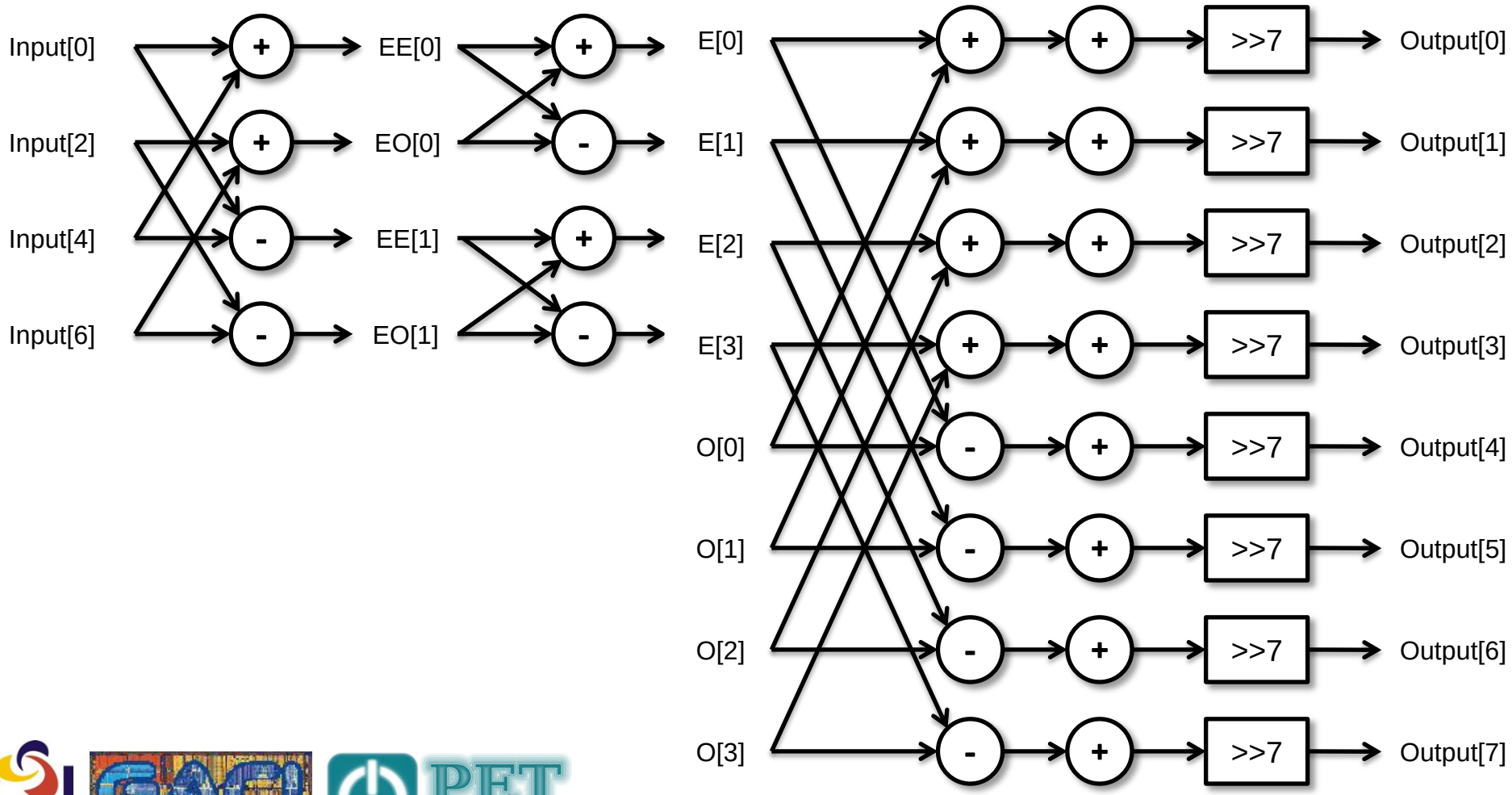
8 Points 1-D IDCT

- **Designed Architecture (1º stage):**
  - Multiplication with sums and shifters:

Constant	Sums and Shifts
89	X<<6 + X<<4 + X<<3 + X
75	X<<6 + X<<3 + X<<1 + X
50	X<<5 + X<<4 + X<<1
18	X<<4 + X<<1
83	X<<6 + X<<4 + X<<1 + X
36	X<<5 + X<<2
64	X<<6

8 Points 1-D IDCT

❑ Designed Architecture (2º and 3º stages):



Results

- The architecture was described in VHDL and synthesized to the 5SGXMABN3F45I4 Altera Stratix 5 FPGA device using Quartus II 12.1 64-Bits tool

Frequency (MHz)	ALMs	Registers
124.95	591	256

Related Work

- Related work that presents a hardware design for IDCT 8x8[2]

Features	Developed	Martuza FPGA	Martuza CMOS
Frequency (MHz)	124.95	-	211.4
Samples per Clock Cycle	8	1	1
Gate Count	-	-	12.3K
LUTs	-	706	-
ALMs	591	-	-
Frames per Second (4:2:0) QFHD	77	-	16

2 – M. Martuza, et al.”A cost effective implementation of 8 × 8 transform of HEVC from H.264/AVC” in Electrical & Computer Engineering (CCECE), 2012 25th IEEE Canadian Conference on, Montreal, Quebec, pp 1-4.

Conclusions

- This work presented the 8 Points 1-D IDCT.
- Synthesis results showed that this work is capable to process more than 30 QFHD frames per second, reaching established goals.

Future Works

- All inverse transform sizes stipulated by HEVC
- Implement a multi-size architecture which is capable to process all sizes of IDCT

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Thank You! Questions?

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