

A Fully-Integrated CMOS Class-AB Power Amplifier

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Introduction

A Power Amplifier (PA) is a circuit designed for delivering high power signal to a load, while keeping the efficiency as high as possible. Trends in the design of these circuits include its full integration in CMOS technologies and addressing the trade-offs between supply voltage, output power, power efficiency and linearity.



Proposed Topology

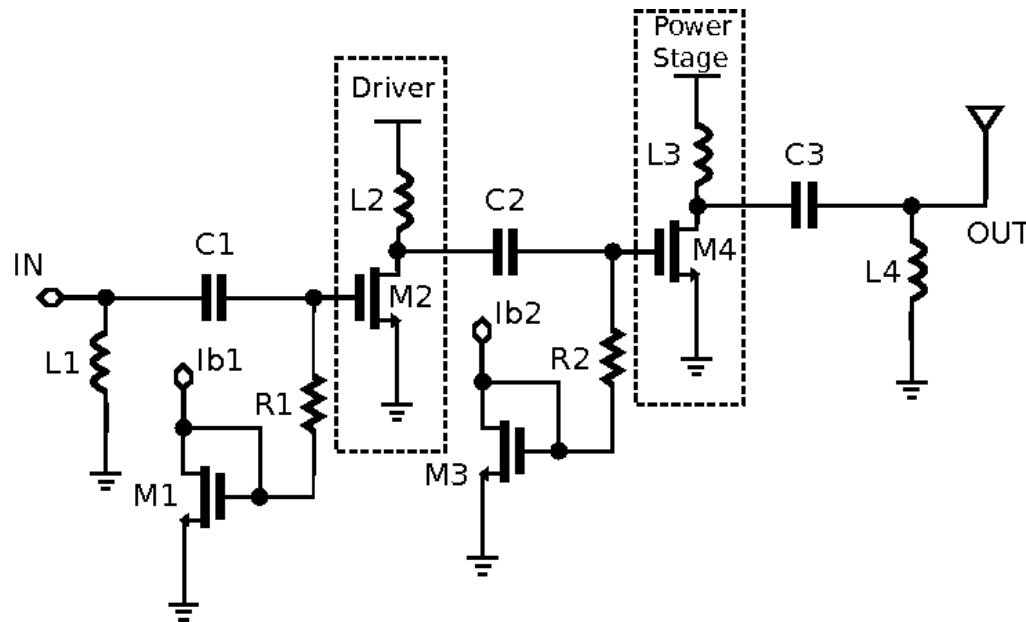


Fig.1 Topology of Proposed PA

Design Methodology

Load pull

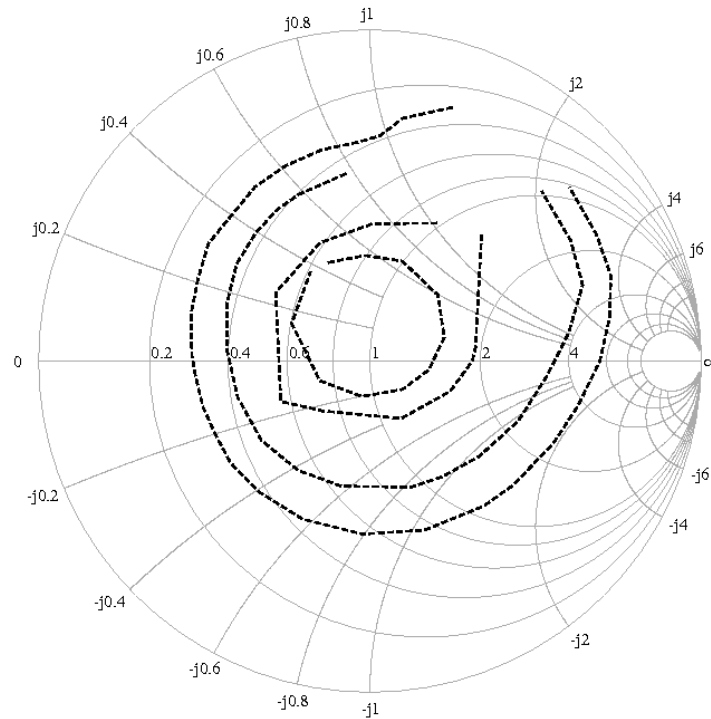


Fig.2 Load Pull Contours example for 2.4GHz

Design Methodology

Stability

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

$$\beta_{1f} = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$

$$\Delta = S_{11}S_{22} - S_{21}S_{12}$$

Design Methodology

Efficiency

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}}$$

$$n = \frac{P_{out}}{P_{DC}}$$

$$n_{AVG} = \frac{P_{out_{AVG}}}{P_{DC_{AVG}}}$$

Simulation Results

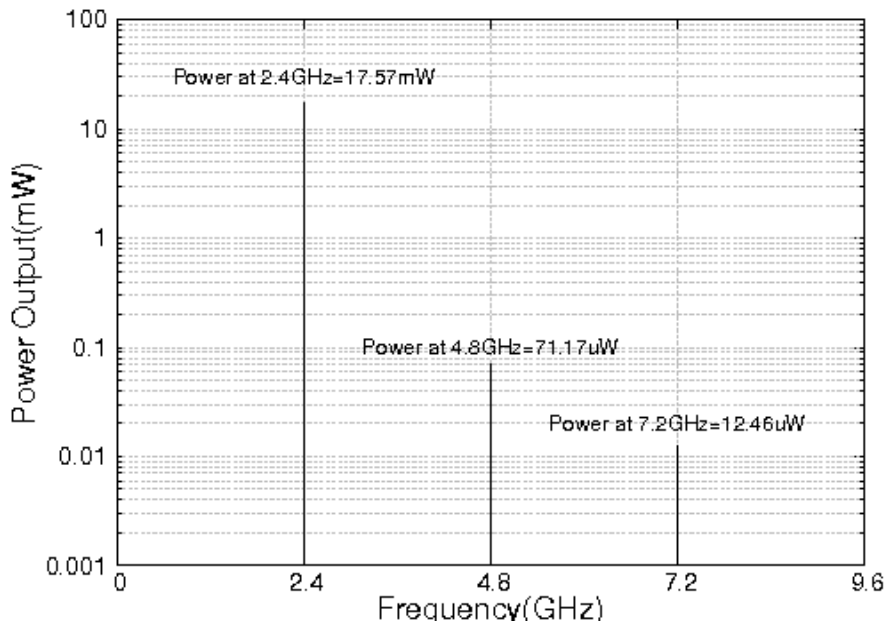


Fig.3 Spectrum of Power Output

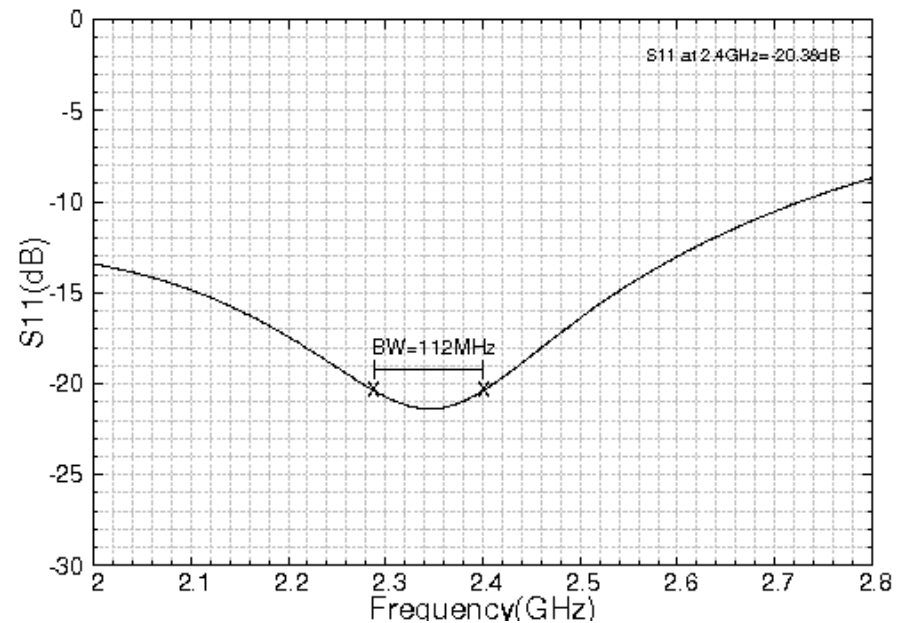


Fig.4 Curve of S-parameters analysis for (S_{11})

Simulation Results

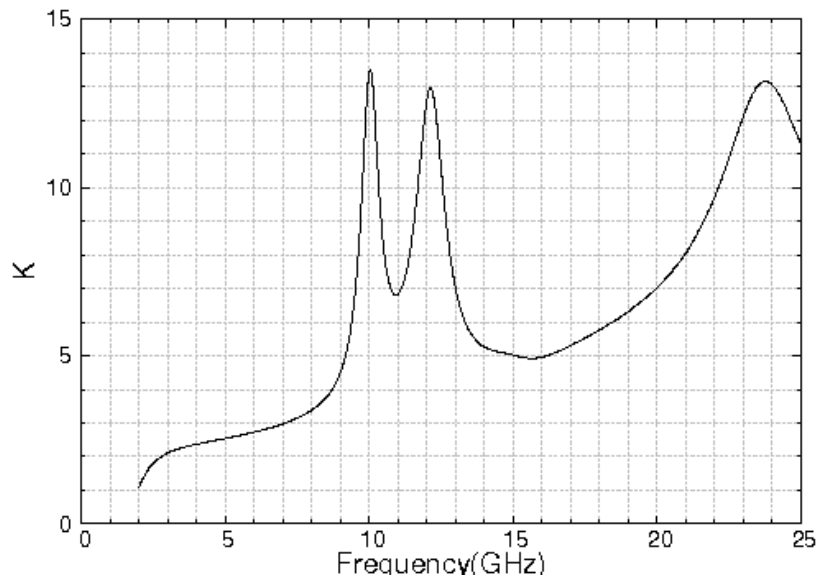


Fig.5 Stability factor K

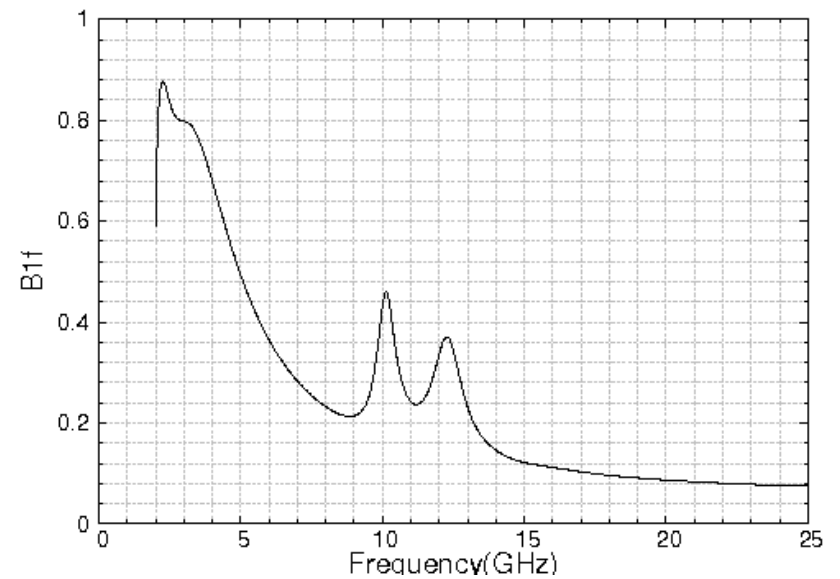


Fig.6 Alternative stability factor (β_{1f})

Simulation Results

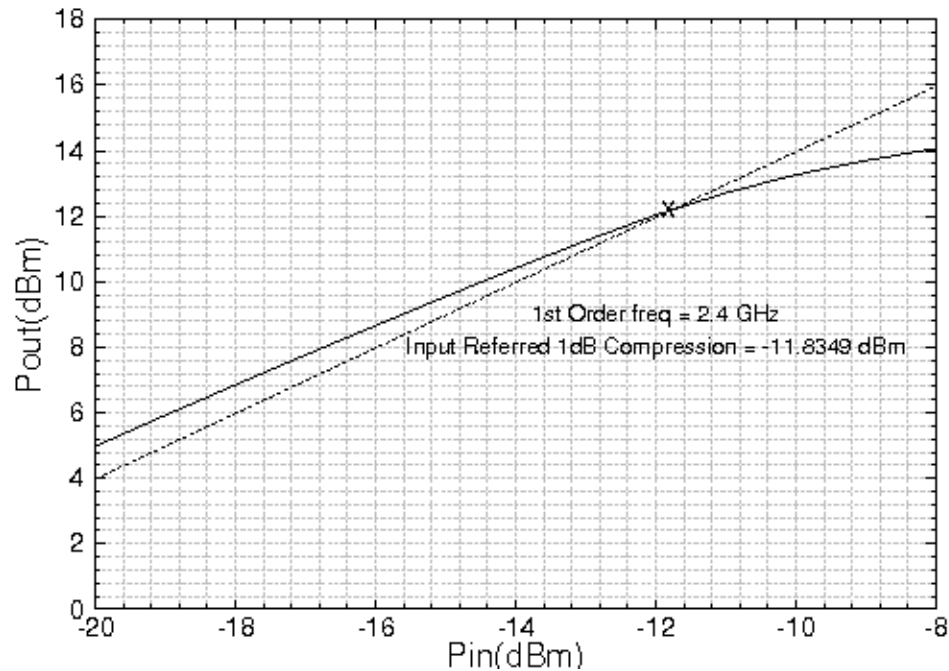


Fig.7 Curve of 1 dB Compression Point

Simulation Results

Table 1- MonteCarlo Analysis

	σ	μ	N
Output Power	1.74 mW	17.35 mW	442
Power Consumption	1.65 mW	41.92 mW	442
K	0.032	1.70	442
β_{1f}	0.004	0.85	442
S_{11}	1.034 dB	-20.278 dB	442
Efficiency	2.67 %	41.4 %	442

Simulation Results

Table 2- Corners Analysis

Corners	Output Power (mW)	DC Consumption (mW)	K	β_{1f}	S_{11} (dB)	n (%)
Nominal	17.57	42.08	1.7	0.856	-20.38	41.75
ff	21.64	46.02	1.652	0.856	-22.09	47.02
ss	13	37.53	1.765	0.855	-18.75	34.63
fff	23.03	47.4	1.638	0.855	-22.8	48.58
ssf	12.03	36.57	1.779	0.855	-18.42	32.89

Layout

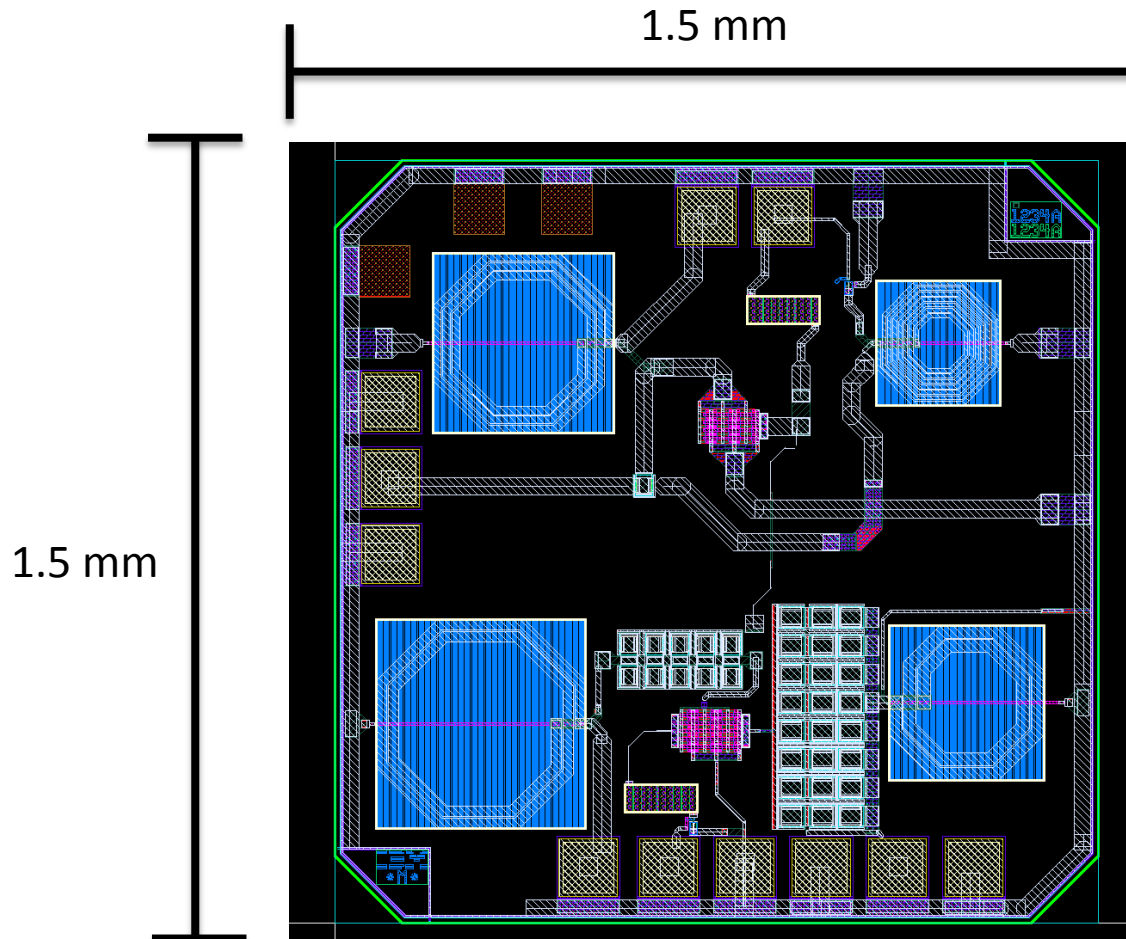


Fig.8 Power Amplifier Layout

Conclusion

A fully-integrated 2.4 GHz power amplifier implemented in standard CMOS 0.18- μm technology was presented. By using a driver and power stage as well as on-chip input and output matching networks, the presented PA achieves high gain and high output power. It can submit an output power of 12.45 dBm with 41% of drain efficiency, in the power stage, for a input power of -11.42 dBm. The corners and montecarlo analysis showed good accuracy with the typical simulations.

Thanks

Questions?

