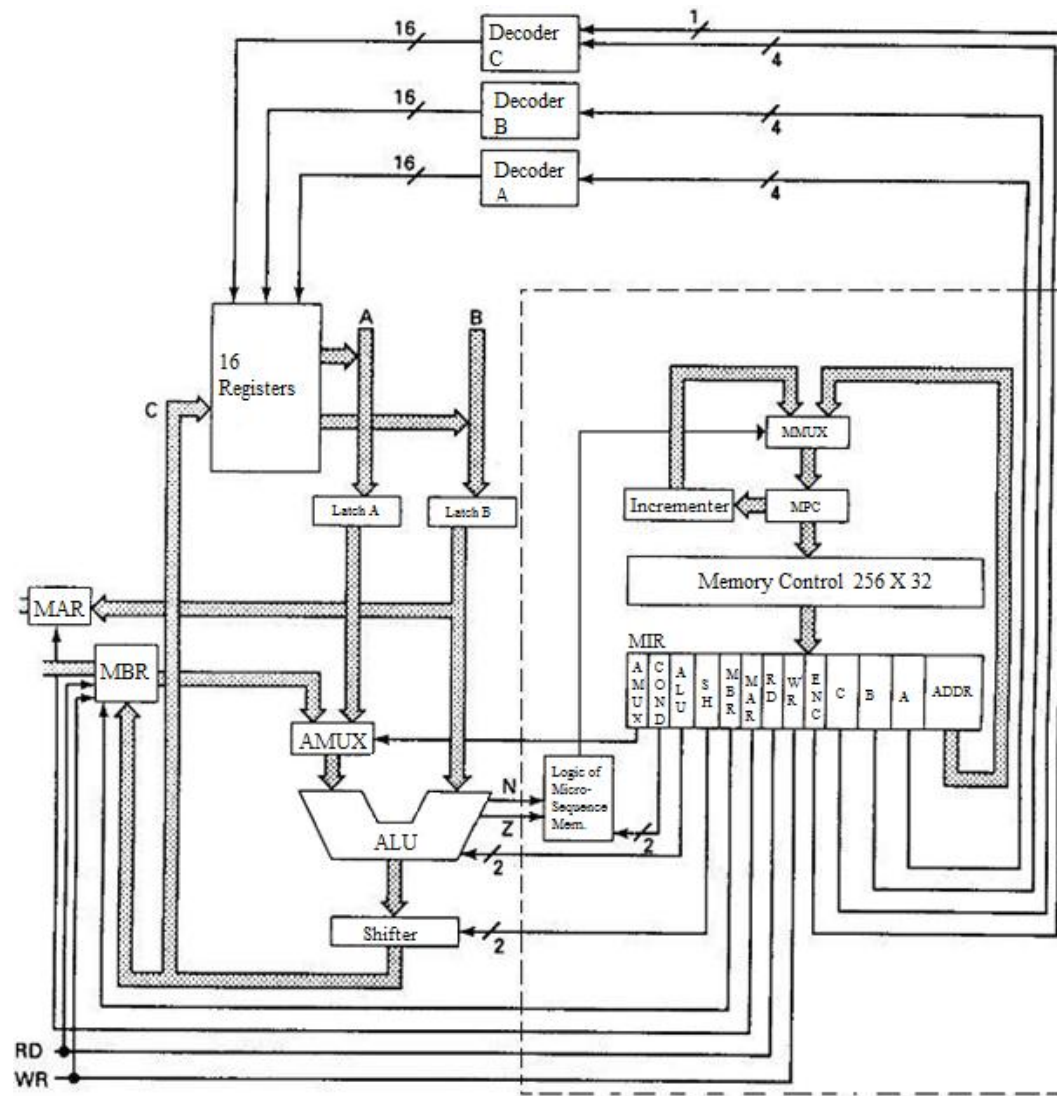


Design of a Didactic Processor in FPGA

Fernanda Mota, Bruno Leonardo, Vagner Rosa



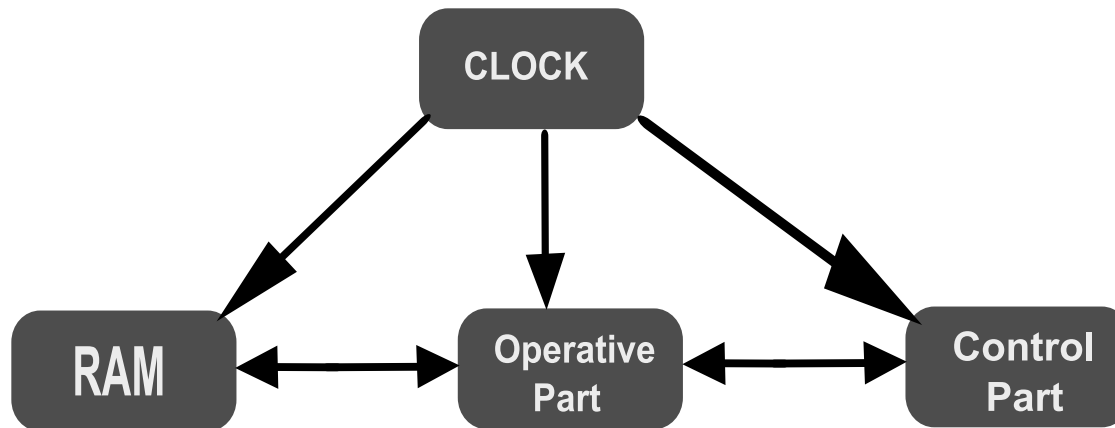
Introduction



Introduction

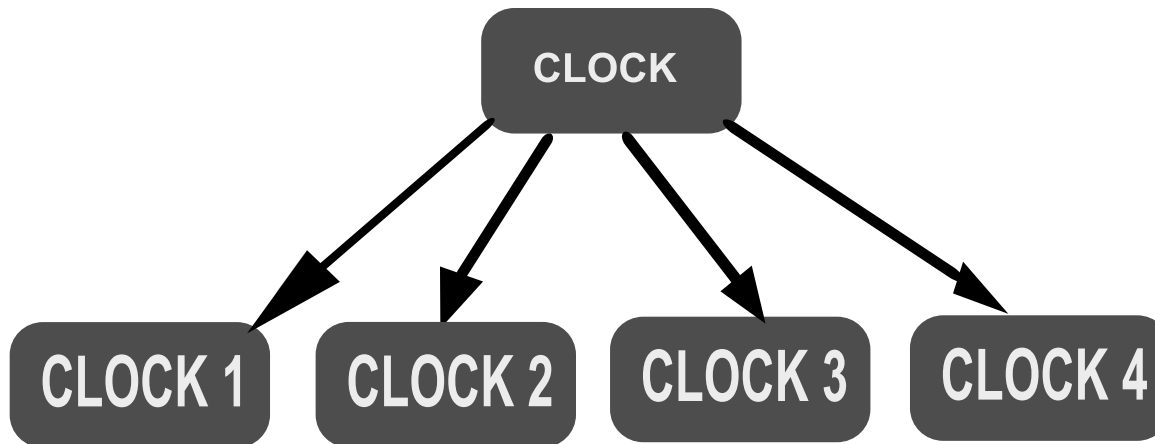
- The following changes in the architecture of the book Tanenbaum MAC-1 were found to be necessary :
 - ☐ **Clock**
 - ☐ **Latches**
 - ☐ **ROM/RAM**

Implementation



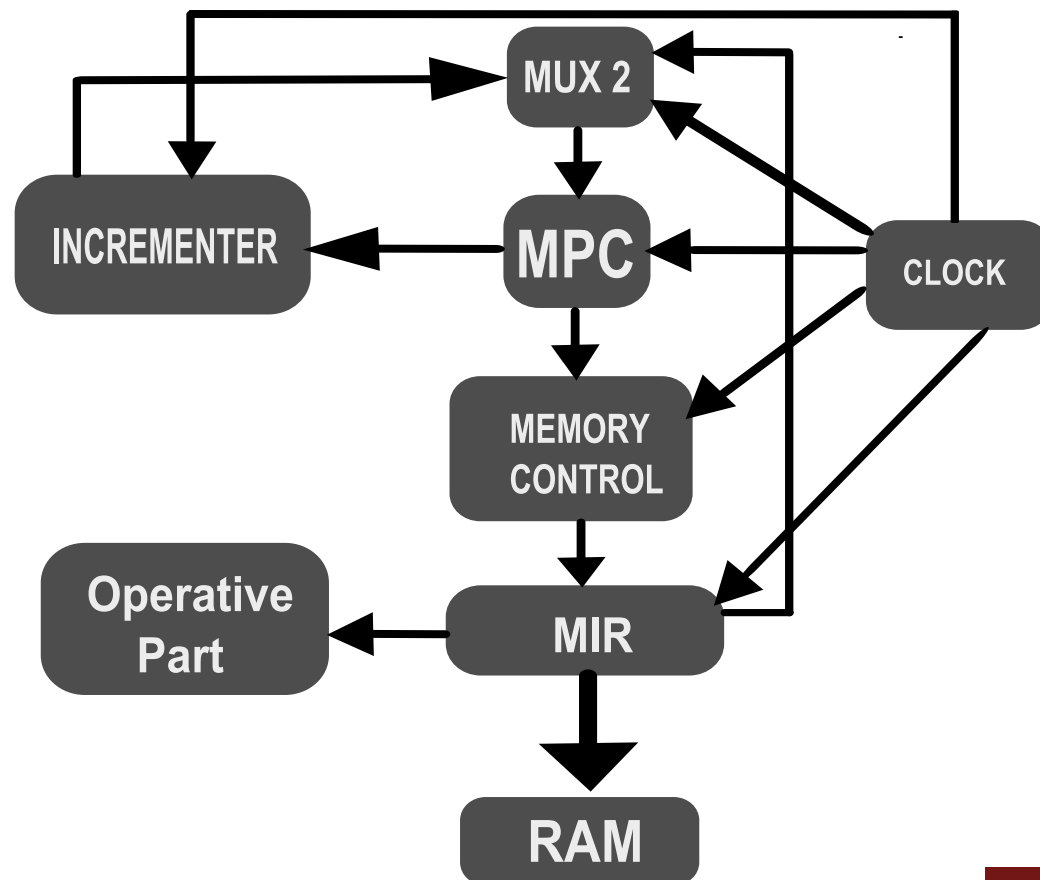
Implementation

➤ Clock



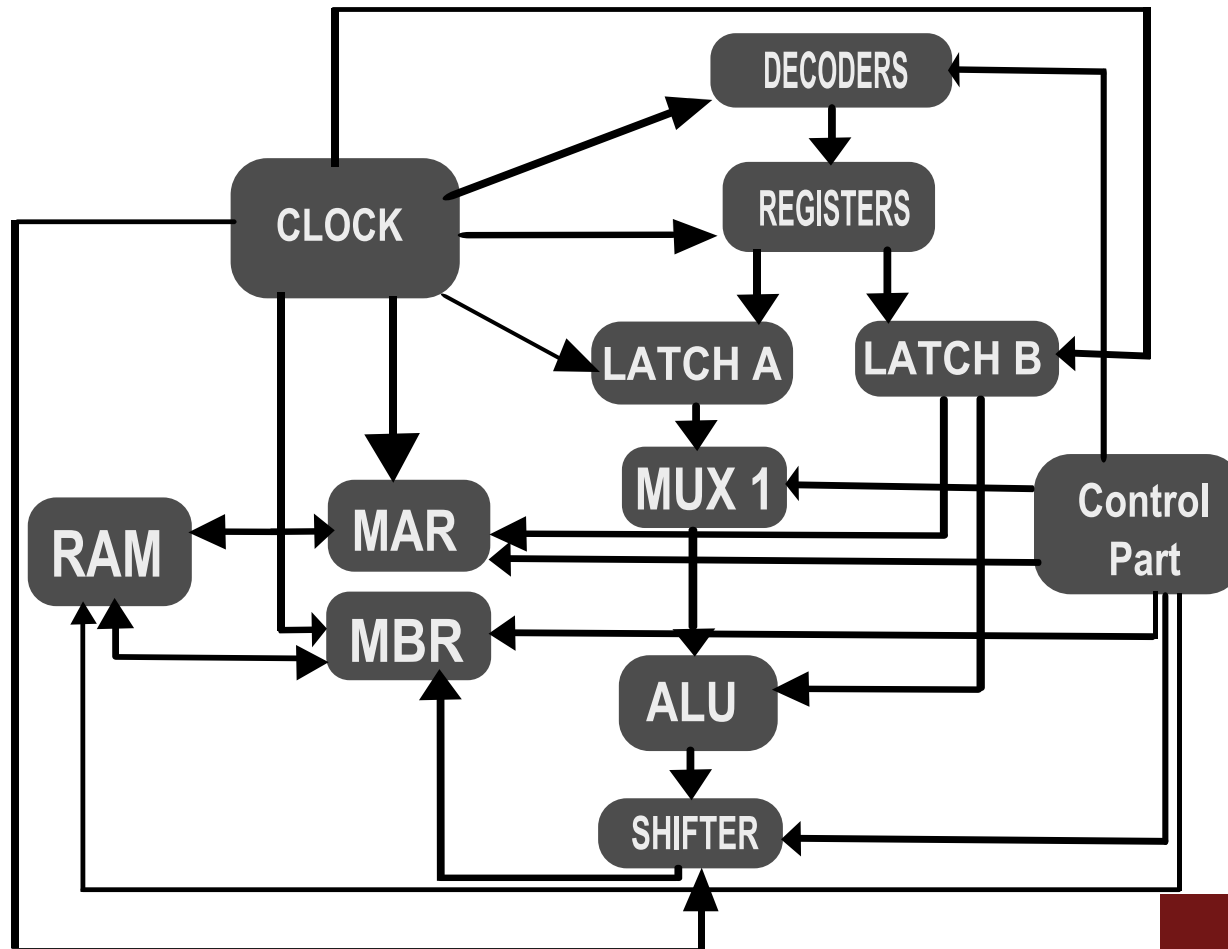
Implementation

➤ Control Part



Implementation

➤ Operation Part



Results

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Total Number Slice Registers	401	9,312	4%
Number used as FlipFlops	385		
Number used as latches	16		
Number of 4 input LUTs	2,387	9,312	25%
Number of occupied Slices	1,269	4,656	27%
Number of Slices containing only related logic	1,269	1,269	100%
Number of Slices containing unrelated logic	0	1,269	0%
Total Number of 4 input LUTs	2,436	9,312	26%
Number used as logic	1,331		
Number used as route-thru	49		
Number used for 32X1 RAMs	1,056		
Number of bonded IOBs	47	232	20%
IOB Flip Flops	11		
Number of RAMB 16s	1	20	5%
Number of BUFGMUXs	4	24	16%
Average Fanout of Non-Clock Nets	5.48		

Results



Conclusion and Future Work

➤ Conclusion:

- ☐ Relatively simple architecture
- ☐ Implementation and validation required the much knowledge of the Xilinx's design flow and FPGA restrictions.
- ☐ Need for architectural adaptations made this design appropriate for didactic purposes.

➤ Future Work:

- ☐ Will be implemented as improvements in control words to avoid repetition of commands that are generated in the current architecture, using a flag to indicate when the result of the MBR and MAR are stable.
- ☐ CLP based on this microprocessor is planned.

References

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