Federal University of Pelotas Group of Architectures and Integrated Circuits

An Architecture for the new Adaptive Loop Filter of the High Efficiency Video Coding

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Outline

- Introduction
- □ HEVC High Efficiency Video Coding
- □ ALF Adaptive Loop Filter
- Proposed Architectures
- Results
- Conclusions





Introduction

Digital video popularization;

> Several devices that held digital video;

➤ Inviable task without video compression.





HEVC

- > The H.264/AVC standard is still the state-of-art;
- Higher resolutions demand;
- High Efficiency Video Coding HEVC;
- > HEVC goals:
 - Double H.264 compression rates;
 - Same or reduced computational complexity;
- New techniques are required;





ALF

- Subjective quality of video is deteriorated with coding steps;
- ALF was removed after Working Draft 7 due to high complexity;
- Possible future reinsertion on HEVC's new profile (High efficiency)





ALF

Aims to reduce the image distortion;

> Two core sizes: 5x5 and 9x9;

> Filter coefficients generated by Wiener filters.

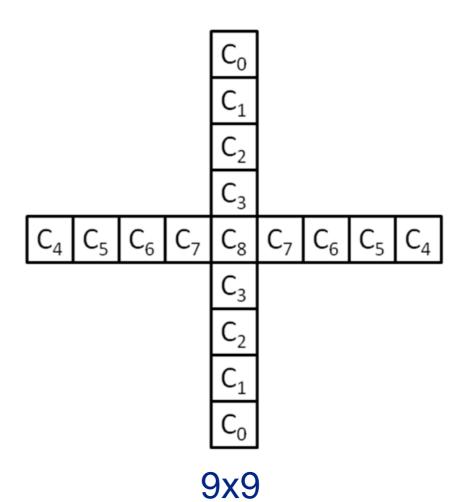




ALF

C_0		C_1		C ₂
	C_3	C_4	C ₅	
C_6	C ₇	C ₈	C ₇	C_6
	C ₅	C ₄	C_3	
C_2		C_1		C_0

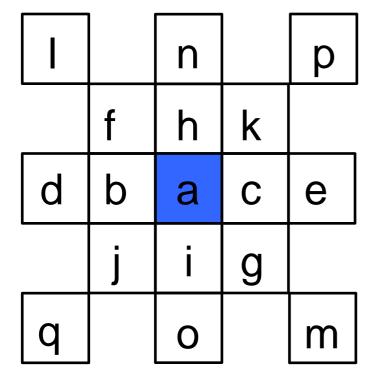
5x5







Video Samples

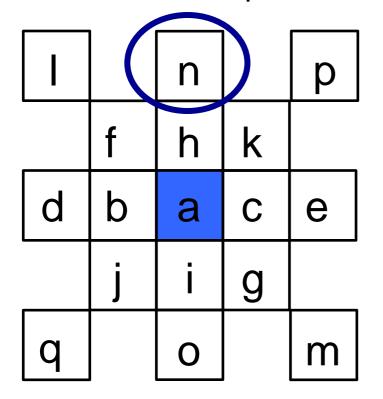


C_6		C_7		C ₈
	C_3	C_4	C_5	
C_2	C_1	C_0	C_1	C_2
	C_5			
C_8		C ₇		C_6

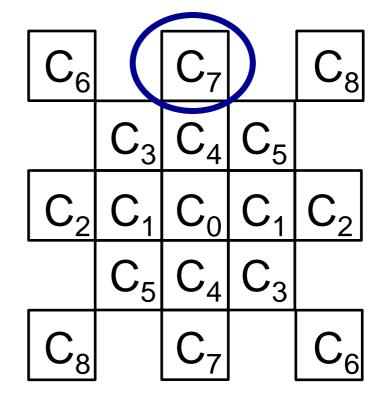




Video Samples



Filter Coefficients

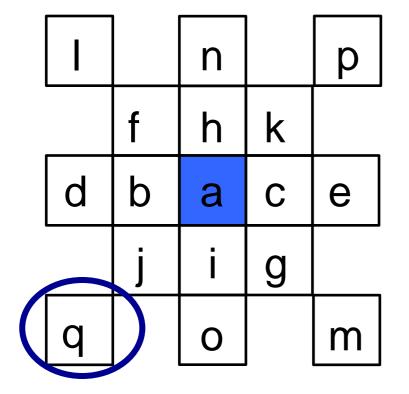


 $(n * C_7)$





Video Samples



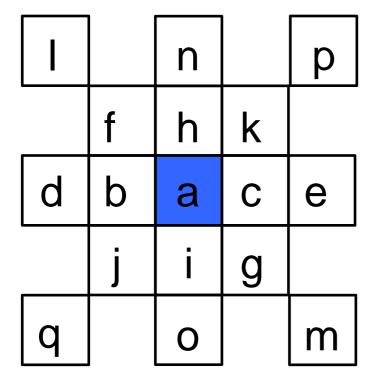
C_6		C ₇		C ₈
	C_3	C_4	C_5	
C_2	C_1	C_0	C_1	C_2
	C_5		C_3	
C_8		C ₇		C_6

$$(q * C_8)$$





Video Samples



$$egin{array}{c|cccc} C_6 & C_7 & C_8 \\ \hline C_2 & C_1 & C_0 & C_1 & C_2 \\ \hline C_2 & C_5 & C_4 & C_3 \\ \hline C_8 & C_7 & C_6 \\ \hline \end{array}$$

$$(I * C_6) + (f * C_3) + (h * C_4) + ... + (m * C_6)$$

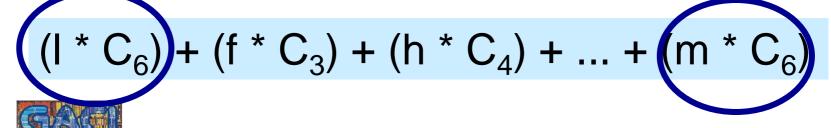




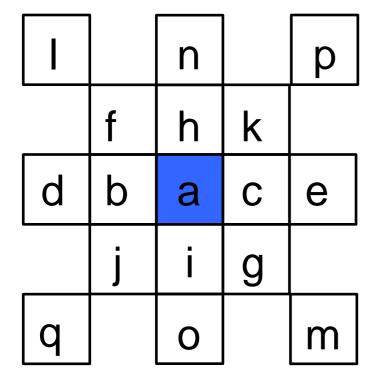
Video Samples

		n		р
	f	h	k	
d	b	a	С	е
	j	i	g	
q		0		m

C_6		C ₇		C ₈
	C_3	C_4	C_5	
C_2			C_1	C_2
	C_5			
C ₈		C ₇		C_6



Video Samples



$$egin{array}{c|cccc} C_6 & C_7 & C_8 \\ \hline C_3 & C_4 & C_5 \\ \hline C_2 & C_1 & C_0 & C_1 & C_2 \\ \hline C_5 & C_4 & C_3 \\ \hline C_8 & C_7 & C_6 \\ \hline \end{array}$$

$$((I + m) * C_6) + ...$$





Video Samples

		n		р		C_6		C_7		C ₈
	f	h	k				C_3	C_4	C_5	
d	b	a	C	е		C_2	C_1	C_0	C_1	C_2
	j	i	g				C_5	C_4	C_3	
q	Reduce multipliers from 17 to 8									

$$((I + m) * C_6) + ...$$





Proposed Architecture

> ALF Core based on HEVC Draft Version 7.0

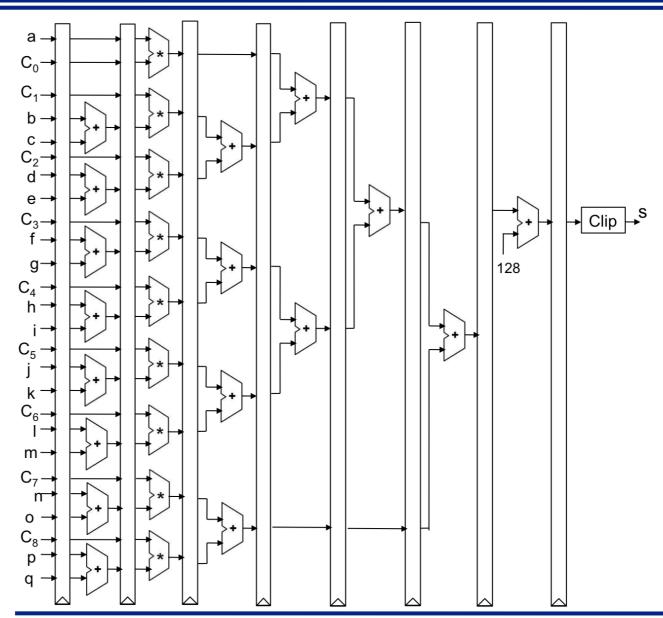
Described in VHDL;

Synthesized for Altera Stratix II EP2S15F484C3 FPGA;





Proposed Architecture for ALF 5x5







Synthesis Results

Filter Size	ALF Core
ALUTs	371 (2 %)
Total Registers	613 (<1%)
Embedded Multiplier 9-bit	14 (5%)
Frequency (MHz)	326

Altera Stratix II EP2S15F484C3





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Comparison

Filter Size	ALF Core
Adders	17
Multipliers	9
Clipping	1
Pipeline stages	8





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Estimated Processing Rates

Video resolution	ALF Core
720p (1280x720)	353
1080p (1920x1080)	157
WQXGA (2560x1600)	79
QFHD(3840x2160)	39





Frame's per second

Conclusions and Future Work

- This work shown the hardware design for the ALF Core;
- High Throughput;
- At least 157 1080p and 39 QFHD frames per second;
- > Future works:
 - Other ALF steps;
 - > Architecture for the entire ALF.





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Thank You!

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