Performance and Power Consumption Analysis of Full Adders Designed in 32nm Technology

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28º Simpósio Sul de Microeletrônica – SIM 2013

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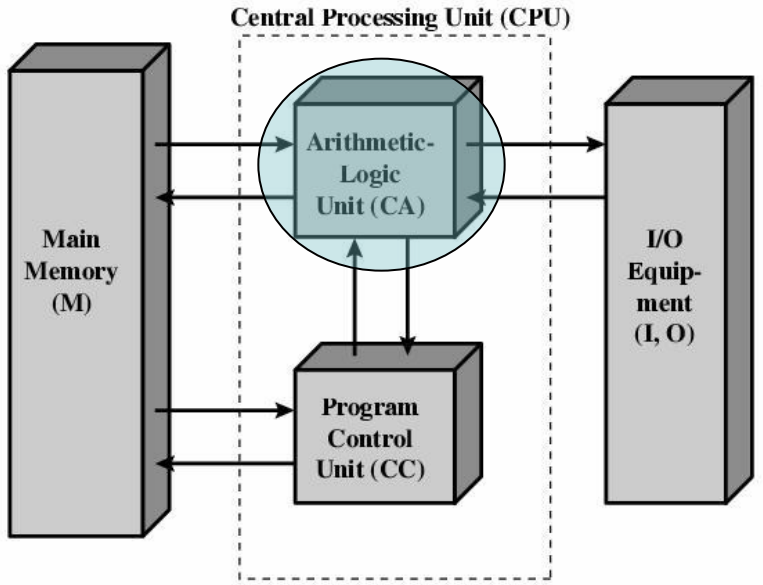
Introduction

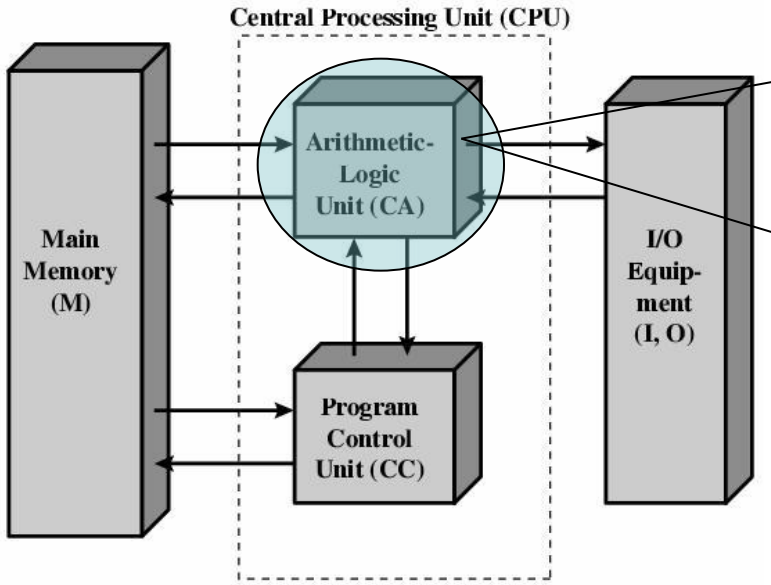
Full adders are largely used in computational systems.



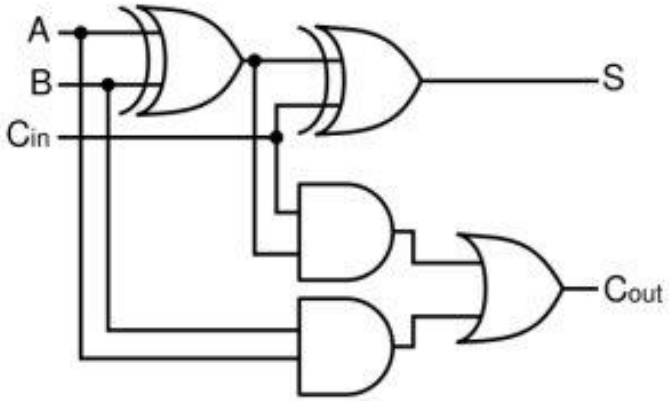
Von Neumann Architecture

Introduction

The full adder is a digital circuit which implement the function of sum of one bit.



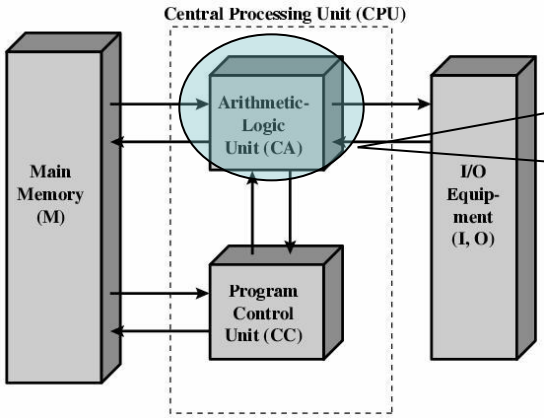
Von Neumann Architecture



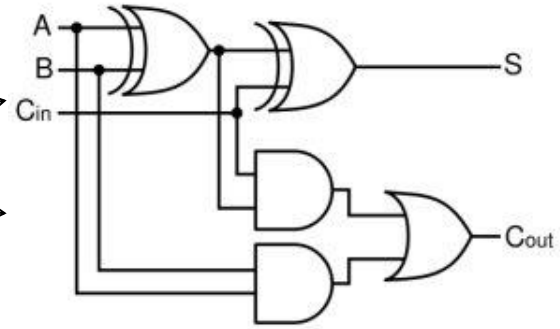
Full Adder

Introduction

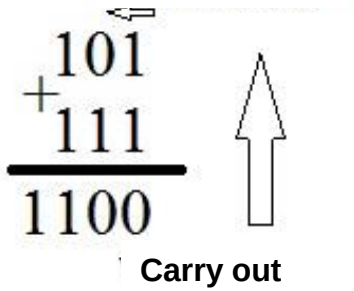
In processing of instructions of computational systems, the sum is among the micro-operations more frequently realized.



Von Neumann Architecture

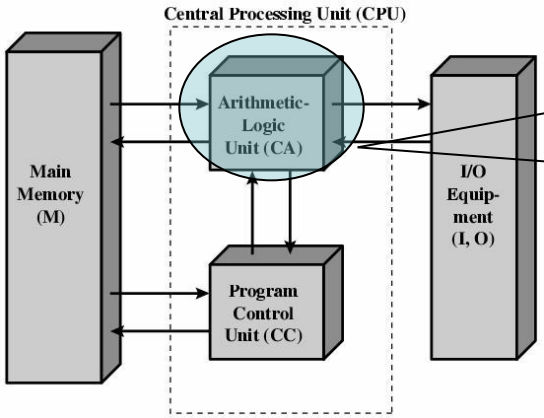


Full Adder

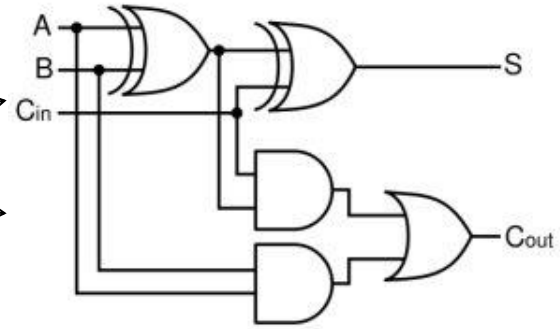


Introduction

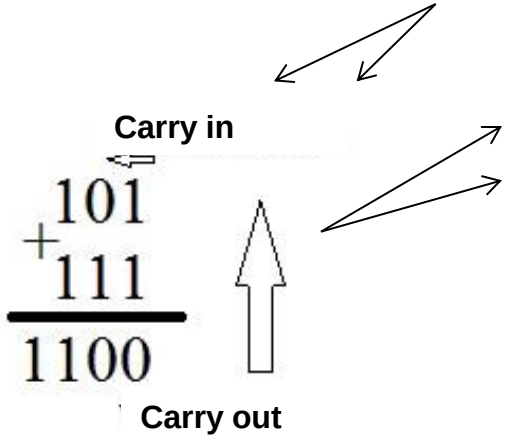
The full adder truth table is:



Von Neumann Architecture



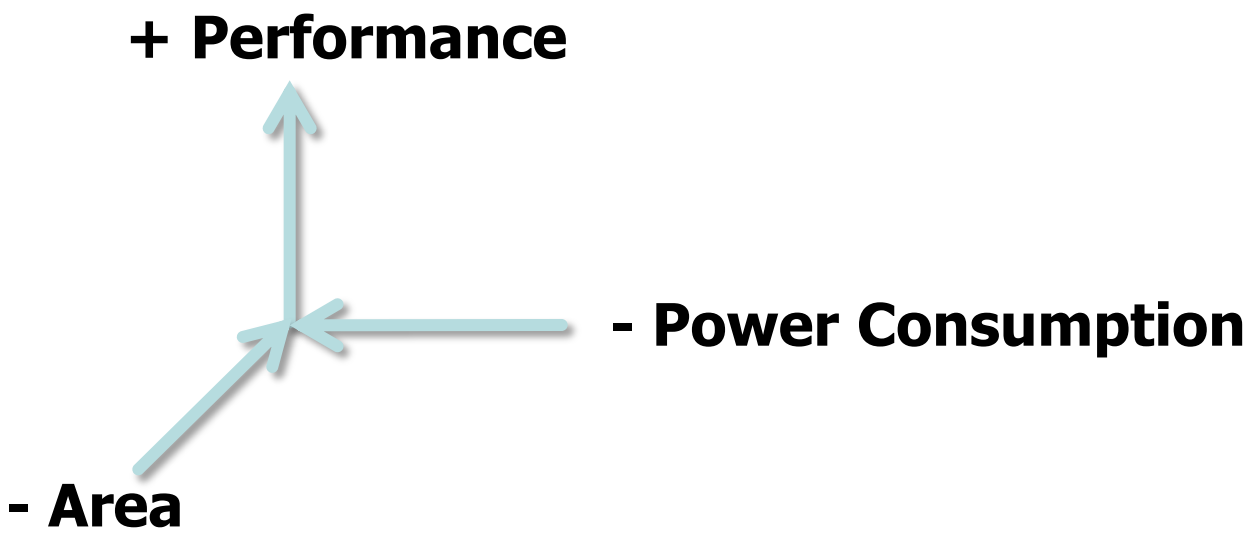
Full Adder



A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Objective

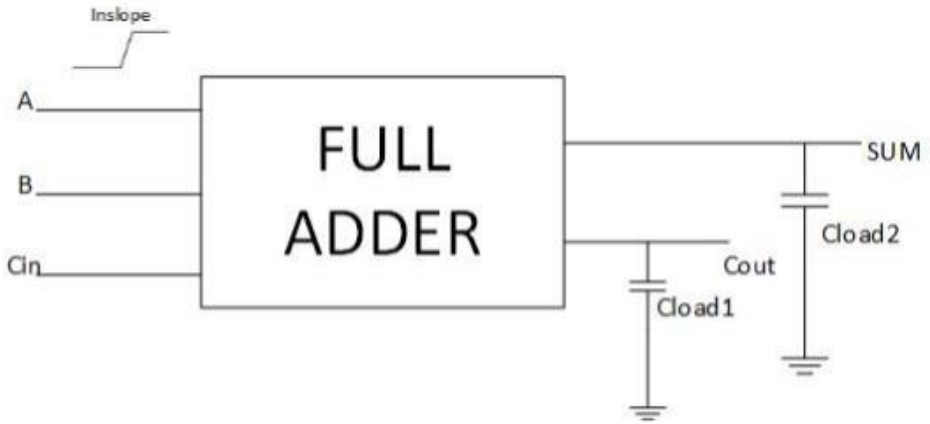
The main objective of this work is **evaluate and compare** different proposals of **full adders**, each with its advantages for use in accordance to project constraints: **performance, area and power consumption.**



Methodology

- Two groups of full adders gates:
  - Six classical architectures
  - 3-blocks strategy

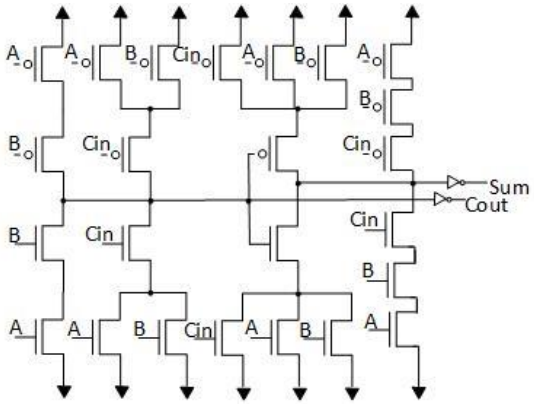
- Characterization through electrical simulations:
  - NGSpice[1]
  - Used values:
    - Technology = 32nm*
    - Nominal voltage= 0,9V
    - Capacitance output = 1fF
    - In slope = 0,01ns
    - Transistors sizing = 100nm



[1] NGSpice. Available at: http://ngspice.sourceforge.net/

[*] W. Zhao, Y. Cao, "New generation of Predictive Technology Model for sub-45nm early design exploration“ IEEE Transactions on Electron Devices, vol. 53, no. 11, pp. 2816-2823, November 2006

Six Classical Archtectures



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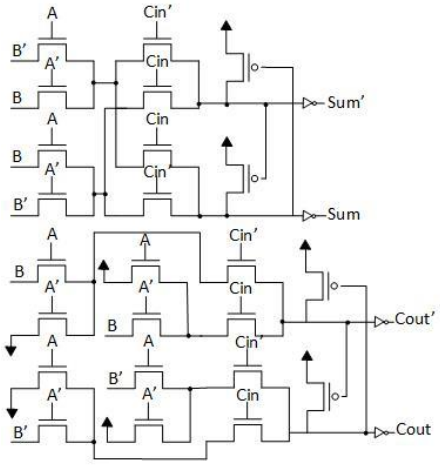
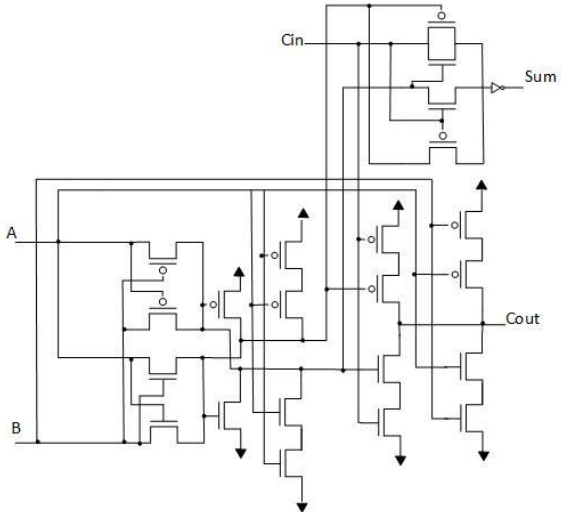


CPL



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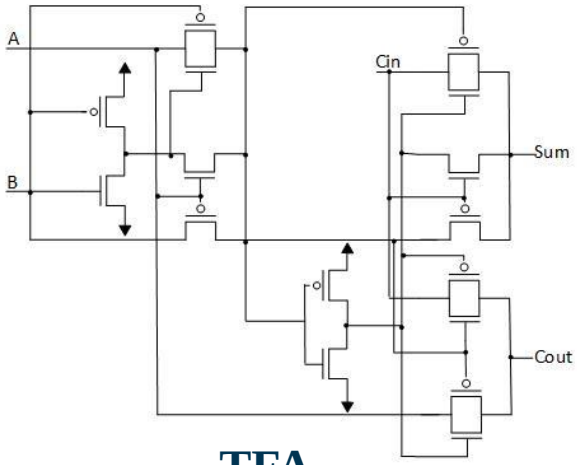

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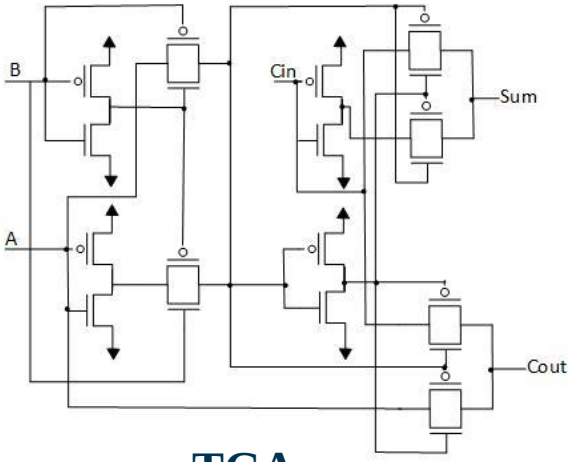
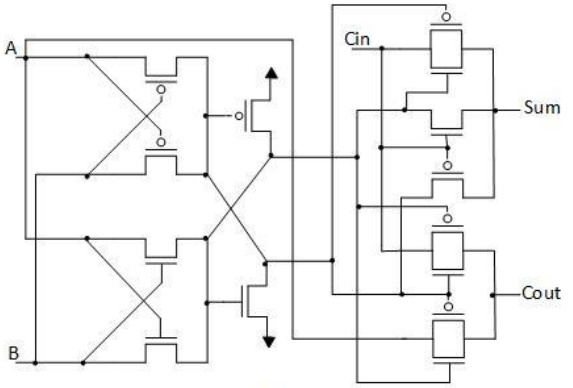


TGA



14T

3-Blocks Strategy

Objective: create different adders through of link 3 different starting blocks[1].

$$Sum = (A \oplus B) \oplus Cin$$

$$Cout = A.B + Cin.(A \oplus B)$$

- Block 1

  $H = A \oplus B$

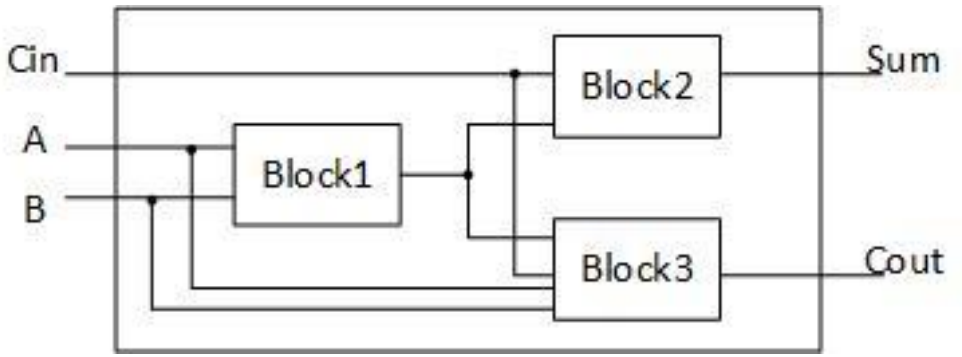
- Block 2

  $Sum = H \oplus Cin$

- Block 3

  $Cout = A.H' + Cin.H$

  $Cout = [A*(B+Cin)] + (B*Cin)$

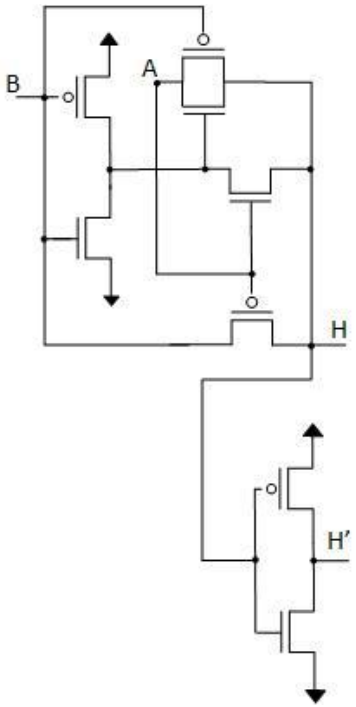


LINK BLOCKS

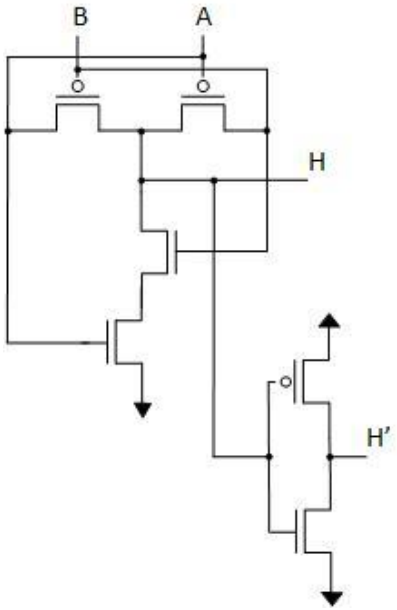
1 V. Moalemi and A. Afzali-Kusha, *Subthreshold 1-Bit Full Adder Cells in sub-100nm Technologies*, IEEE Computer Society Annual Symposium on VLSI (ISVLI'07)(2007).

3-Blocks Strategy - Block1 Designs

- $H = A \oplus B$



A



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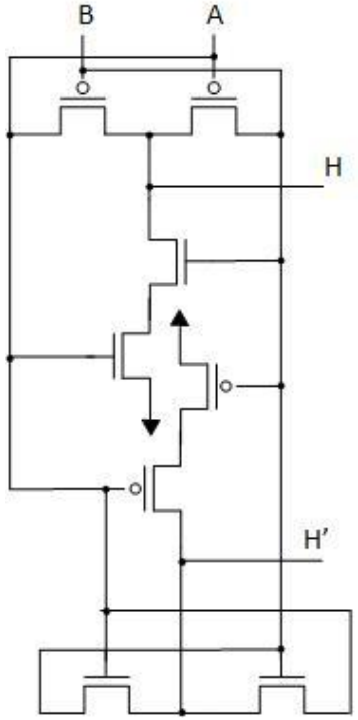
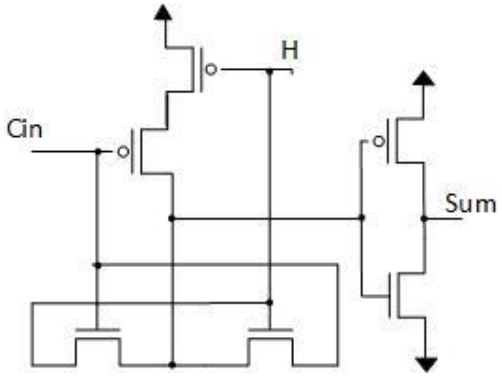


C

3-Blocks Strategy – Block2 Designs

- Sum = H ⊕ Cin



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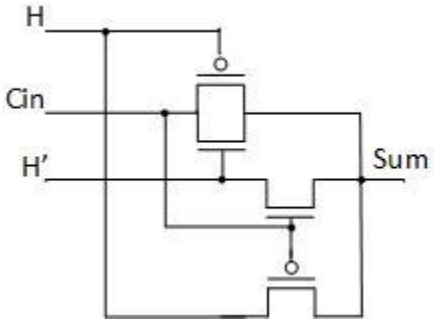

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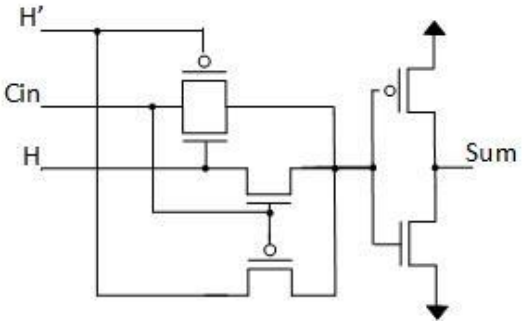

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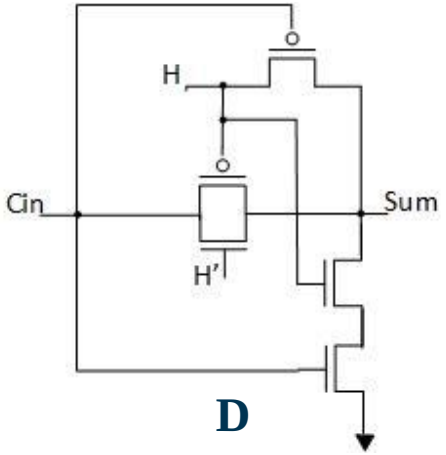
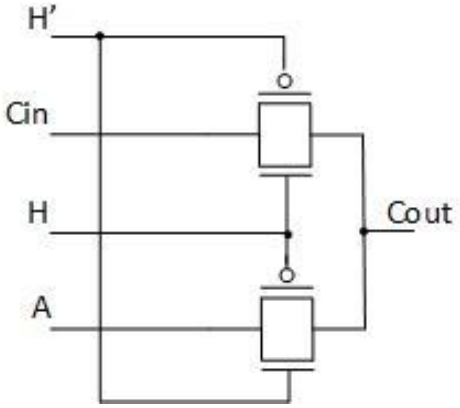


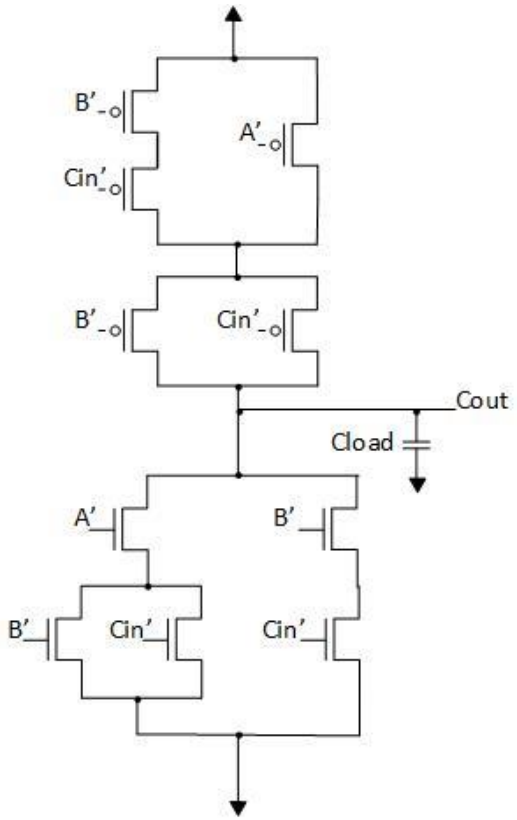
D

3-Blocks Strategy – Block3 Designs



1

$$Cout = A.H' + Cin.H$$



2

$$Cout = [A*(B+Cin)] + (B*Cin)$$

3-Blocks Strategy

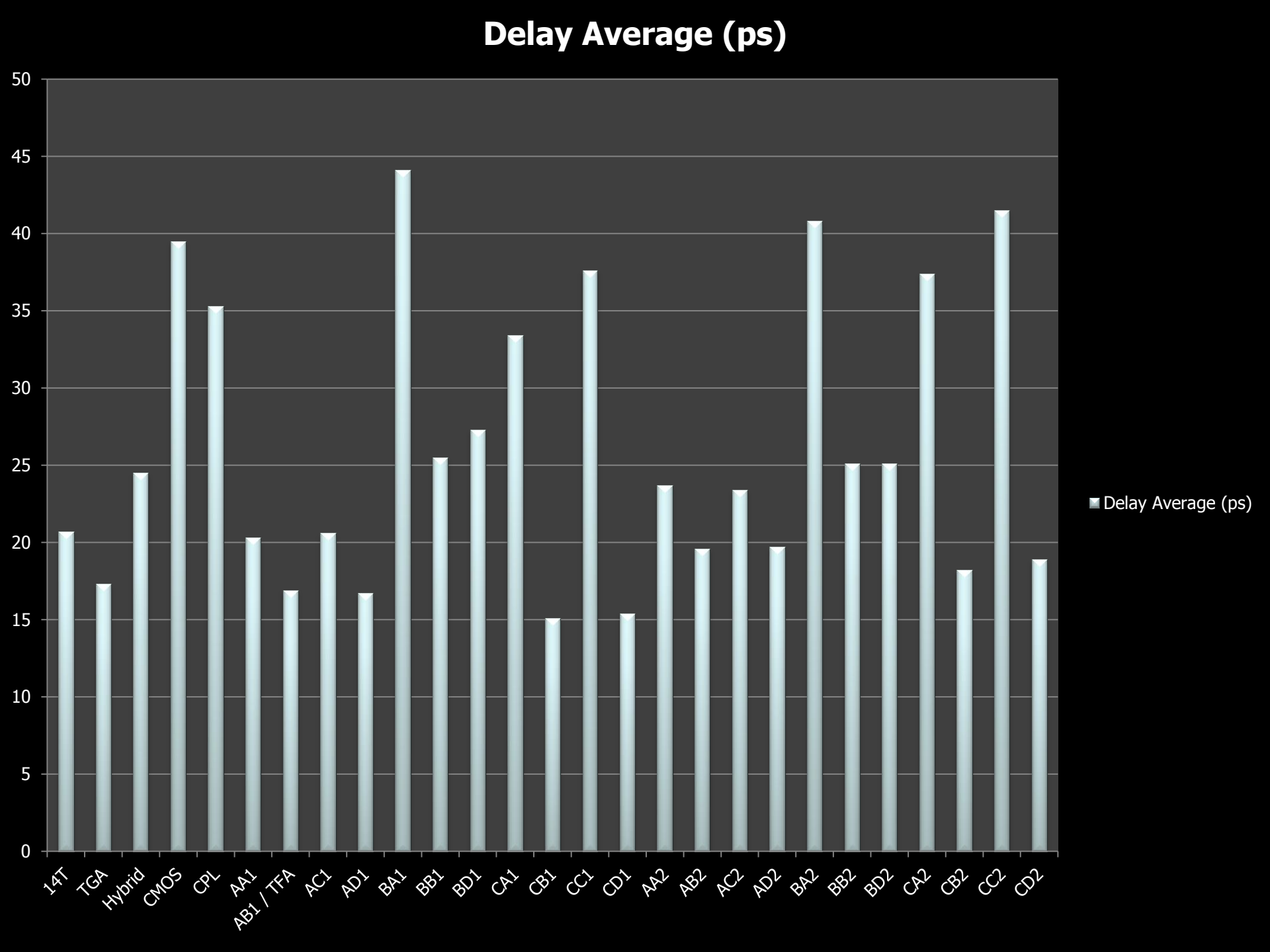
Doing all these combinations is possible to generate 24 different adders, which are named according to the initials of the blocks.

For example:

‘A’ of block1 + ‘C’ of block2 + ‘1’ of block3 = ‘AC1’

Results

Delay Average


Delay Average (ps)
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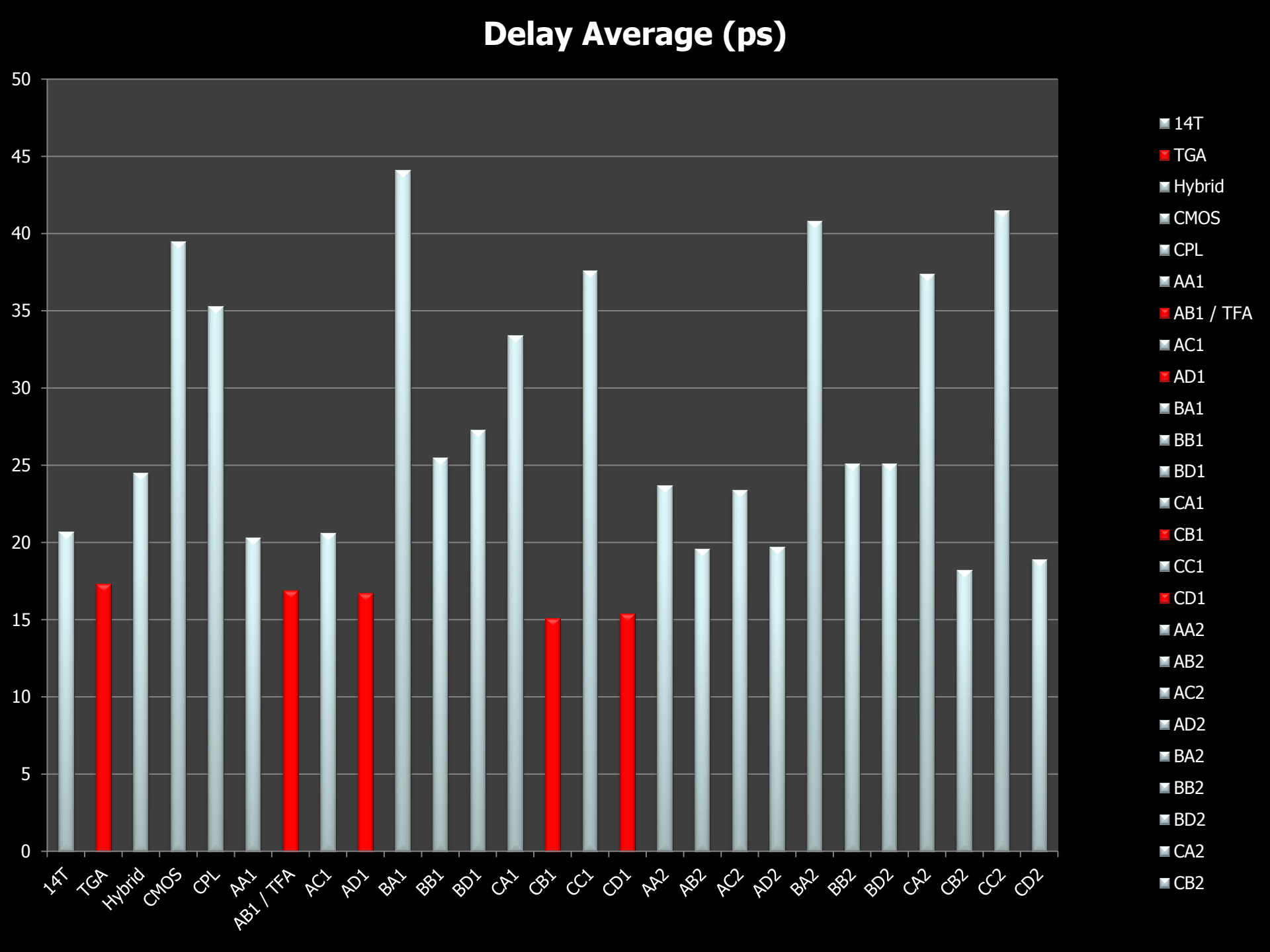
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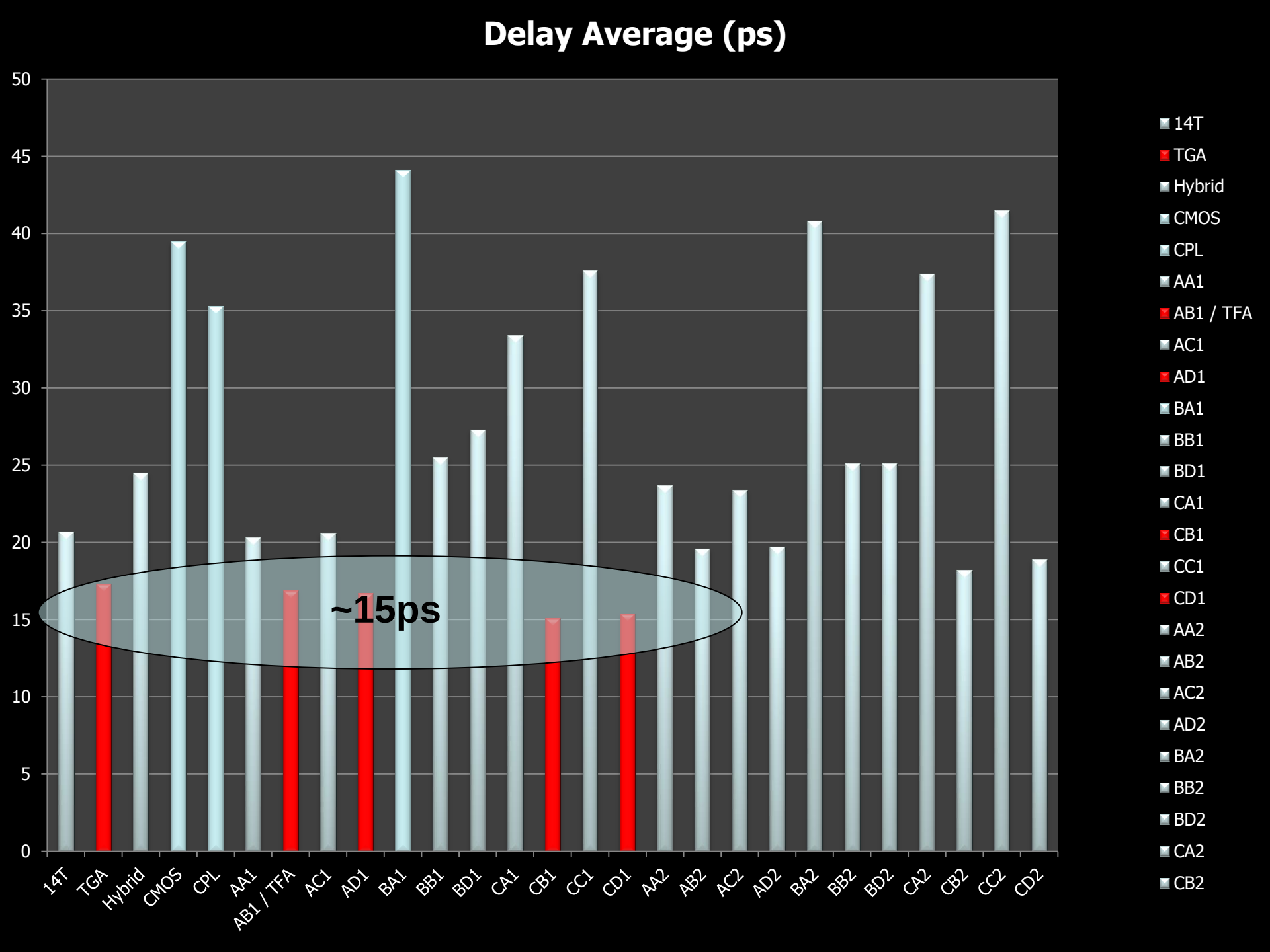
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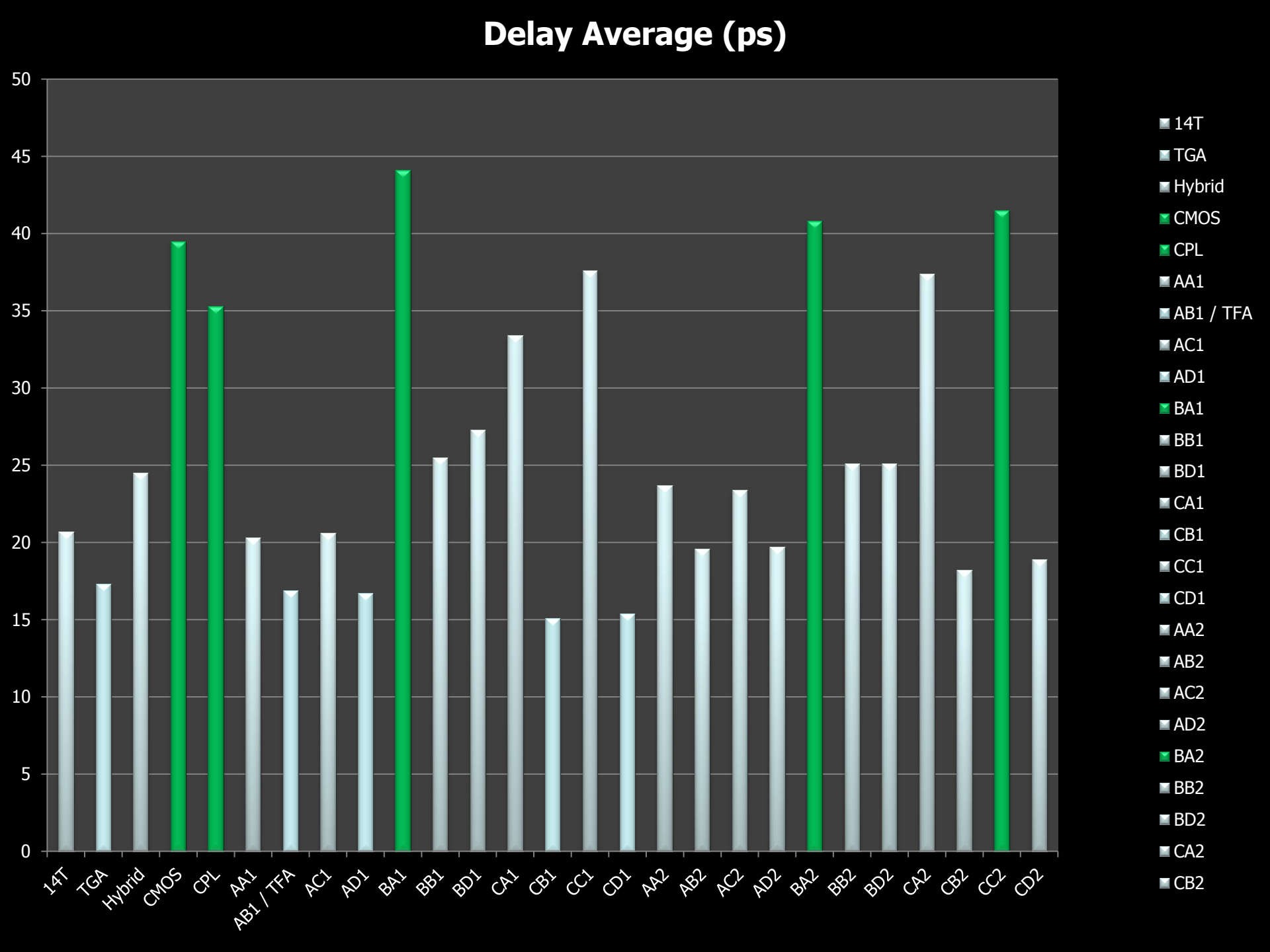
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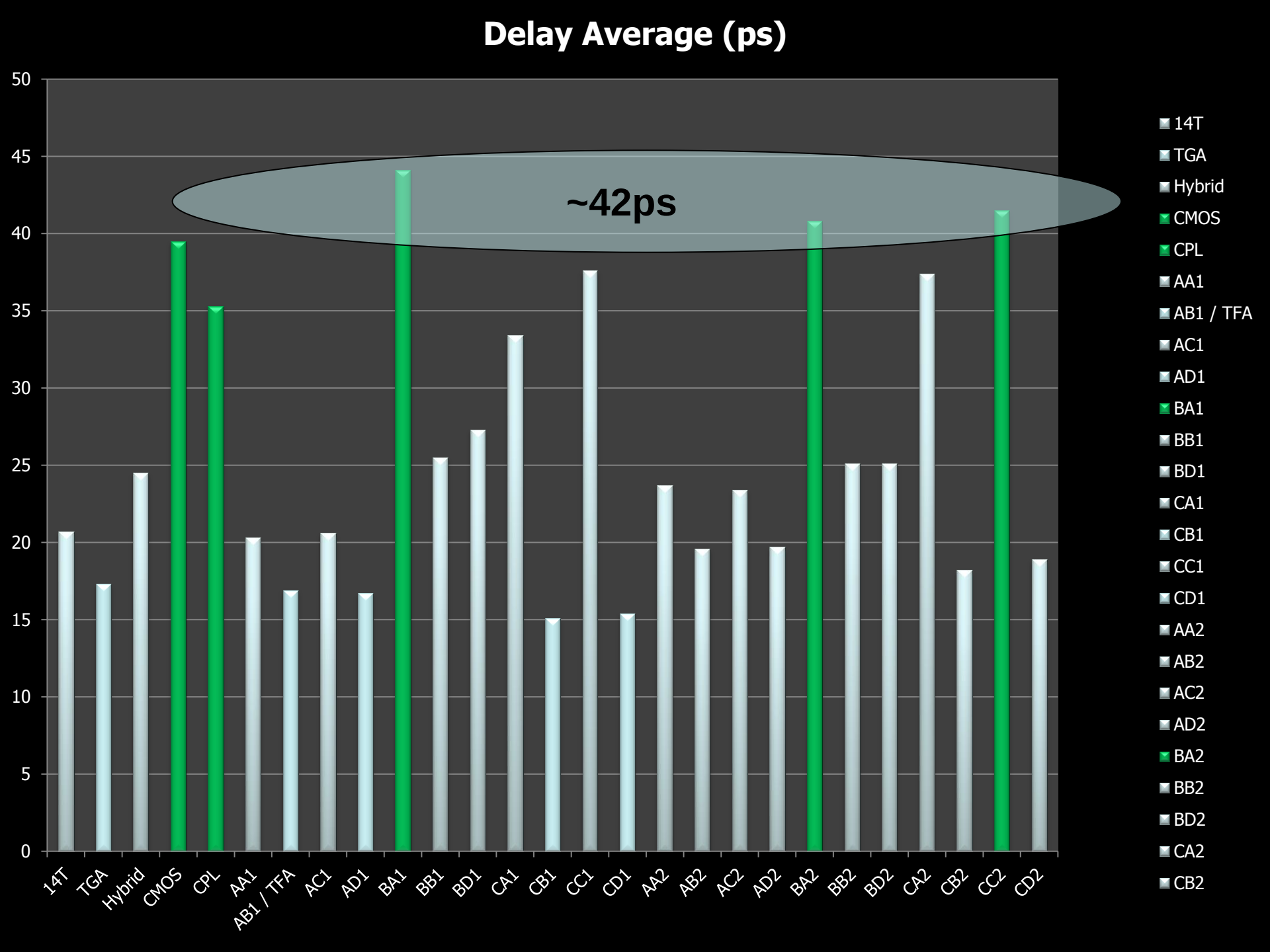
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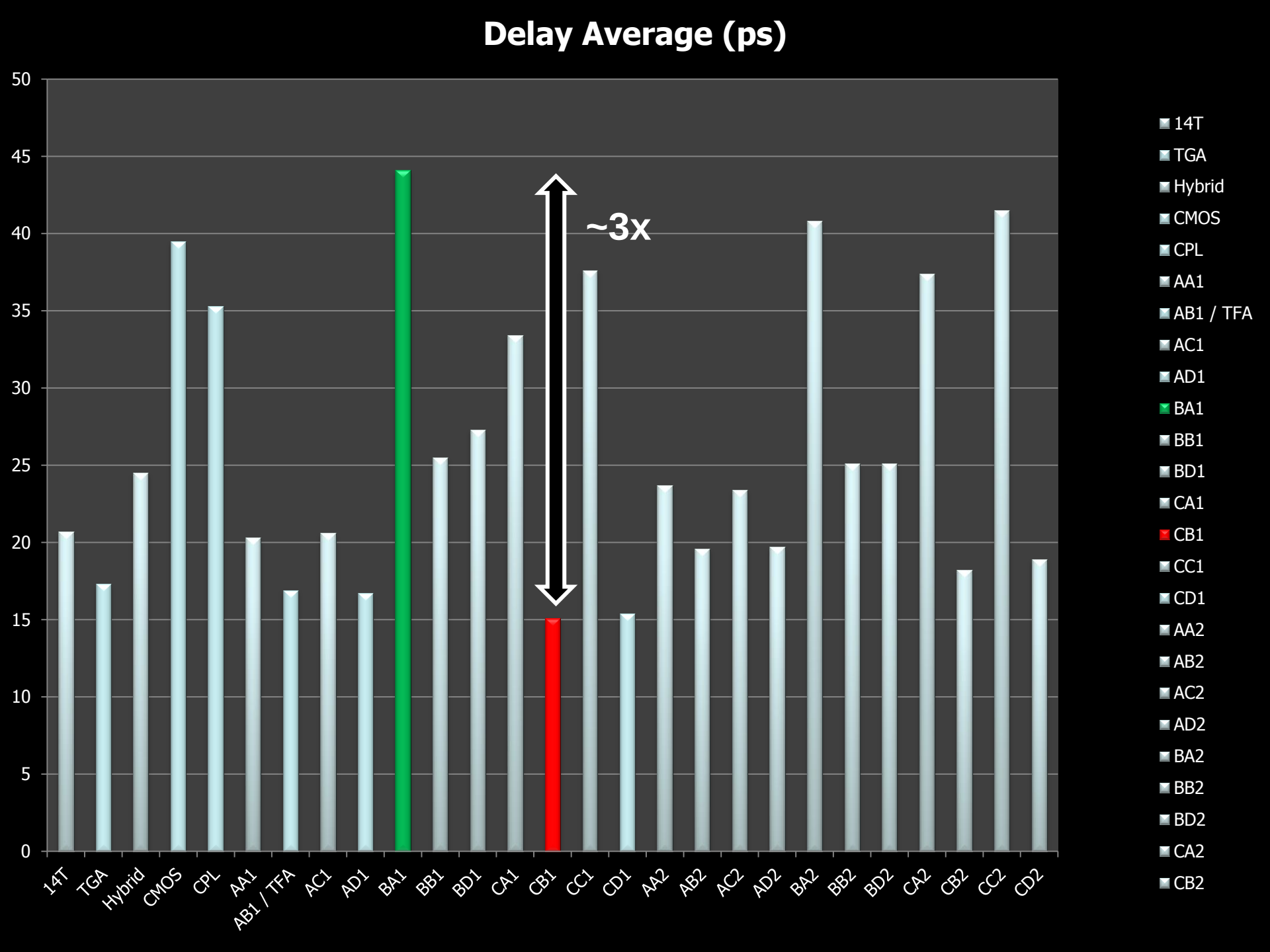
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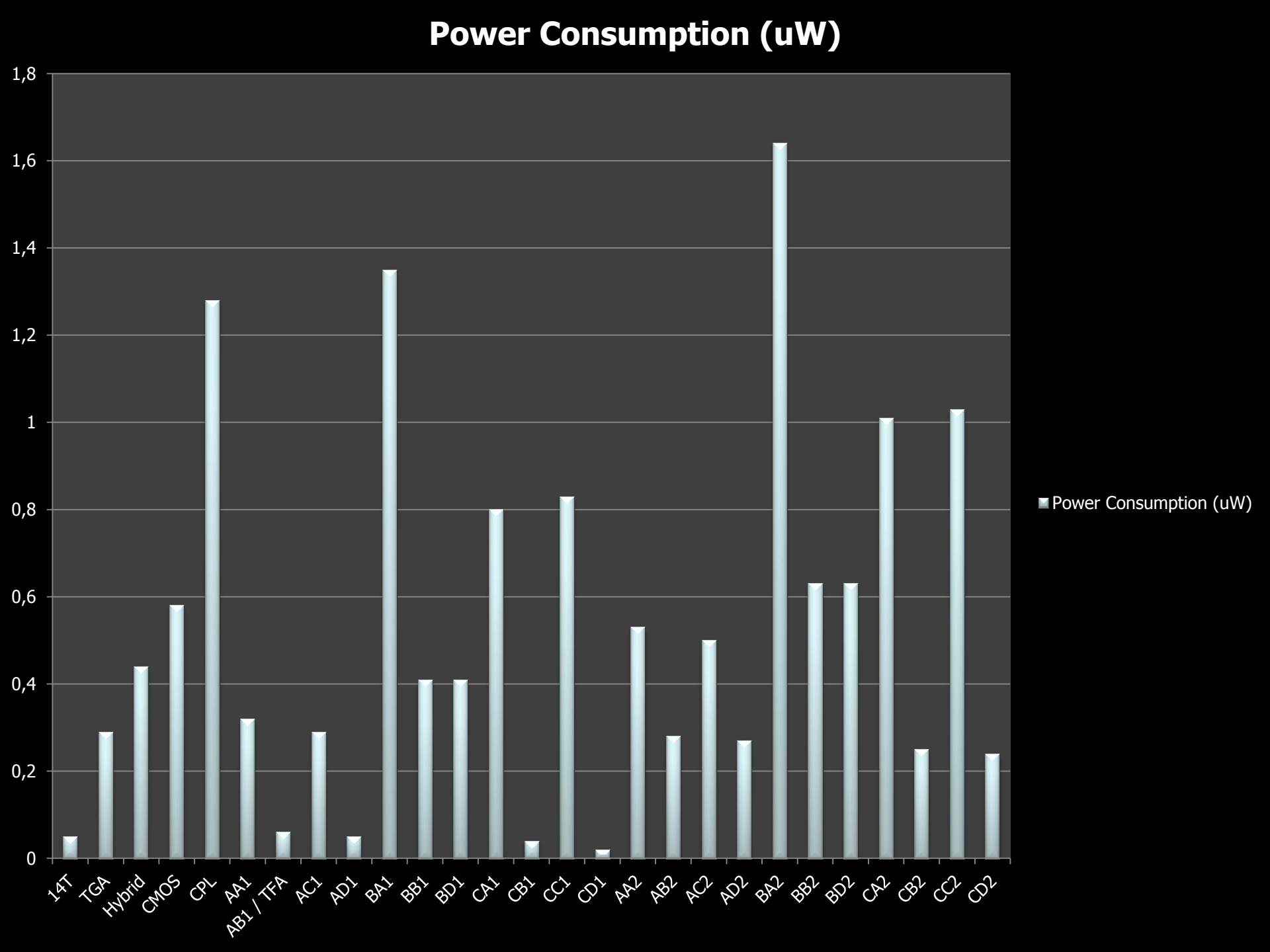
Power Consumption


Power Consumption (uW)
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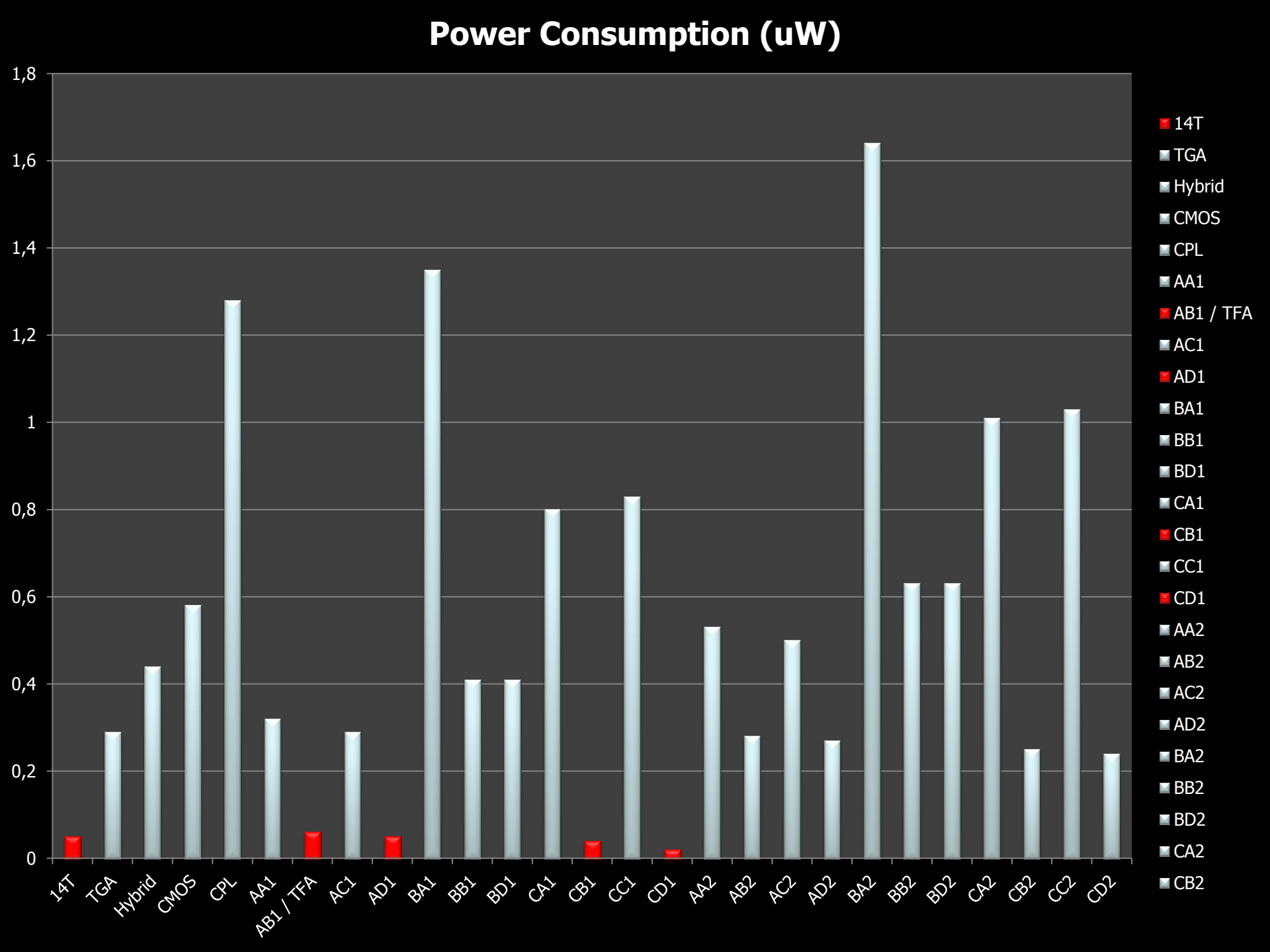
Power Consumption (uW)


Power Consumption (uW)
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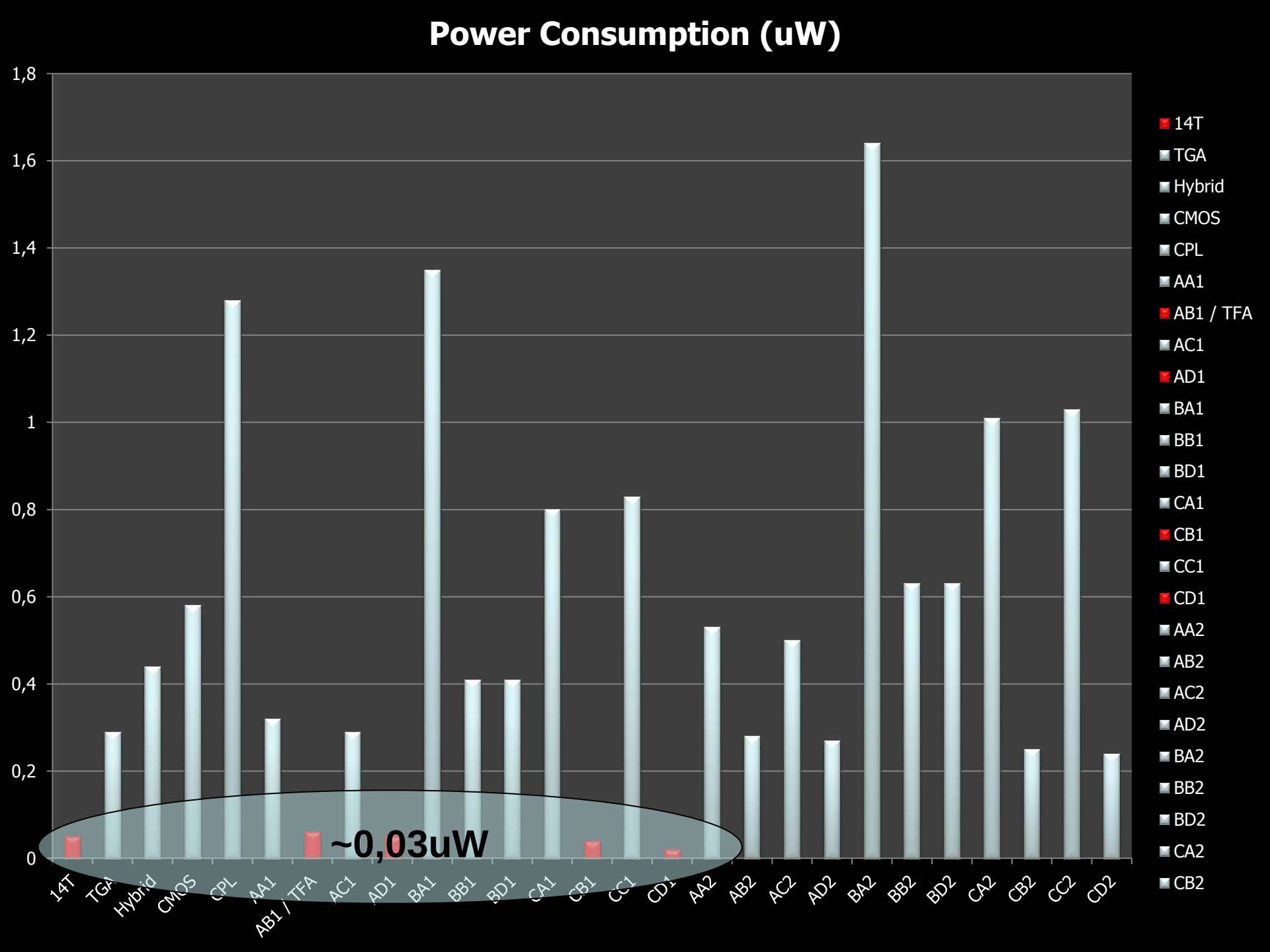
Power Consumption (uW)
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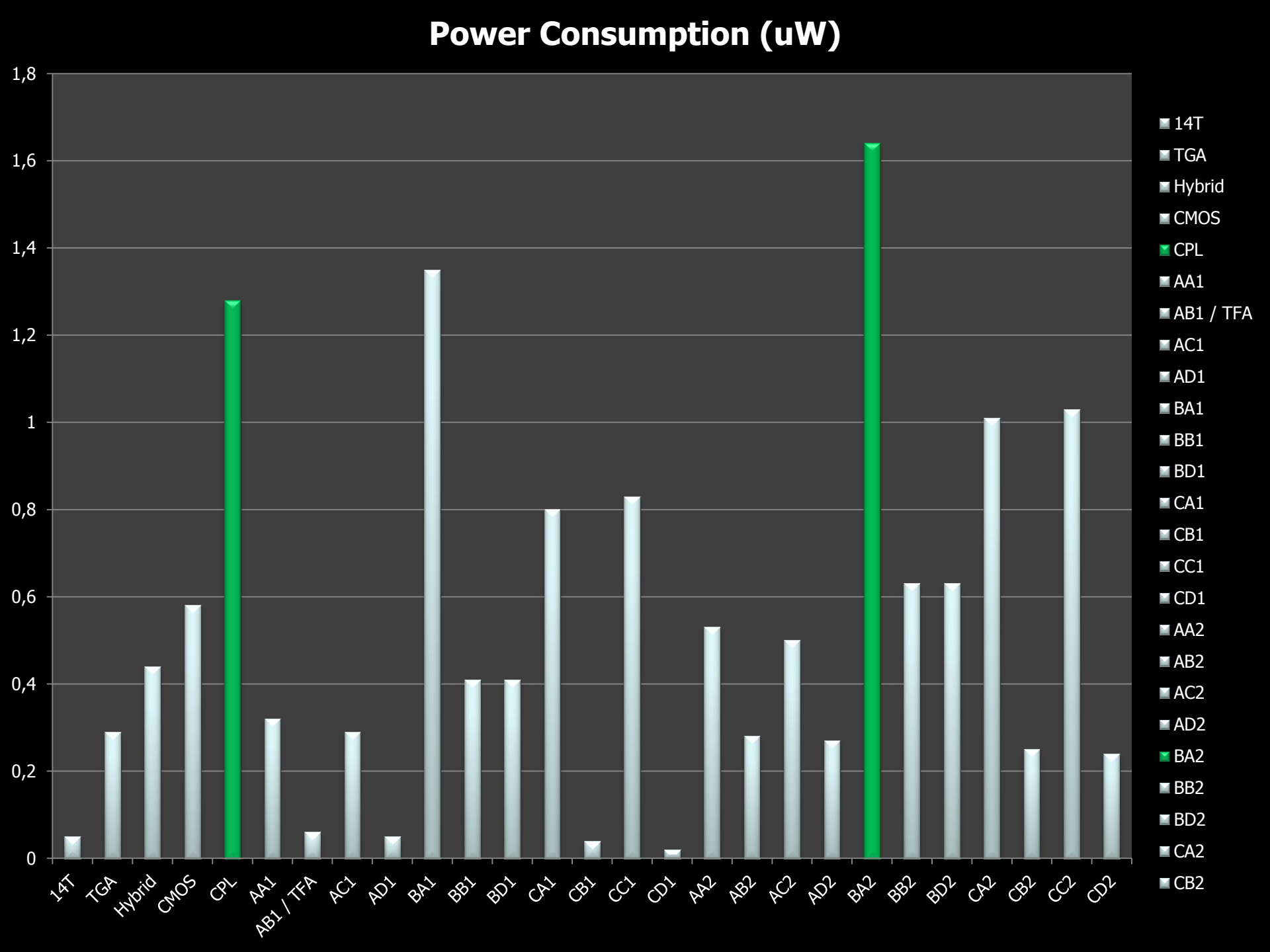
Power Consumption (uW)
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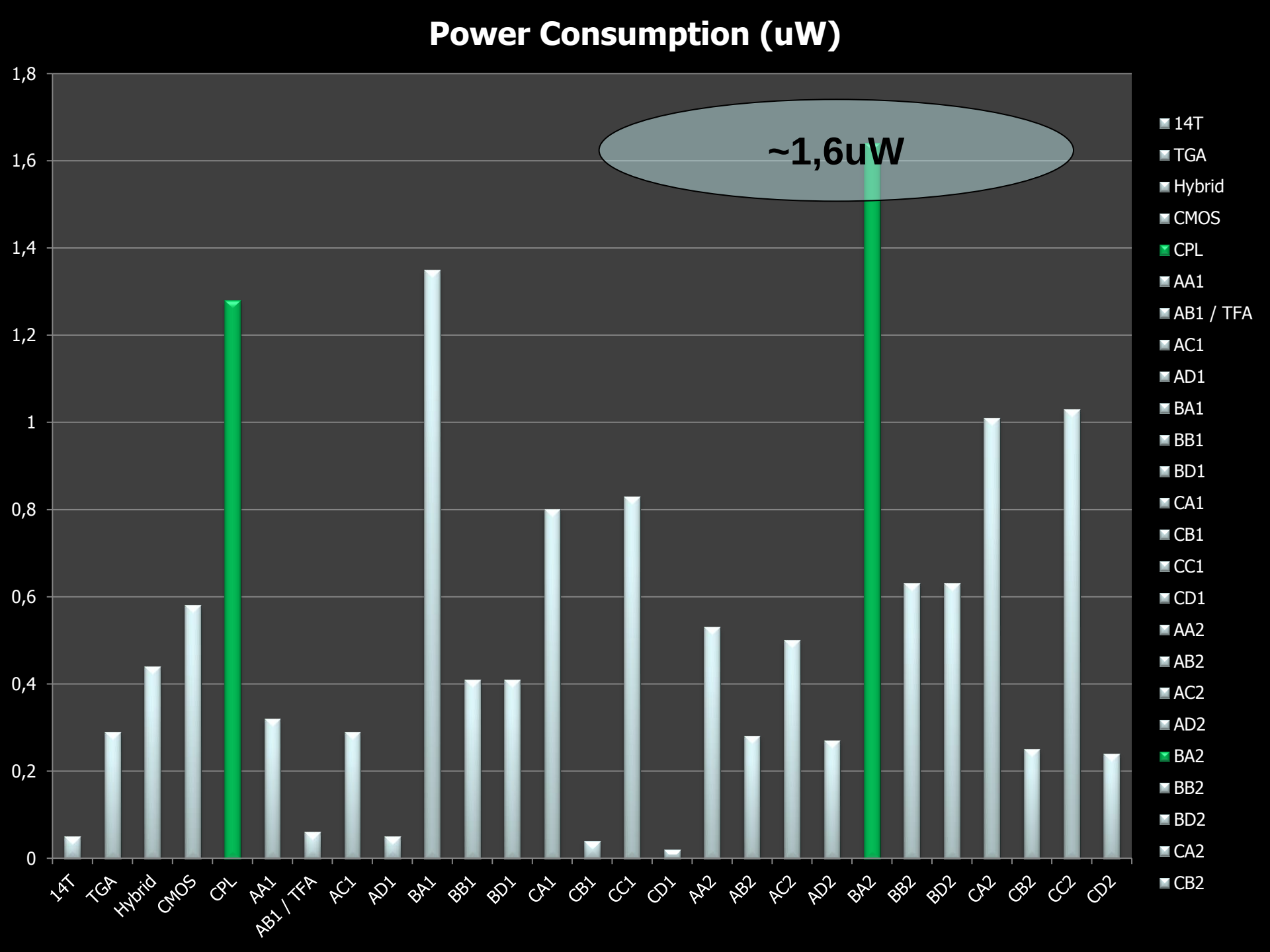
Power Consumption (uW)
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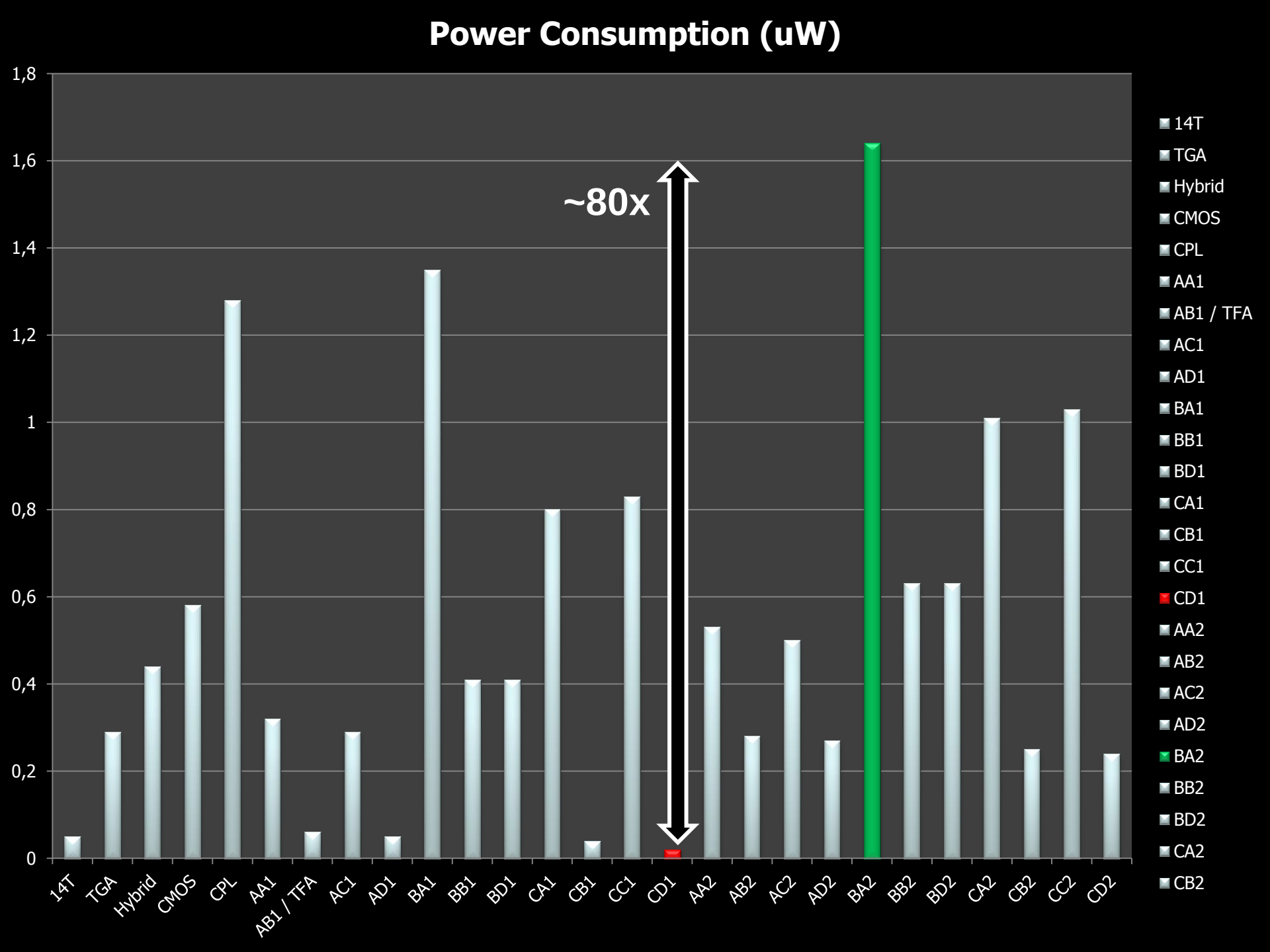
Power Consumption (uW)
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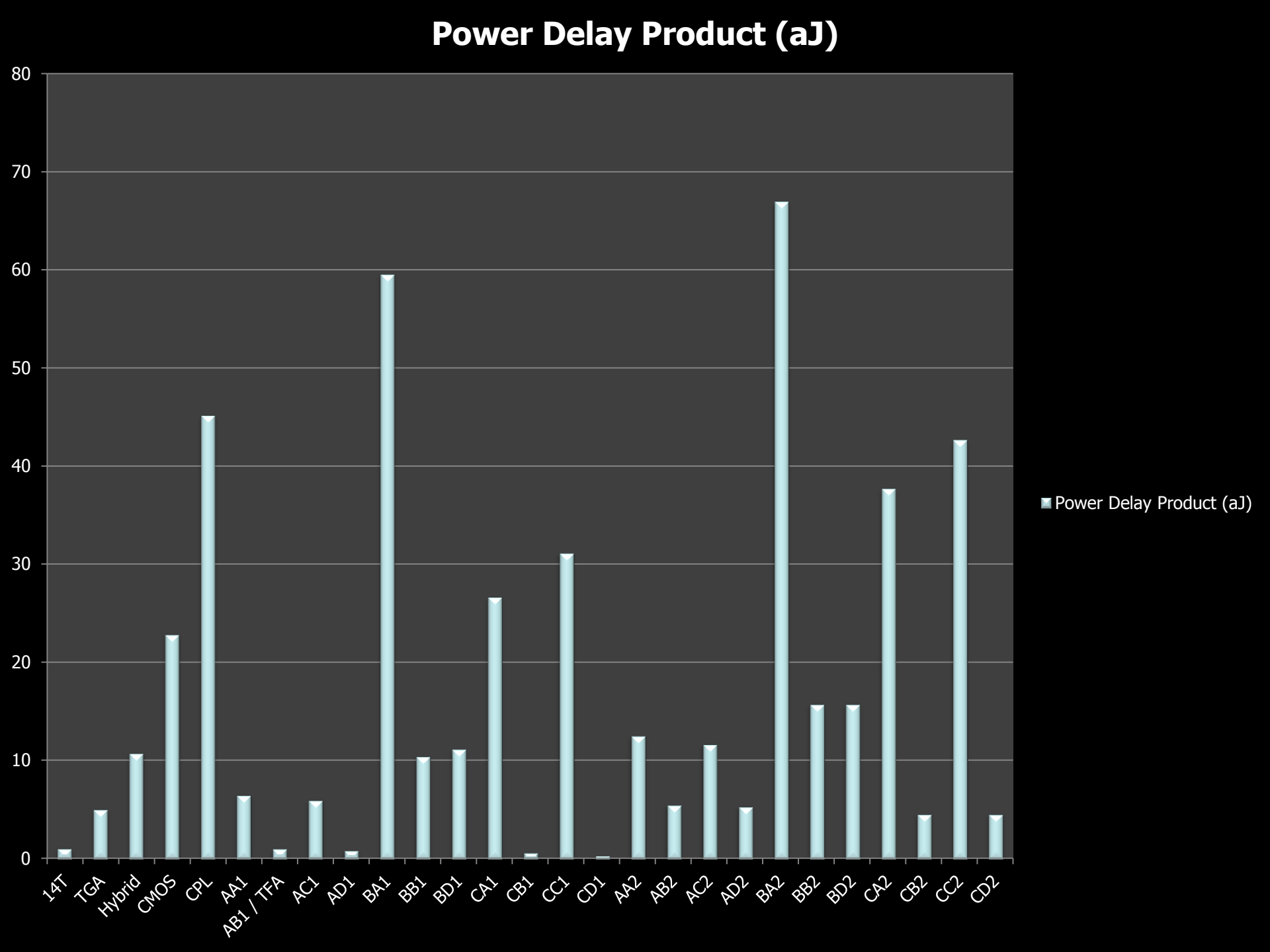
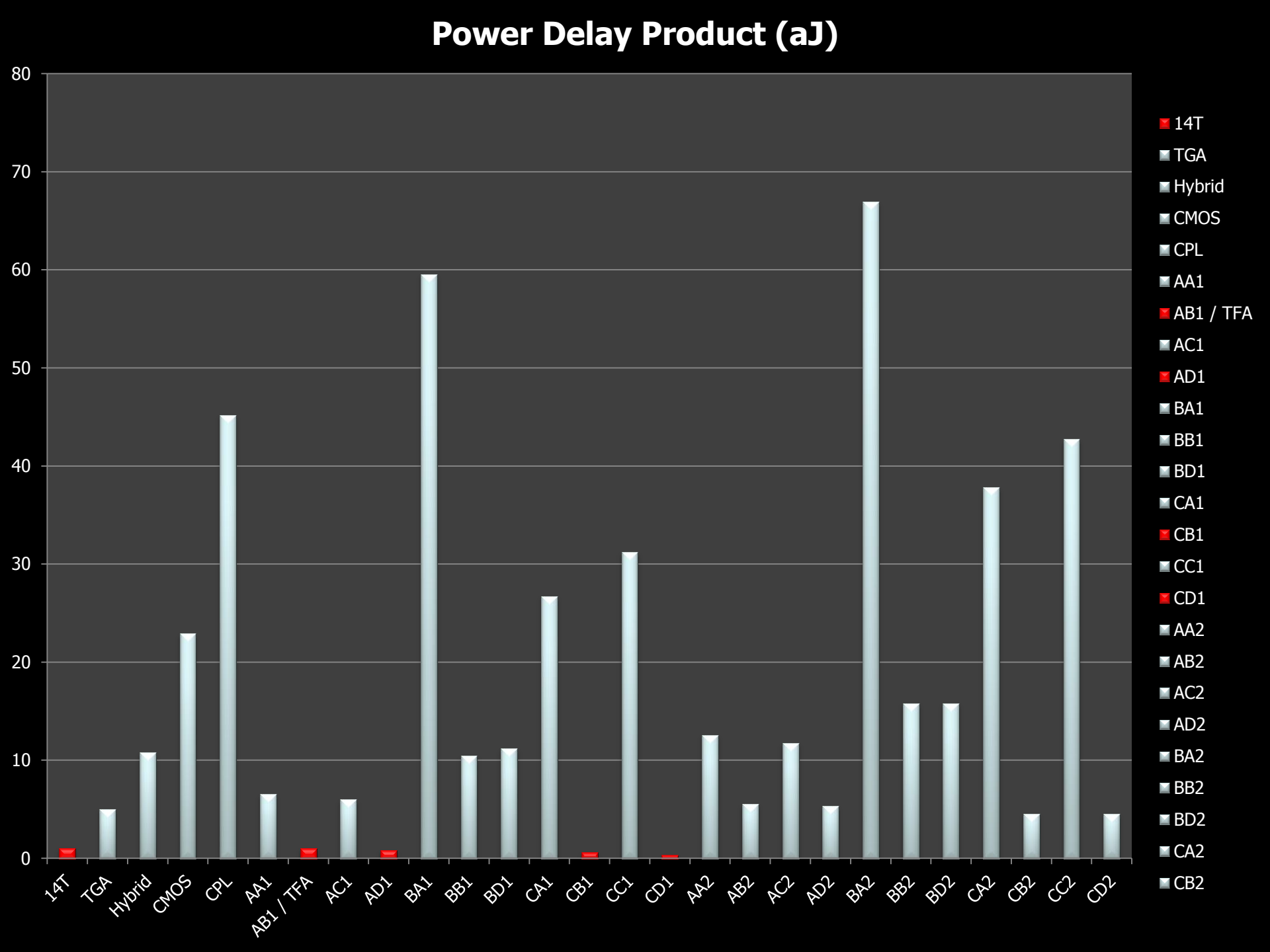
CD2

Power Delay Product


Power Delay Product (aJ)
80
70
60
50
40
30
20
10
0
14T
TGA
Hybrid
CMOS
CPL
AA1
AB1 / TFA
AC1
AD1
BA1
BB1
BD1
CA1
CB1
CC1
CD1
AA2
AB2
AC2
AD2
BA2
BB2
BD2
CA2
CB2
CC2
CD2
Power Delay Product (aJ)


Power Delay Product (aJ)
80
70
60
50
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30
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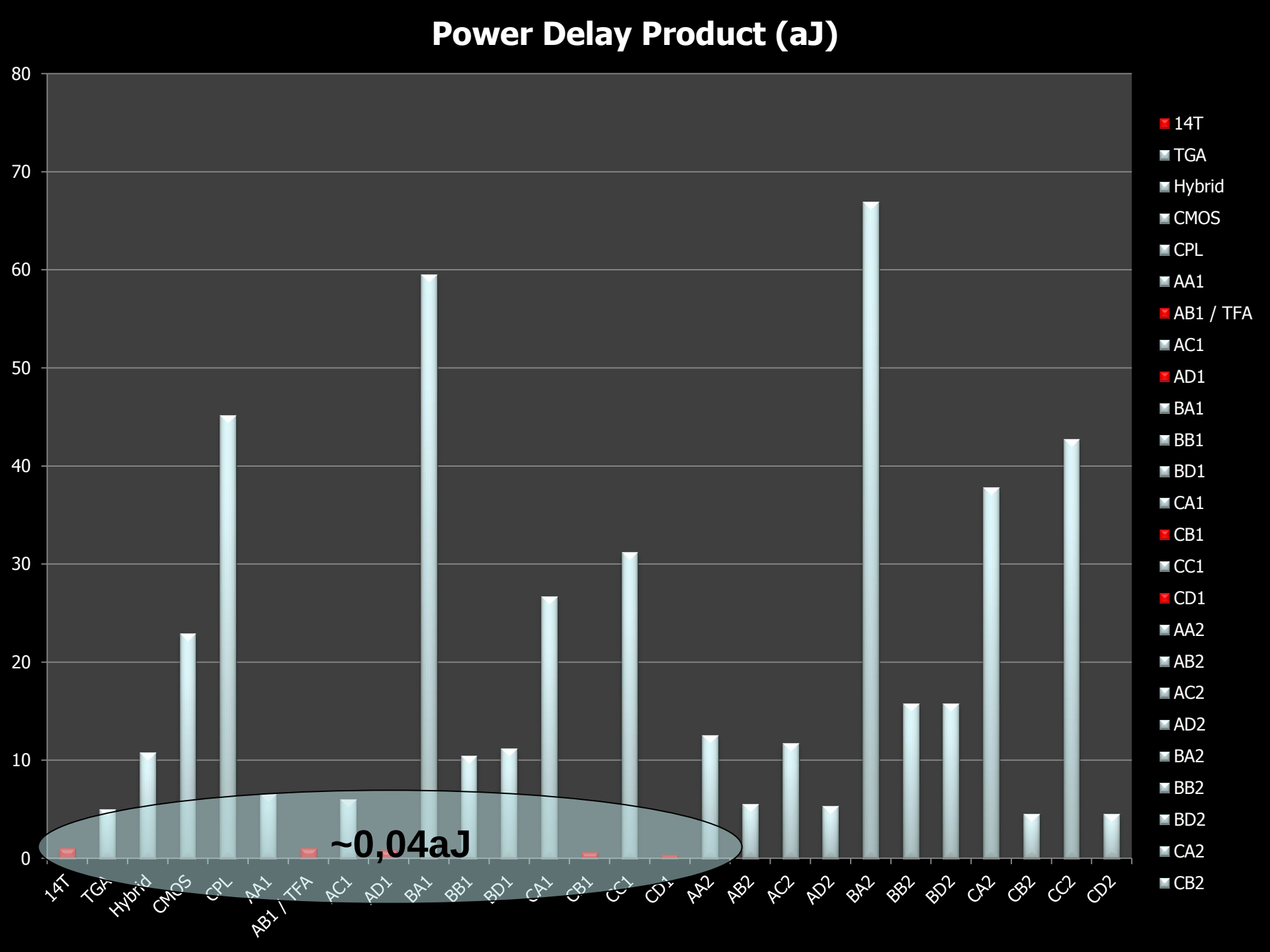
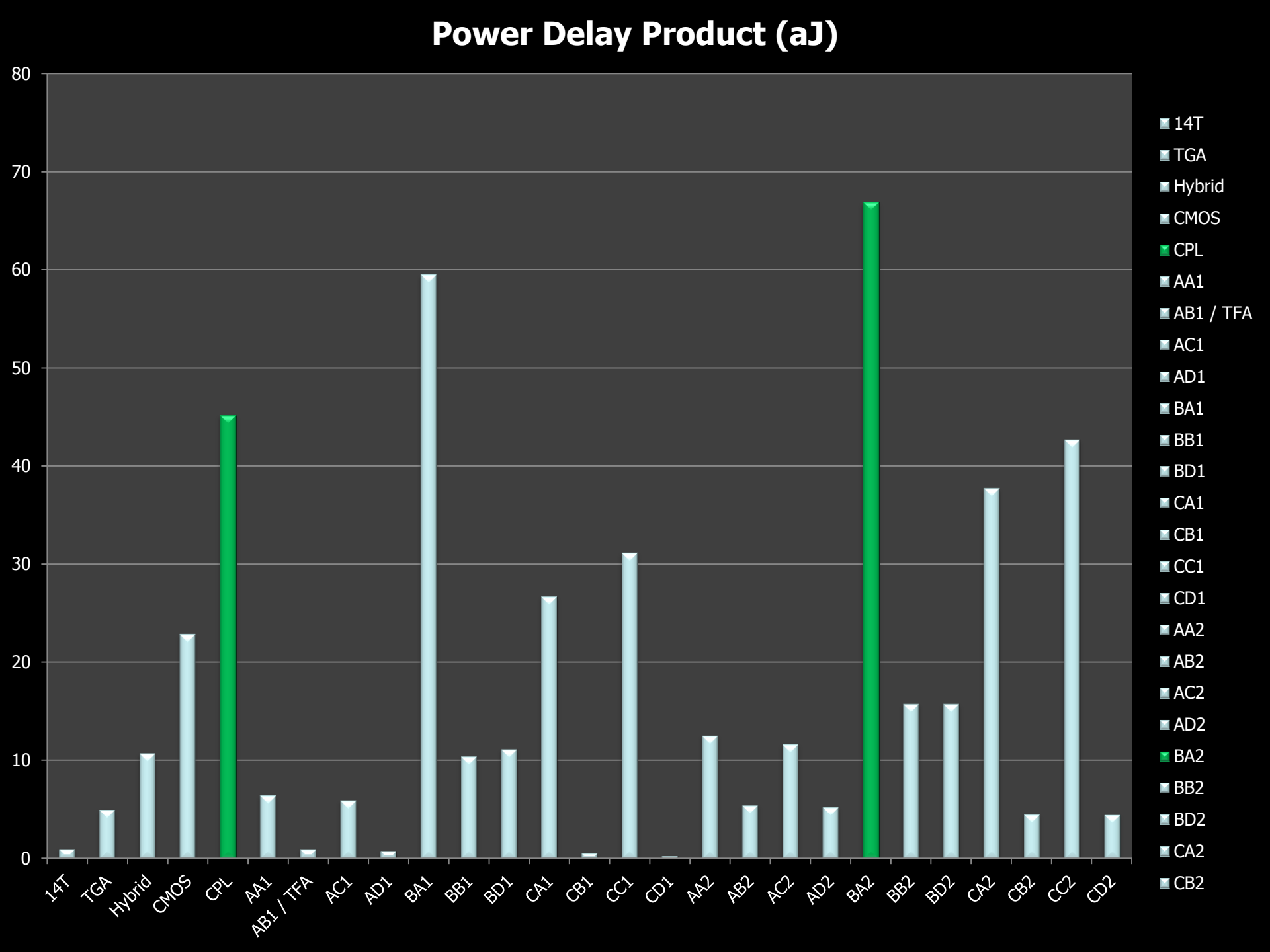
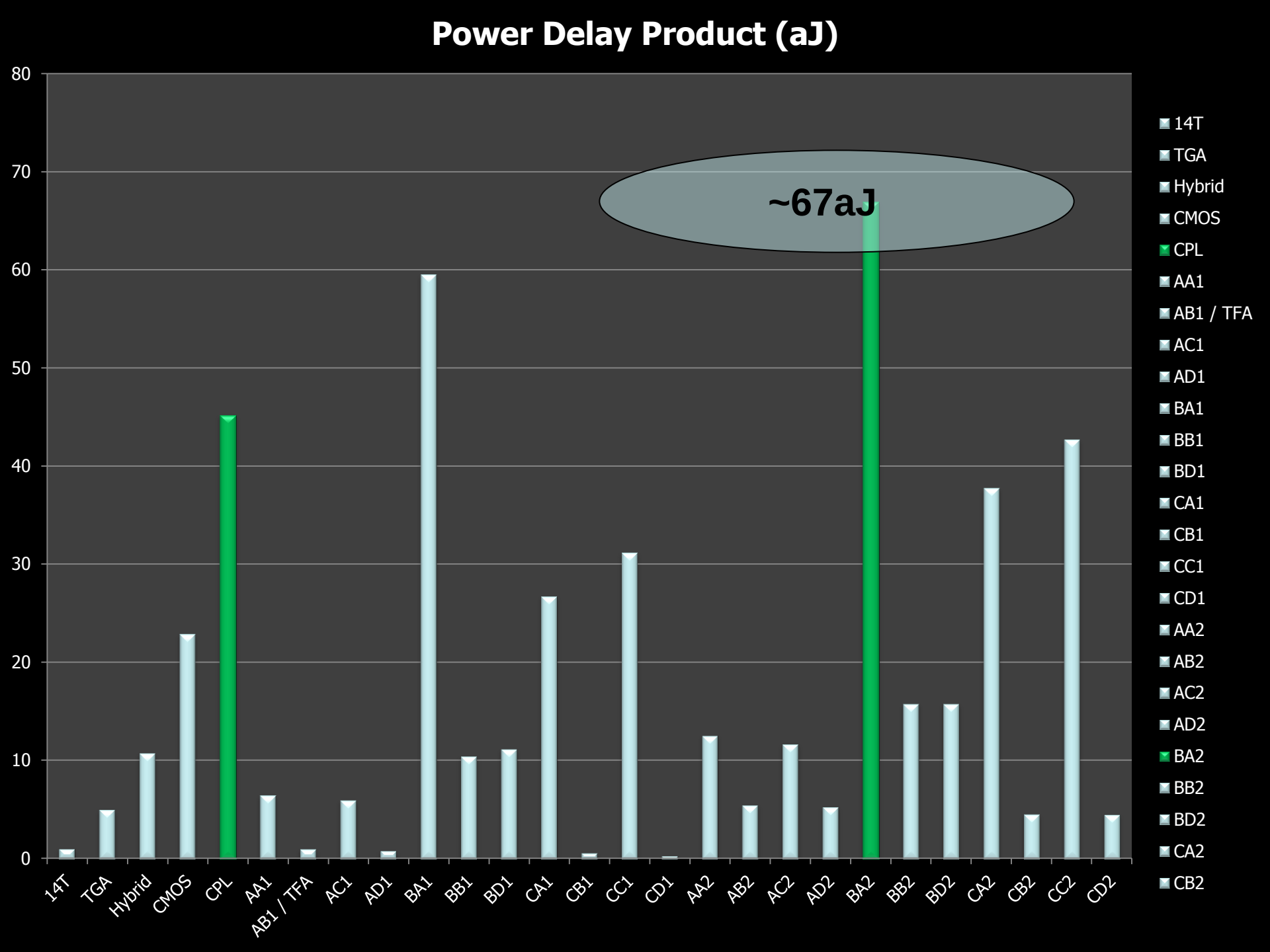
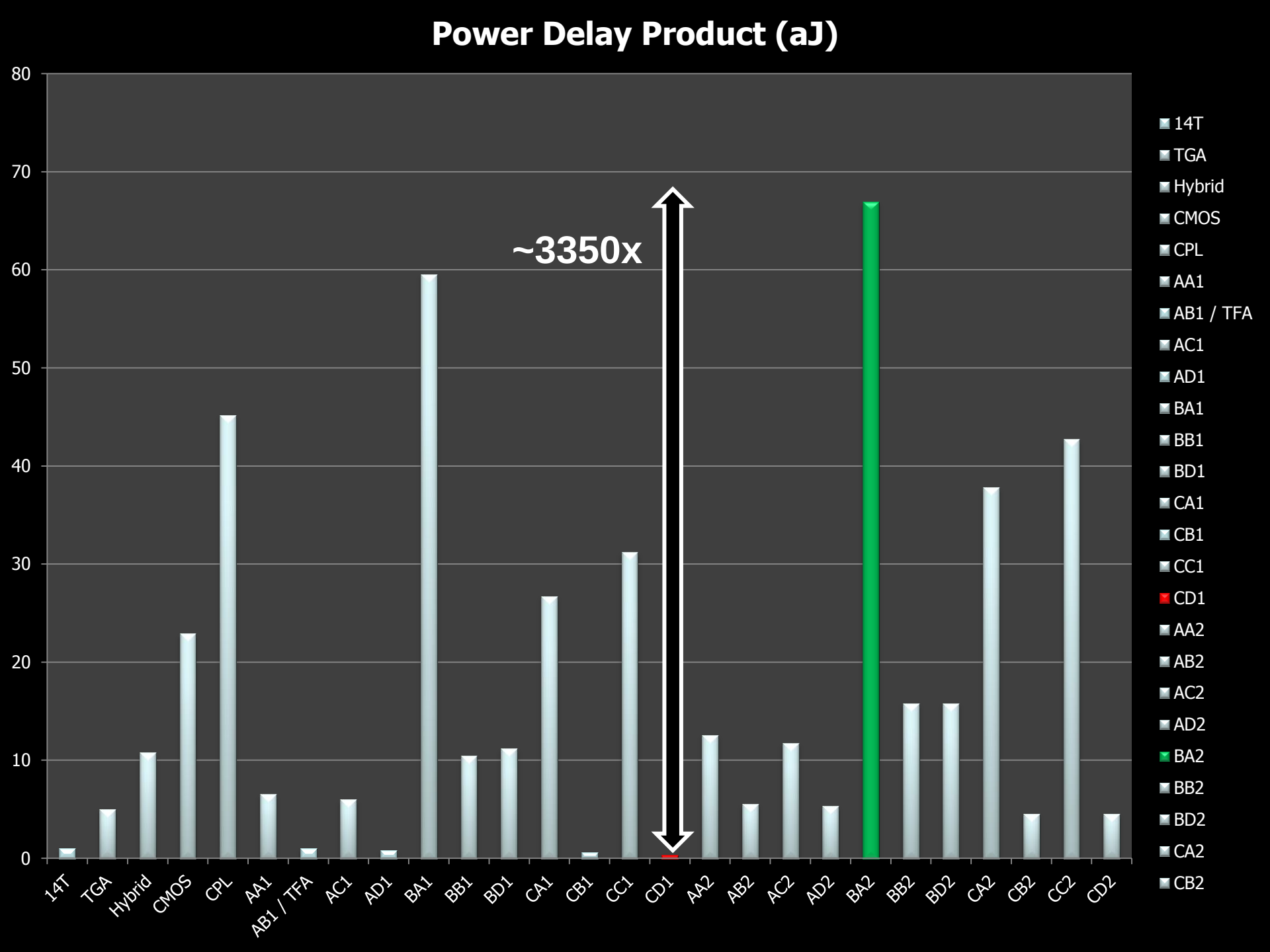
10
0
14T
TGA
Hybrid
CMOS
CPL
AA1
AB1 / TFA
AC1
AD1
BA1
BB1
BD1
CA1
CB1
CC1
CD1
AA2
AB2
AC2
AD2
BA2
BB2
BD2
CA2
CB2
CC2
CD2
14T
TGA
Hybrid
CMOS
CPL
AA1
AB1 / TFA
AC1
AD1
BA1
BB1
BD1
CA1
CB1
CC1
CD1
AA2
AB2
AC2
AD2
BA2
BB2
BD2
CA2
CB2


Power Delay Product (aJ)
80
70
60
50
40
30
20
10
0
~0,04aJ
14T
TGA
Hybrid
CMOS
CPL
AA1
AB1 / TFA
AC1
AD1
BA1
BB1
BD1
CA1
CB1
CC1
CD1
AA2
AB2
AC2
AD2
BA2
BB2
BD2
CA2
CB2
CC2
CD2


Power Delay Product (aJ)
80
70
60
50
40
30
20
10
0
14T
TGA
Hybrid
CMOS
CPL
AA1
AB1 / TFA
AC1
AD1
BA1
BB1
BD1
CA1
CB1
CC1
CD1
AA2
AB2
AC2
AD2
BA2
BB2
BD2
CA2
CB2
CC2
CD2
14T
TGA
Hybrid
CMOS
CPL
AA1
AB1 / TFA
AC1
AD1
BA1
BB1
BD1
CA1
CB1
CC1
CD1
AA2
AB2
AC2
AD2
BA2
BB2
BD2
CA2
CB2


Power Delay Product (aJ)
~67aJ
80
70
60
50
40
30
20
10
0
14T
TGA
Hybrid
CMOS
CPL
AA1
AB1 / TFA
AC1
AD1
BA1
BB1
BD1
CA1
CB1
CC1
CD1
AA2
AB2
AC2
AD2
BA2
BB2
BD2
CA2
CB2
CC2
CD2


Power Delay Product (aJ)
~3350x
80
70
60
50
40
30
20
10
0
14T
TGA
Hybrid
CMOS
CPL
AA1
AB1 / TFA
AC1
AD1
BA1
BB1
BD1
CA1
CB1
CC1
CD1
AA2
AB2
AC2
AD2
BA2
BB2
BD2
CA2
CB2
CC2
CD2

Conclusions

The results show that the traditional approaches (CMOS and CPL) present worst performance when compared to composing solutions.

- The highlights were the following architectures:

  - Average **delay**: CB1 and CD1

  - **Power** consumptions: CD1

  - Power delay product (**PDP**): CB1, CD1 and AD1

Future Works

- To provide a more complete analysis, next steps include:
  - Perform transistor sizing
  - Explore other circuits in 3 blocks strategy
  - Compute static power
  - Evaluate area (layout)

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FURG

Performance and Power Consumption Analysis of Full Adders Designed in 32nm Technology

Thanks to all!