logiCS logic circuit synthesis labs

UFRGS

EXPLICIT LOGICAL EFFORT FORMULATION FOR MINIMUM ACTIVE AREA UNDER DELAY CONSTRAINTS

Caio G. P. Alegretti, Vinícius Dal Bem, Renato P. Ribas, André I. Reis

Institute of Informatics, UFRGS, Porto Alegre, RS

{cgpalegretti, vdbem, rpribas, andreis}@inf.ufrgs.br

SYNAPTIC

CNPq Conselho Nacional de Desenvolvimento Científico e Tecnológico 60 ANOS

CAPES

FAPERGS

SIZING

- Choosing the sizes of logic gates
  - Respecting design constraints
  - Minimizing other costs
- Based on a delay model

OBJECTIVE

- minimize active area (power)

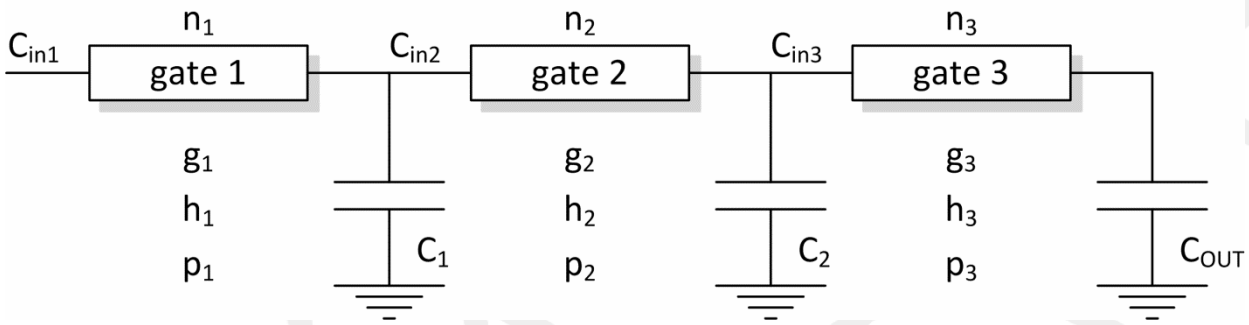
LOGICAL EFFORT DELAY MODEL

- Gain-based delay model

$$d_{abs} = \tau(gh + p)$$

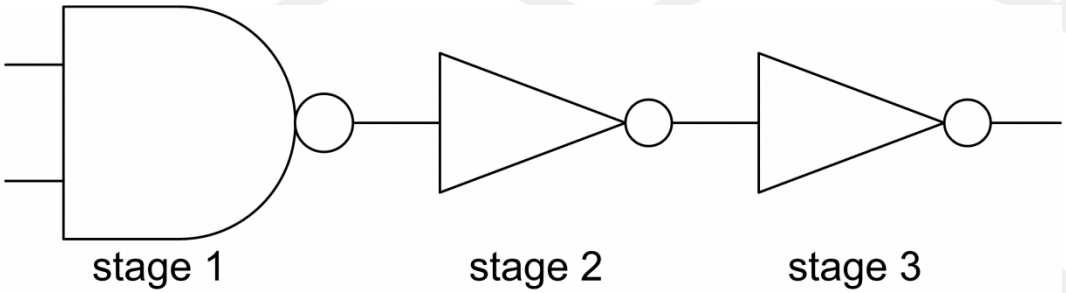
  - d_{abs} : absolute delay
  - τ : delay of an inverter driving an identical inverter with no parasitics
  - g : logical effort of the gate
  - h : electrical effort
  - p : parasitic delay

PROPOSED METHOD



- Total delay of an n-stage logic path: $D = d_1 + d_2 + \ldots + d_n$
- Total active area – 3-stage logic path: $A = n_1 C_{in1} + n_2 C_{in2} + n_3 C_{in3}$
- dA / dC_{in1} ; dA / dC_{in2} ; dA / dC_{in3}
- one-variable equation

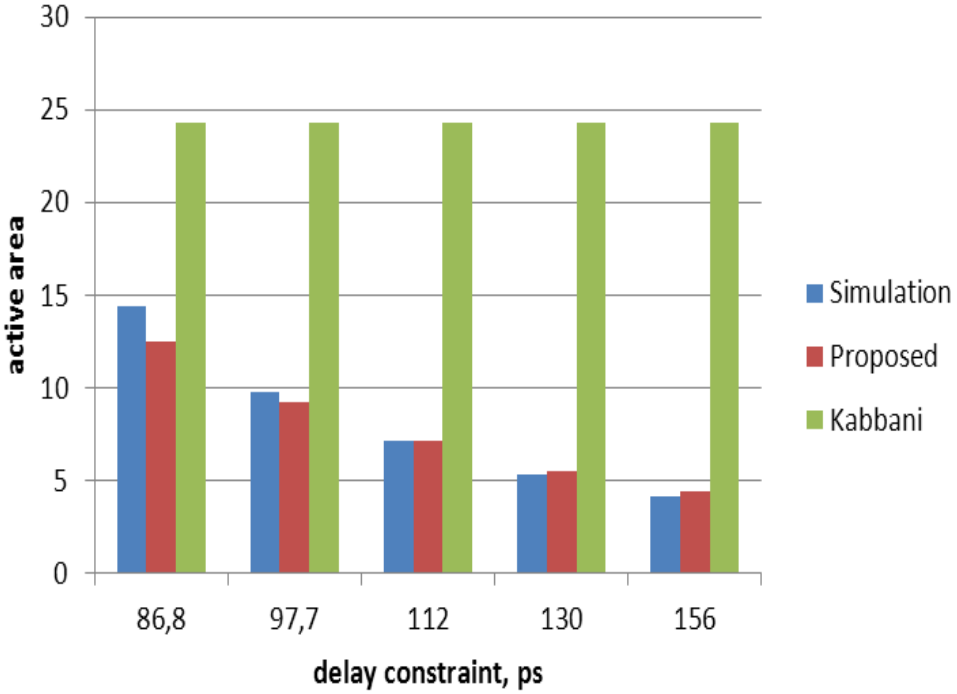
EXAMPLE: NAND – INV – INV



- Loads: X4, X16, X32, X40, X64, X100
  (input capacitance of the minimum inverter)
- Delay constraints: minimum possible delay + slacks
  (for every load)

RESULTS

Significant improvement over previous method*



Active areas for output load X100 *and 5 delay constraints.*

*Kabbani, A.: 'Logical effort based dynamic power estimation and optimization of static CMOS circuits', *Integration, the VLSI journal*, 2010, 43, pp. 279-288

CONCLUSION

- New method for sizing subcircuits
- Finds minimum active area analytically
- Solving a one-variable equation
- Maximum sizing error: 13.5%
- Maximum power error: 4.1%
- Maximum delay error: 5.6%
- Future work