A Tool to Evaluate Stuck-Open Faults in CMOS Logic Gates

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Summary

- Introduction
- Motivation
- Stuck-Open Faults
- Stuck-Open Faults in Nanometer Technologies
- Tool Development
- Conclusions and Future Works

Introduction

- The technology scaling causes several undesired effects:
  - Leakage;
  - Variability;
  - Reliability–Aging;
  - Increase the number of possible faults.

Stuck-On

Stuck-Open

Transients

Stuck-At

Bridging

Introduction

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  - Leakage;
  - Variability;
  - Reliability–Aging;
  - Increase the number of possible faults.

Stuck-On

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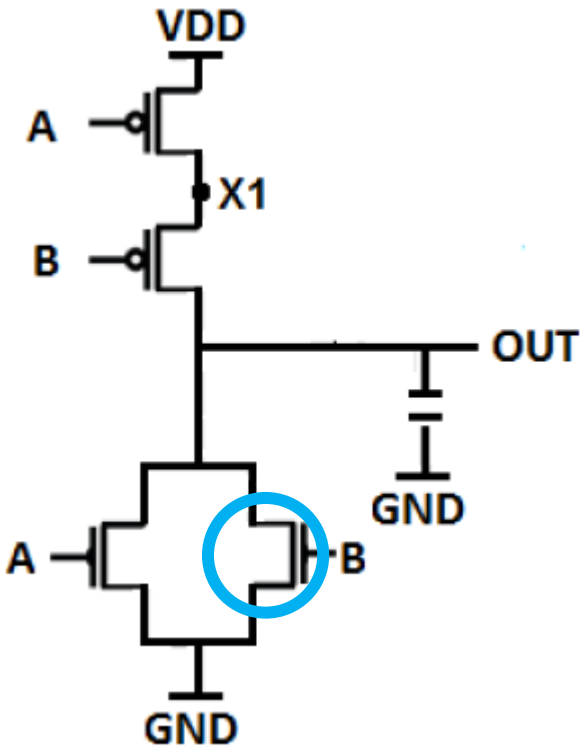
Stuck-Open Faults

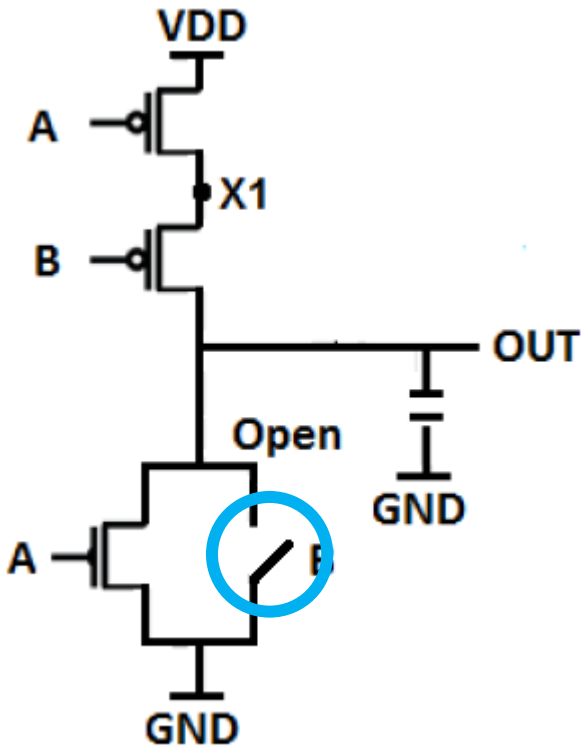
NOR2 Logic Gate



A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Stuck-Open Faults

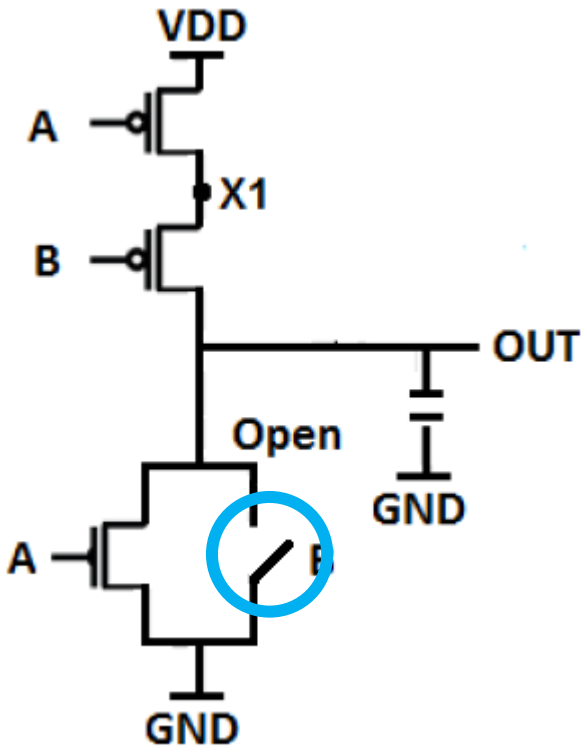
NOR2 Logic Gate



A	B	OUT
0	0	1
0	1	Z
1	0	0
1	1	0

Stuck-Open Faults

NOR2 Logic Gate



A	B	OUT
0	0	1
0	1	Z
1	0	
1	1	

The output signal floats in a high impedance state.

Stuck-Open Faults

- For example, considering the pair of vectors below:
  - AB = 00: Previous State

Expected Result: **1**	Obtained Result: **1**

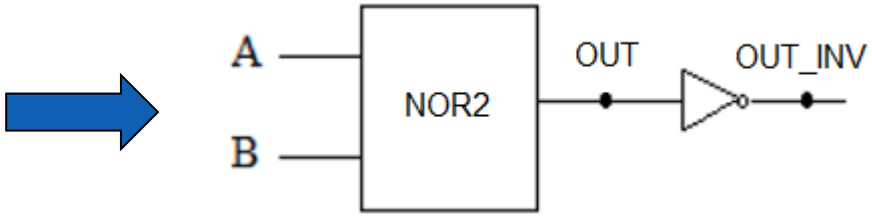
  - AB = 01: Next State

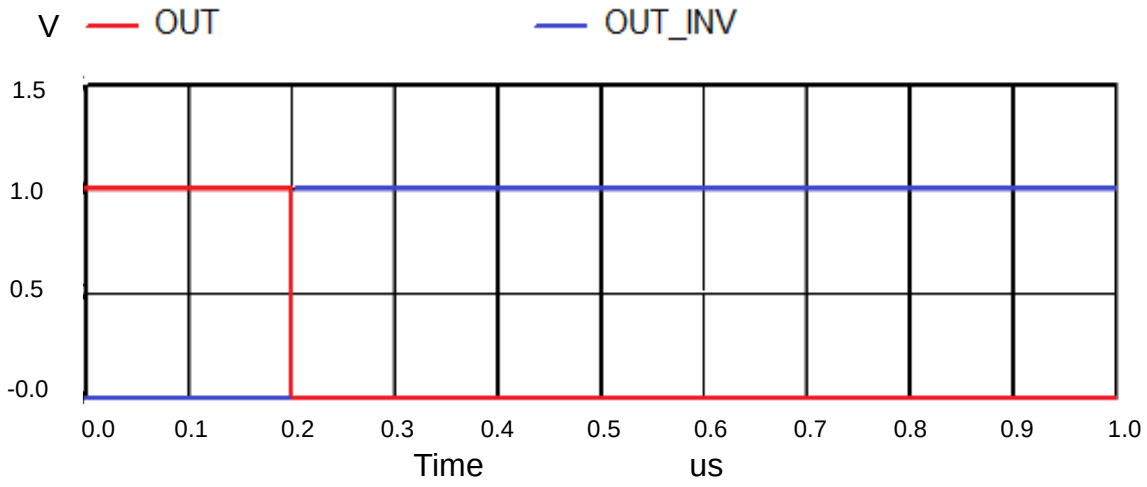
Expected Result: **0**	Obtained Result: **1**

Voltage of the previous state

Stuck-Open Faults in Nanometer Technologies

The structure used for analysis of logic gates in presence of faults.





Expected result with test application of technology of 45nm .

Stuck-Open Faults in Nanometer Technologies

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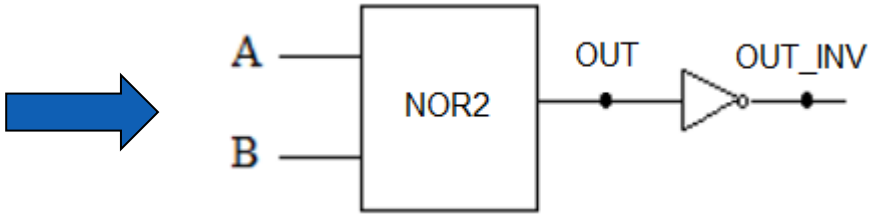

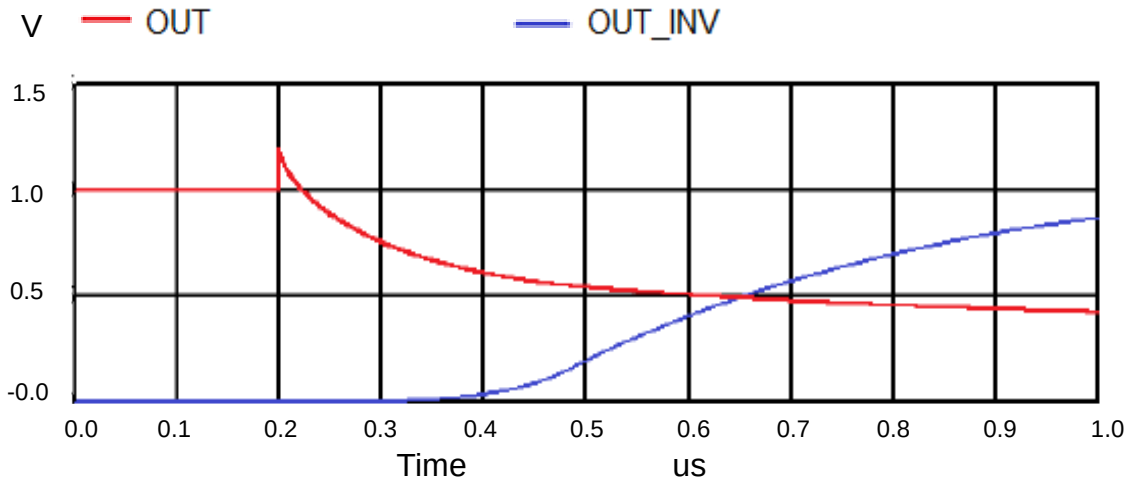

Obtained result with SOF in technologies of 45nm.

Stuck-Open Faults in Nanometer Technologies

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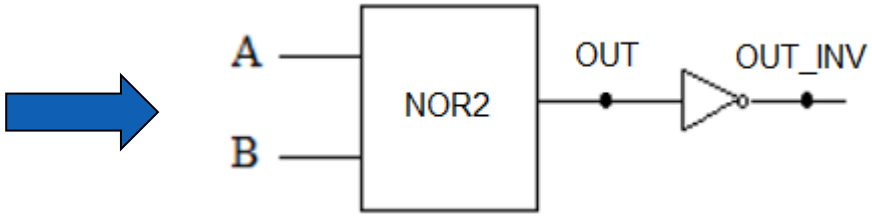
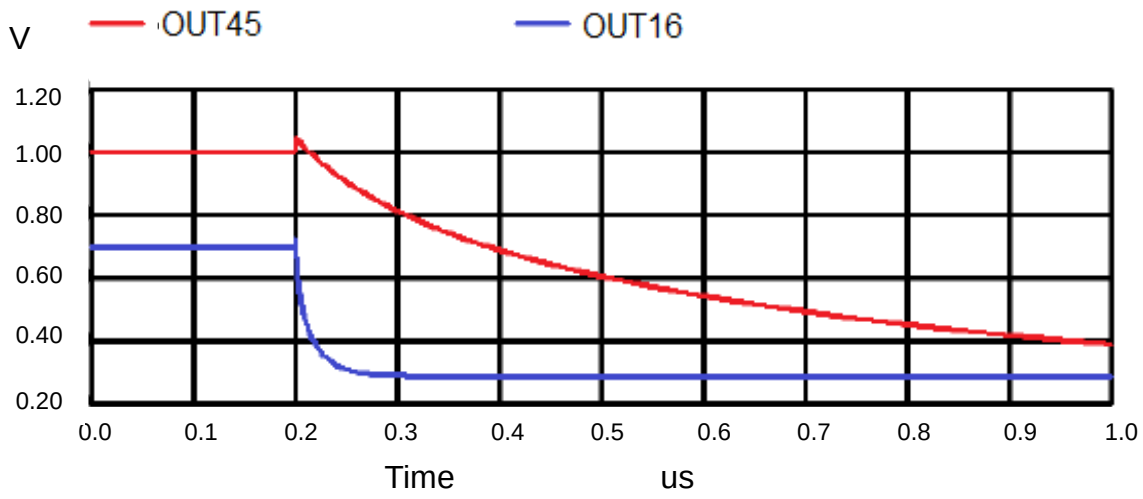
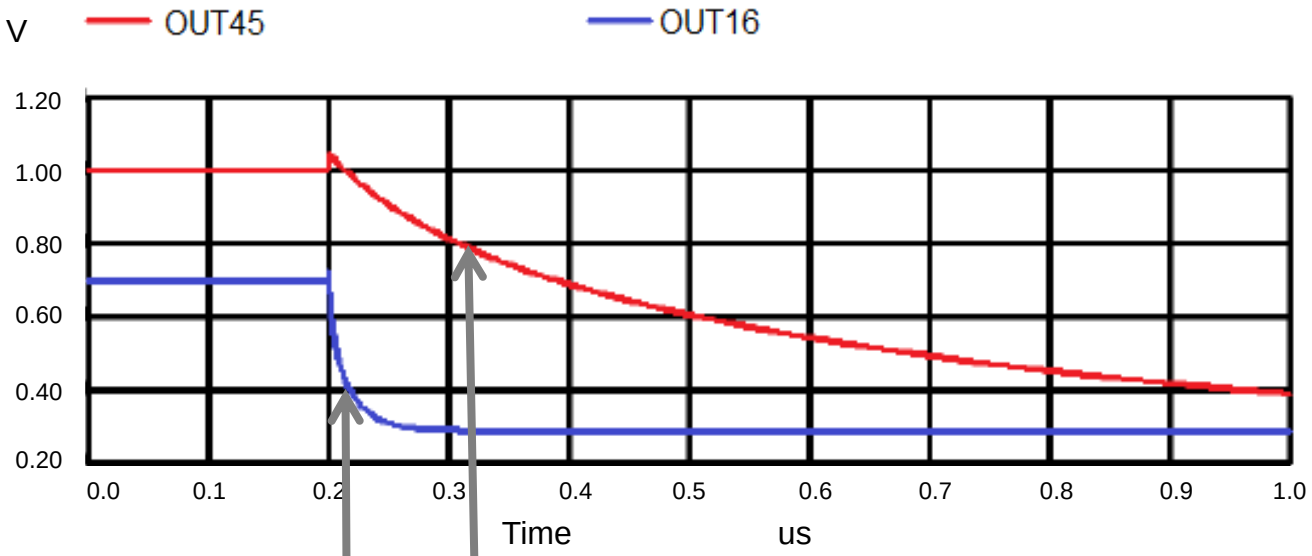




Obtained result with SOF in technologies of 16nm and 45nm.

High leakage currents influence greatly behavior of SOFs!

Holding Time



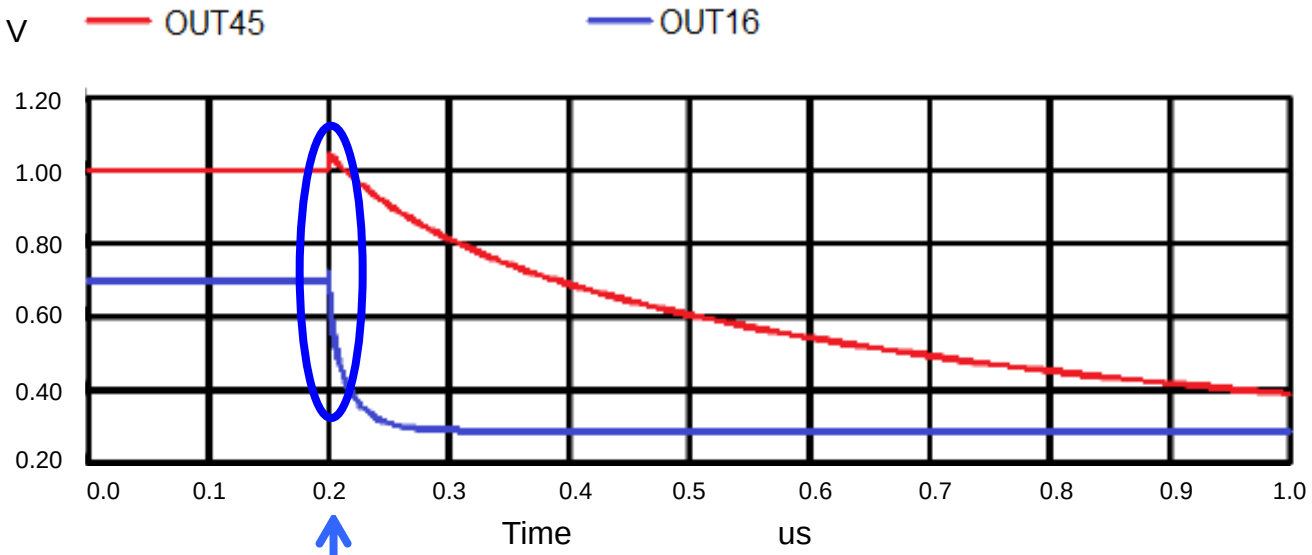
Holding time (VDD – |Vtp|)[1]

45nm = 200ns

16nm = 30ns

[1] R. Gomez, V. Champac, C. Hawkins and J. Segura, *A Modern Look at the CMOS Stuck-Open Fault, IEEE, 2009.*

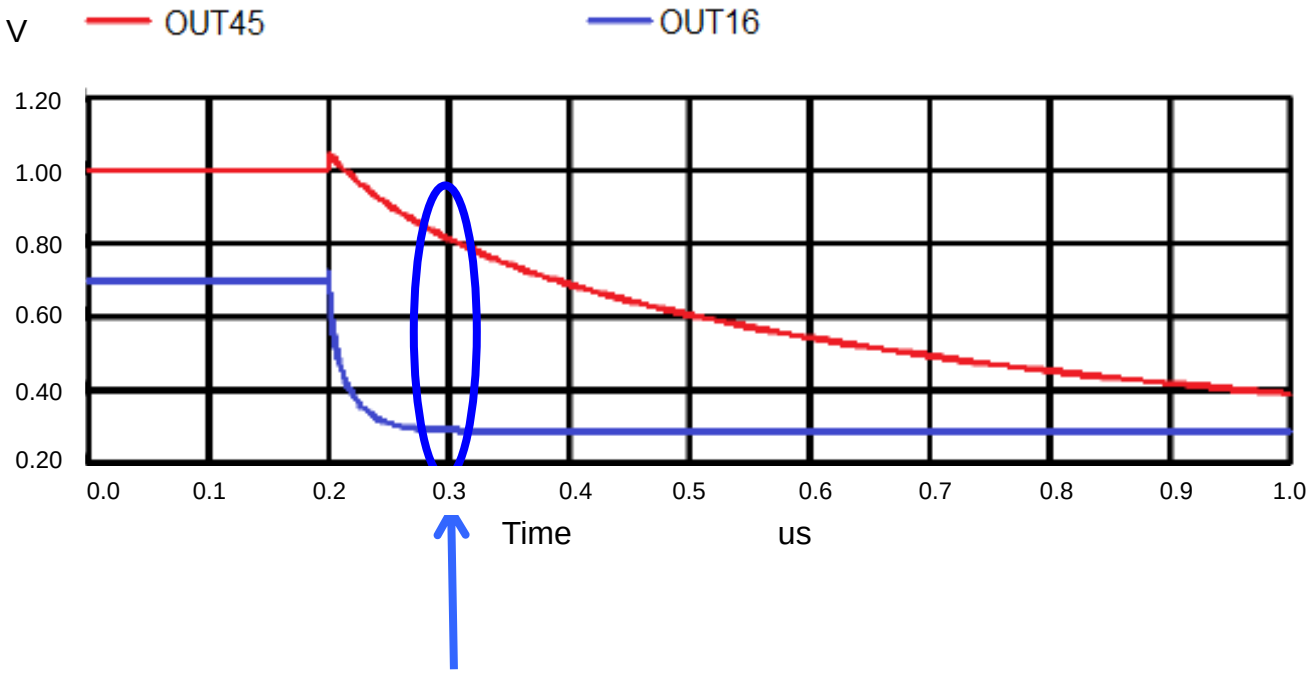
Holding Time x Technology



High Frequency

16nm: 1 fault
45nm: 1 fault

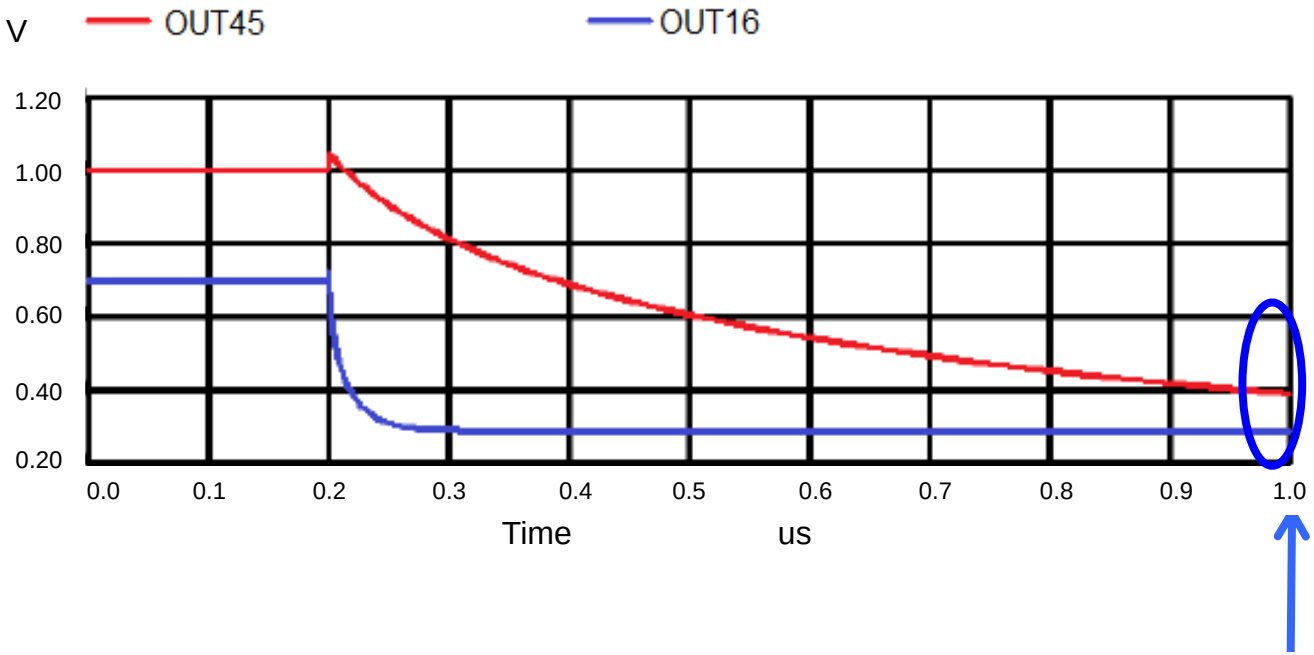
Holding Time x Technology



Medium Frequency

16nm: 0 fault
45nm: 1 fault

Holding Time x Technology



Low Frequency

16nm: 0 fault
45nm: 0 fault

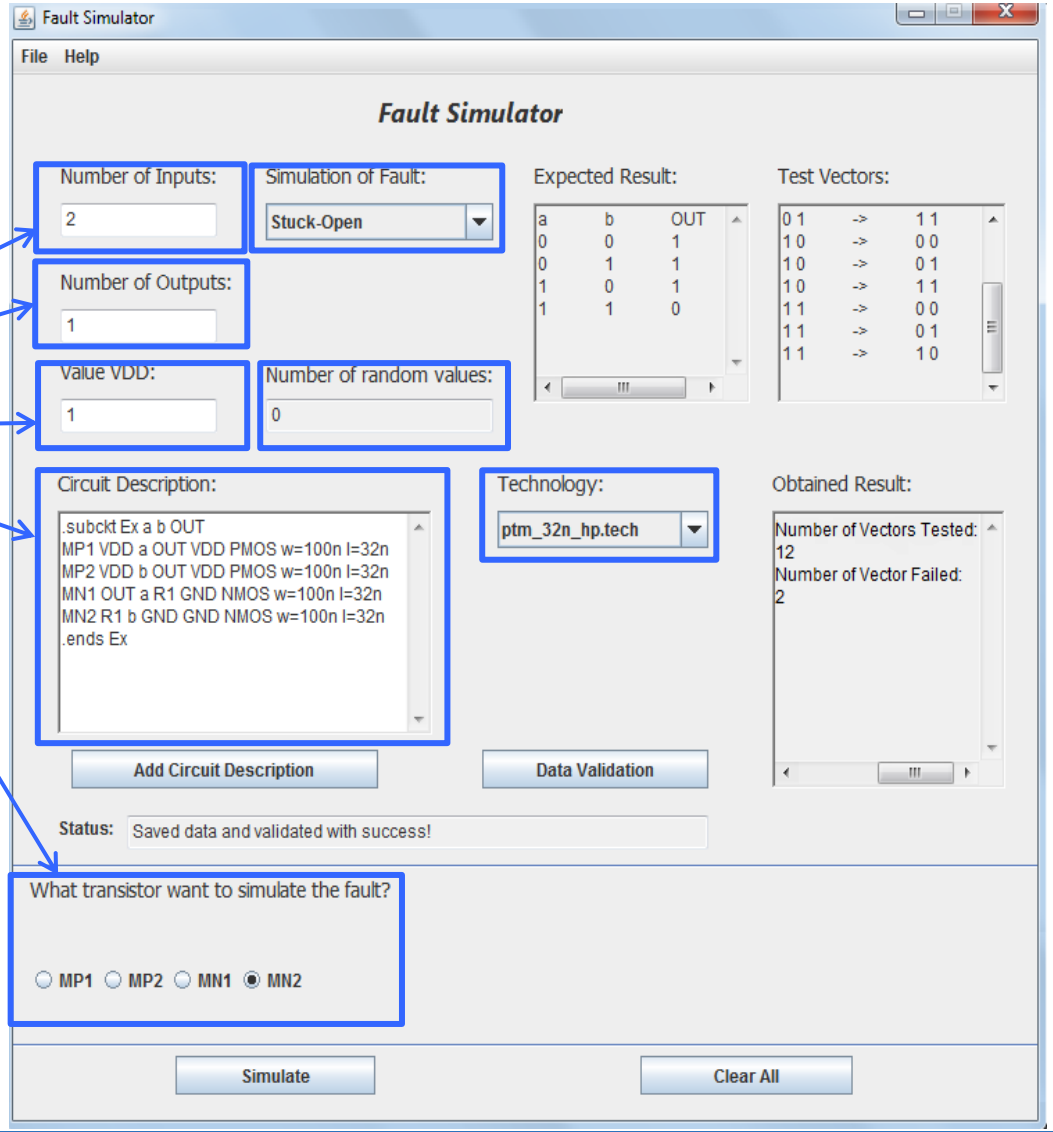
Motivation

- The use of tools that assist the project of integrated circuits are relevant due to the high design complexity.
  - Even more important in nanometer technologies due to emergent challenges

- This work presents a tool that analyzes the circuit behavior in the presence of SOFs and the interaction with leakage currents, also allows to evaluate the holding time parameter.

The Tool – Fault Simulator

- User Interface
  - **Input Parameters**
  - Fields generated by the program



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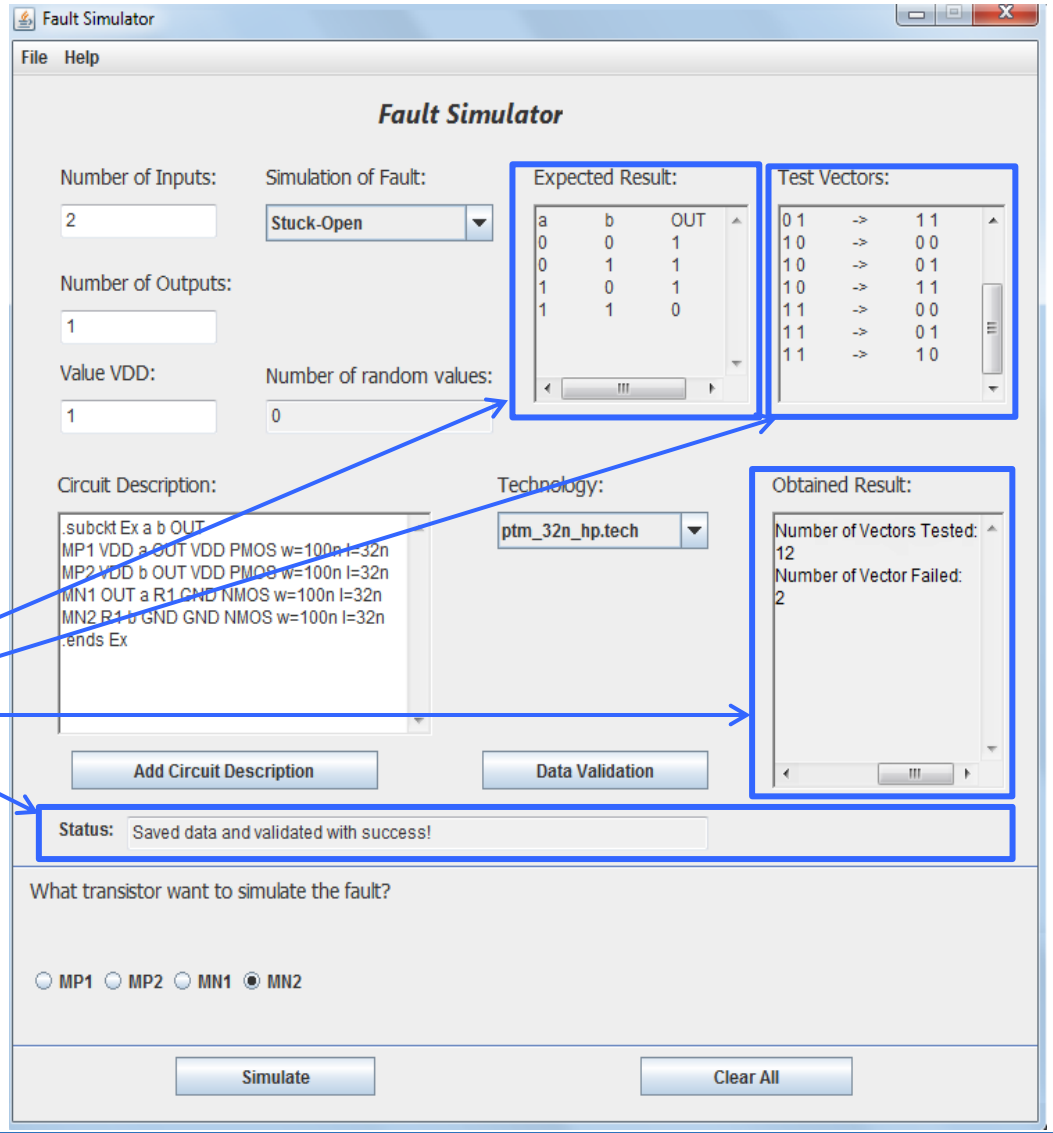
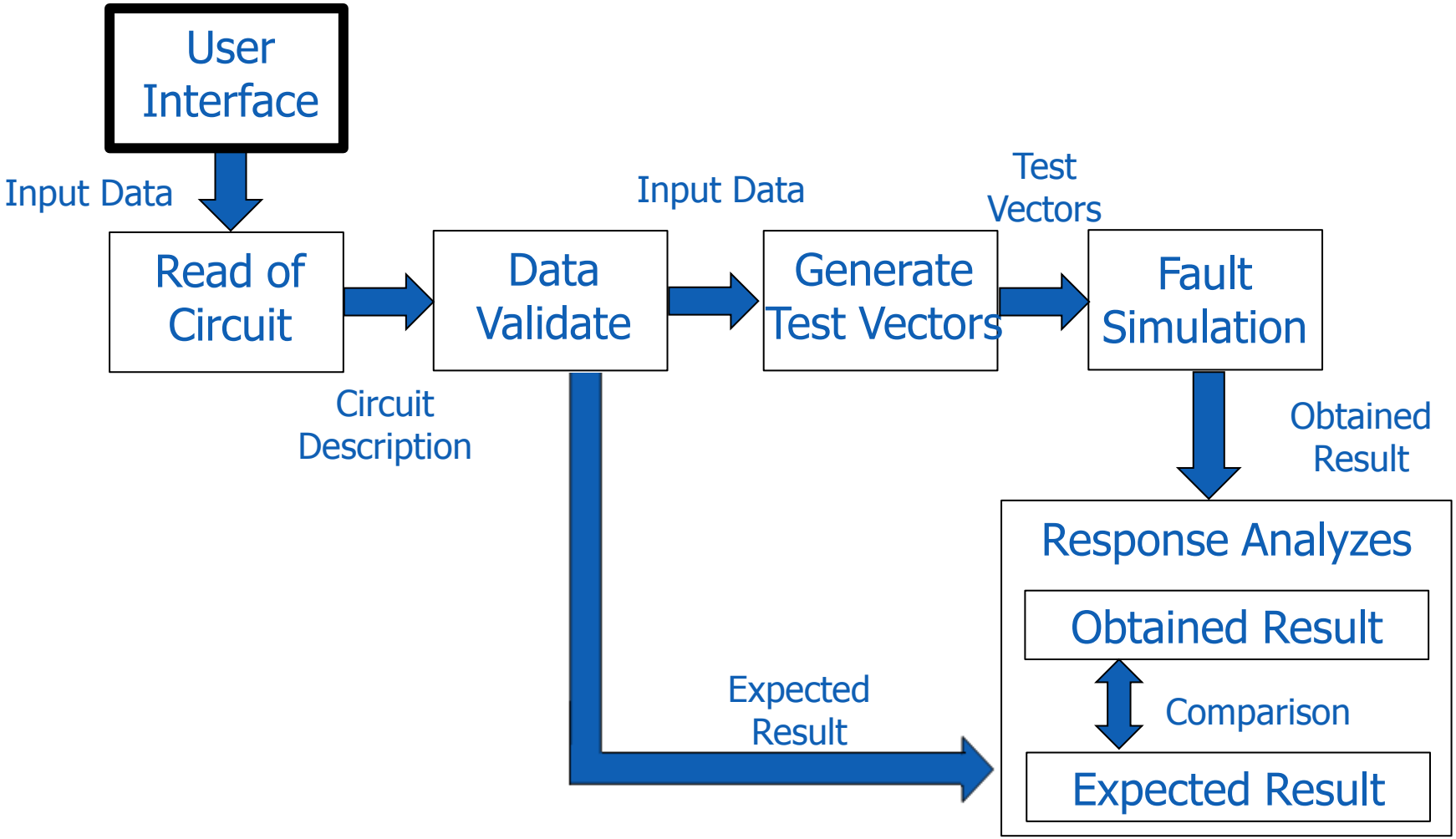
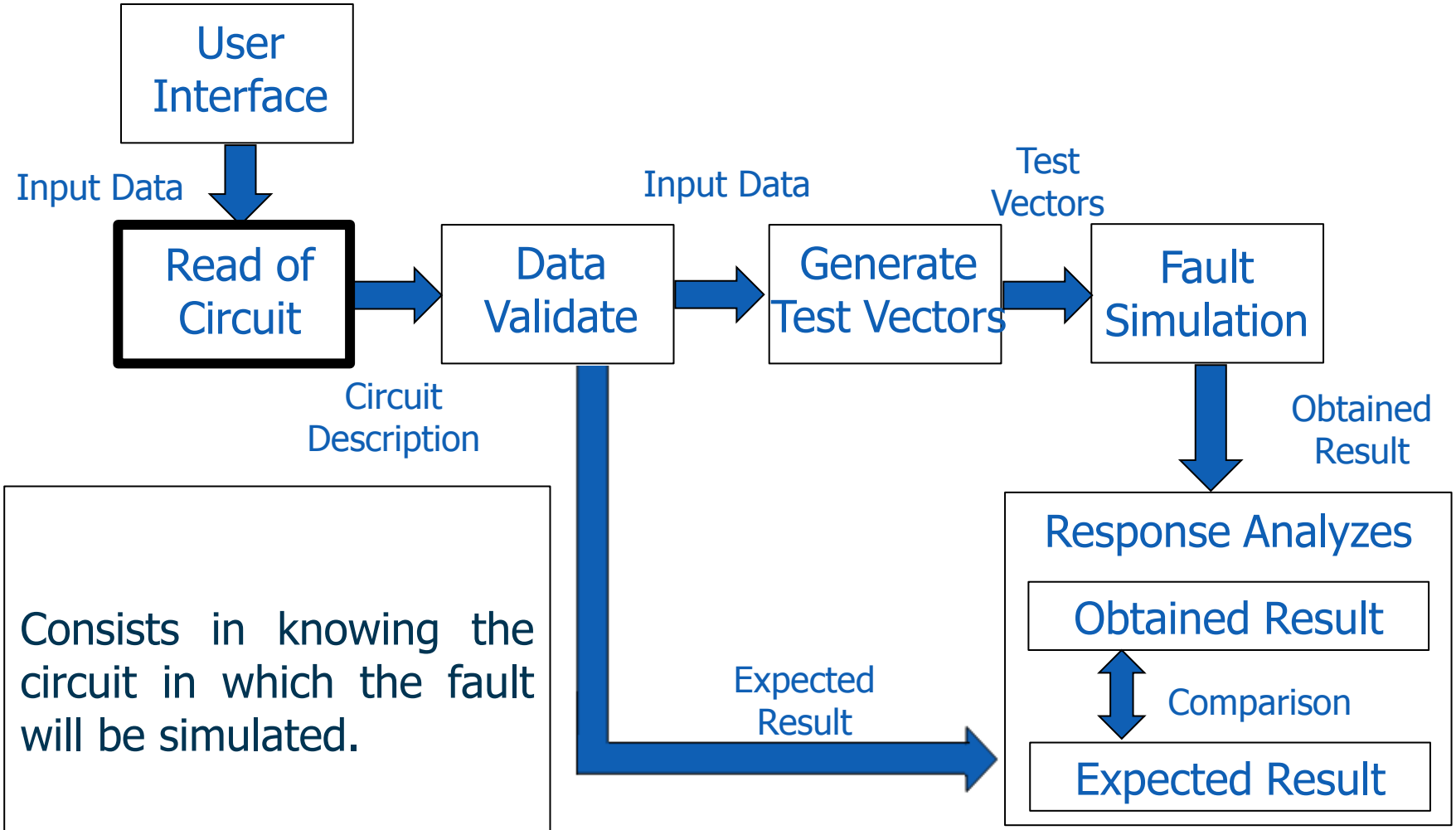


Tool Development

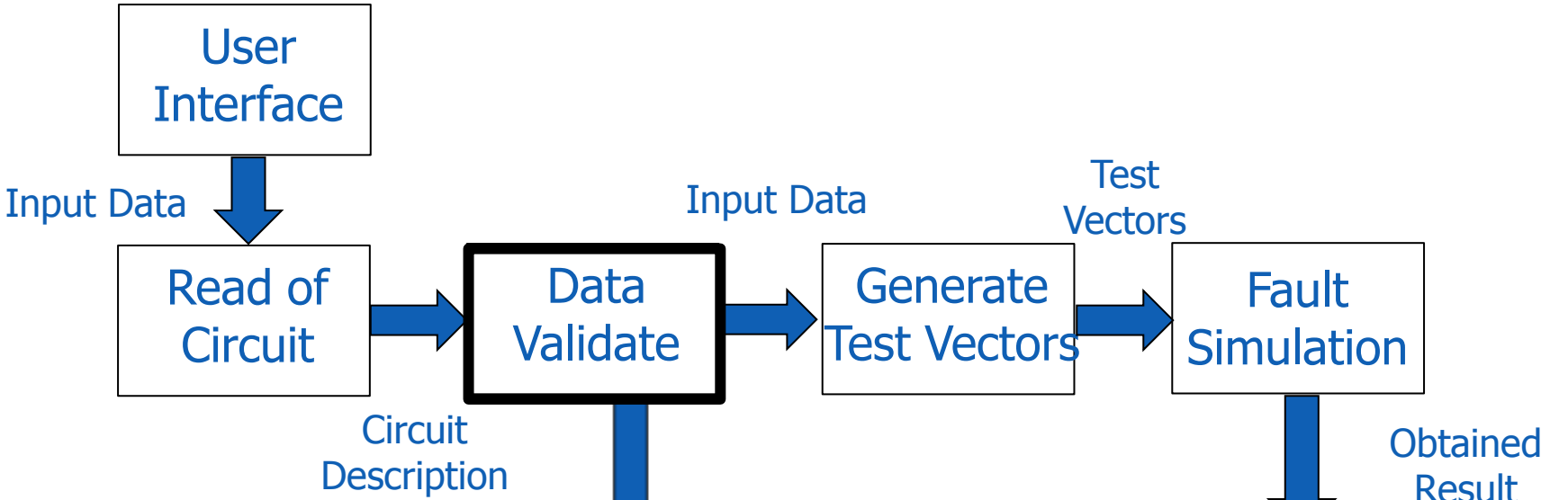


Tool Development



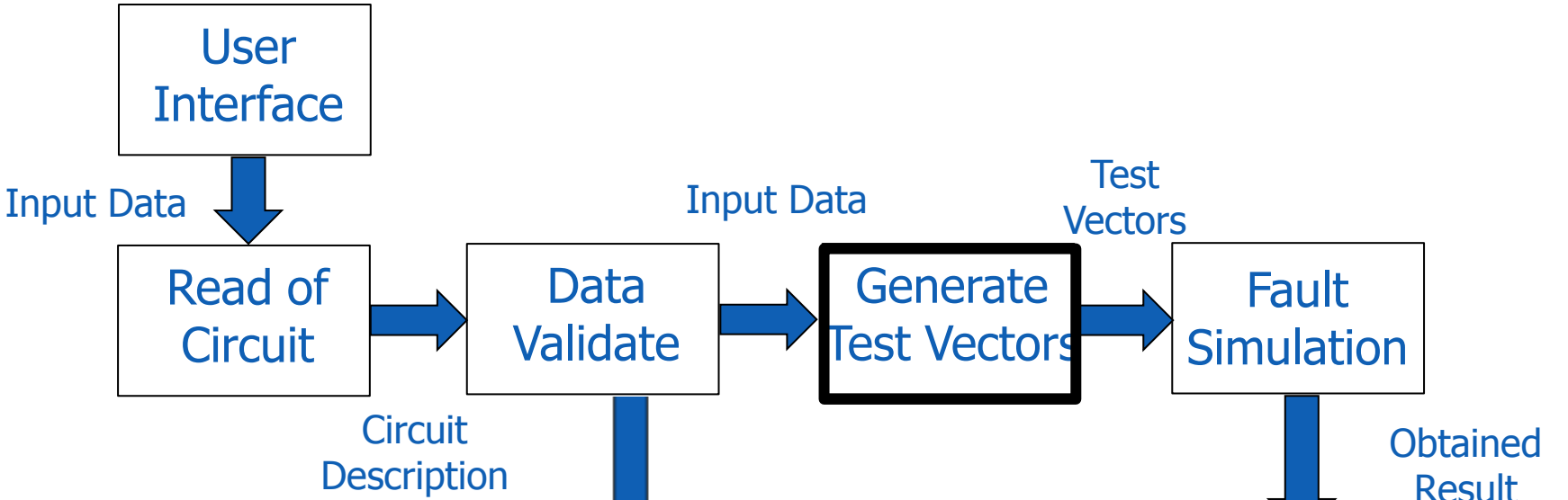
Consists in knowing the circuit in which the fault will be simulated.

Tool Development



Verifies the data supplied by the user.
Automatically generated the correct truth table.

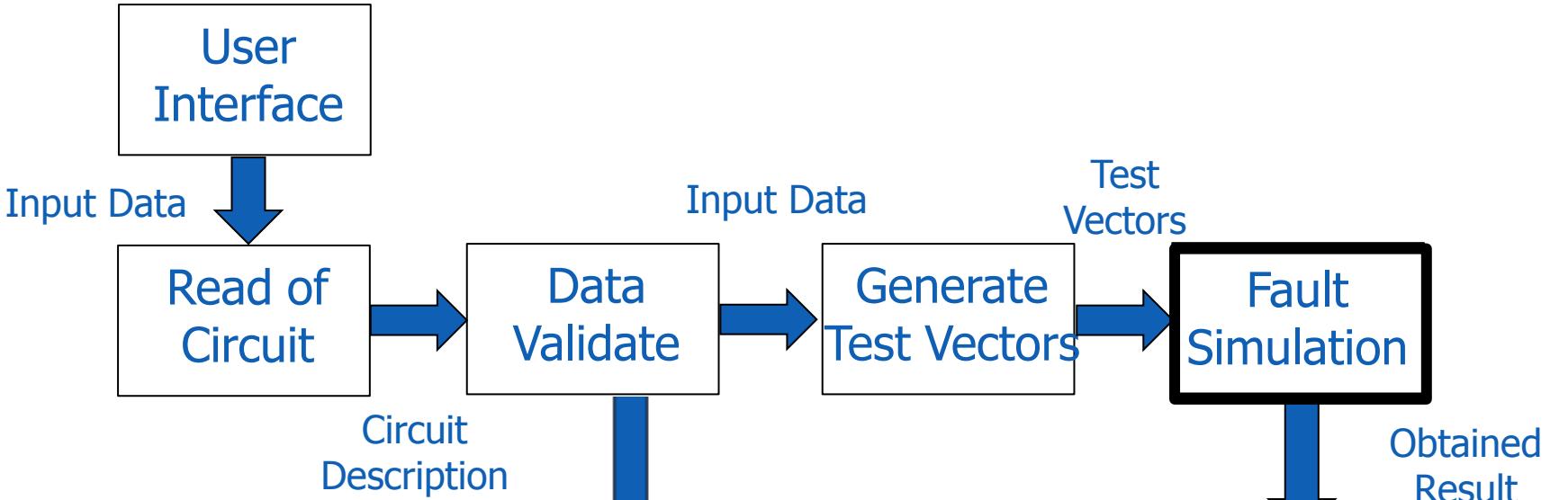
Tool Development



Generation of vectors:

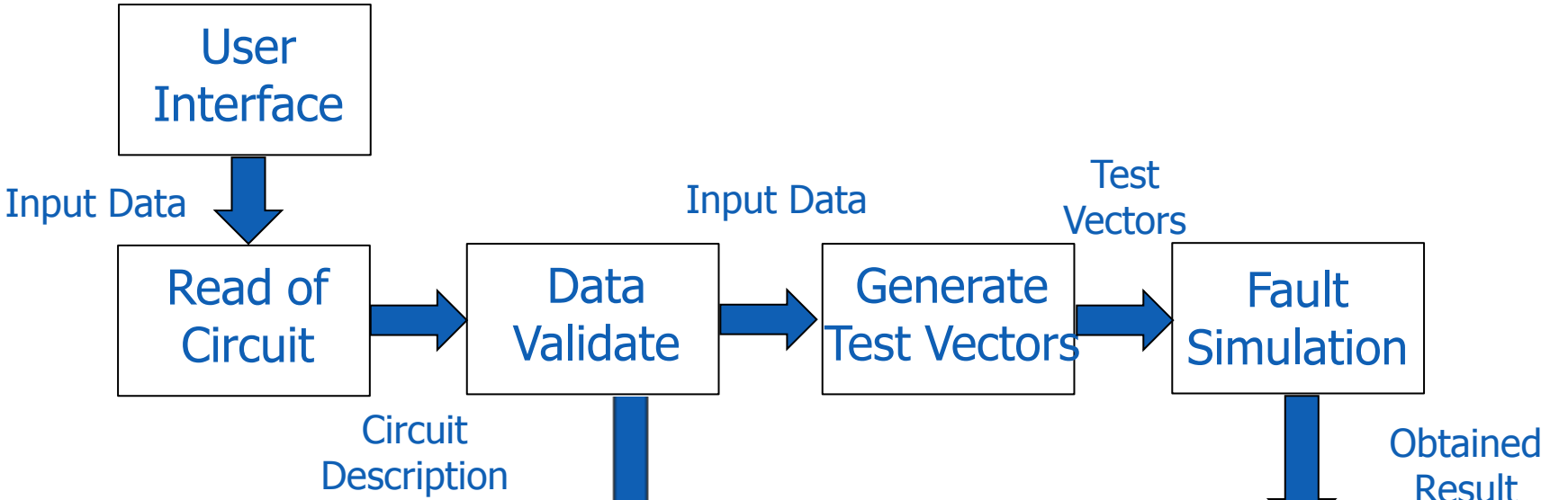
- <= 3 inputs: all combinations.
- > 3 inputs: random.

Tool Development



Simulates the circuit in the presence of a stuck-open fault in the transistor chosen for the user.

Tool Development



Makes the comparison between these two results and from this module calculates the percentage of faults during test application.

Conclusions and Future Works

- With the aid of this tool, it is possible to determine the coverage fault of some circuits;
- This tool can be also used to assist the impact evaluation of fault tolerance techniques applied to logic gates
- Next step in the development of this tool is compute the holding time and include analyses of other kinds of faults

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Muito Obrigada!

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