Comparison of 90nm and 65nm Logic Synthesis of a SAD Configurable VLSI Architecture

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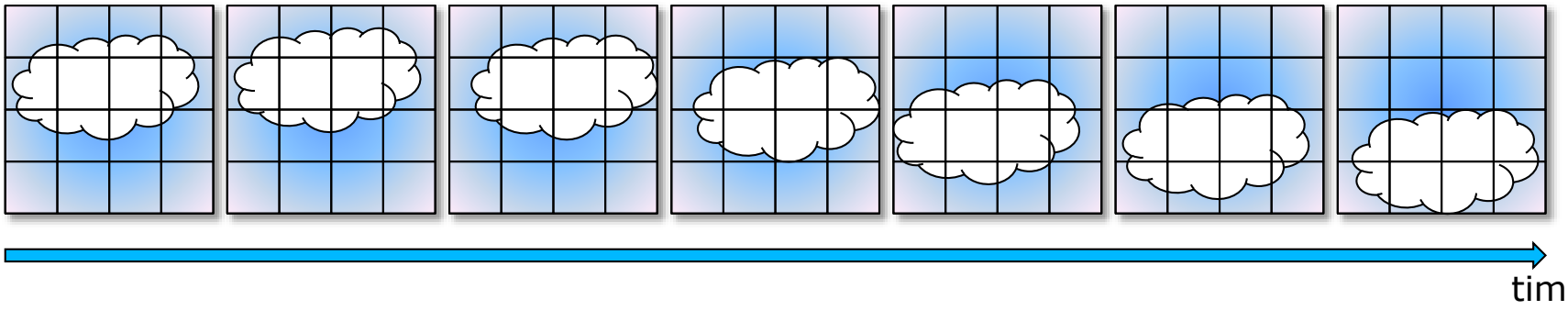
Outline

Comparison of 90nm and 65nm Logic Synthesis of a SAD Configurable VLSI Architecture

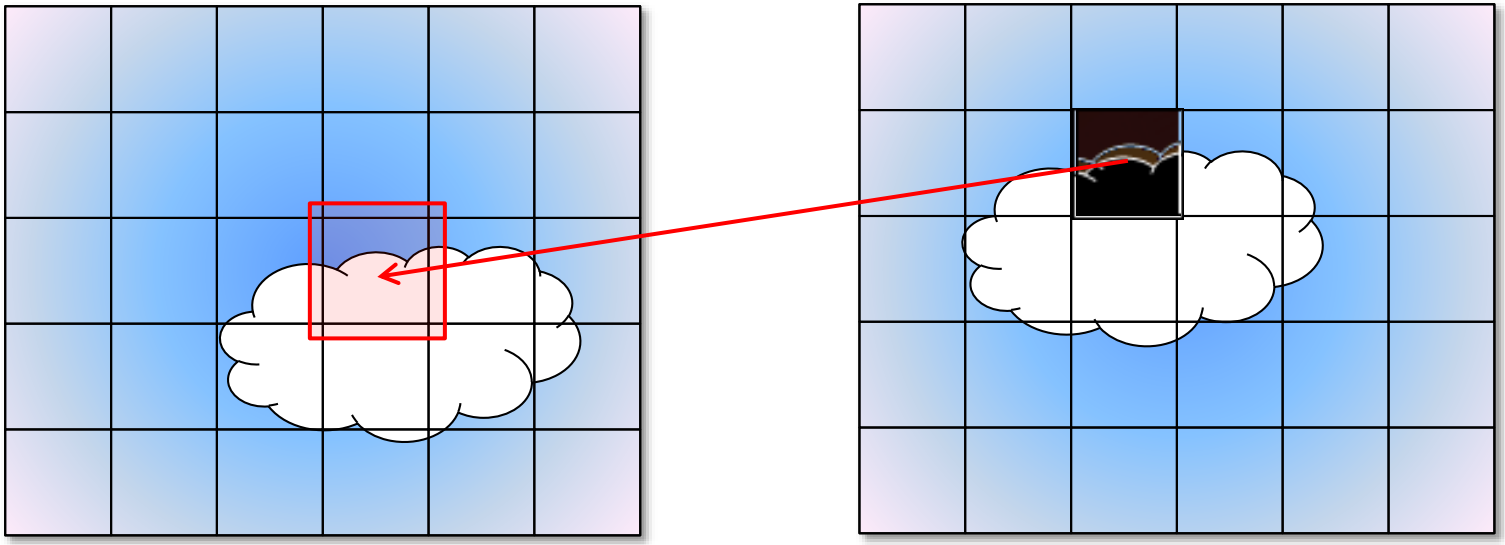
- ✓ Introduction
- ✓ Proposed SAD Architecture
- ✓ Synthesis Results
- ✓ Conclusions

Introduction



- ✓ Video is a sequence of images (called frames);
- ✓ Lots of redundant data!
  - ✓ Video compression explores the redundancies;
    - ✓ **Temporal, Spatial**, Frequency and Entropy;
- ✓ To simplify the compression, the frames are divided in blocks.

Temporal (Motion Estimation)



- ✓ Inter frame prediction;

Similarity Metrics

$$SAD = \sum_{i=0}^{M} \sum_{j=0}^{N} |Ori_{i,j} - Dec_{i,j}|$$

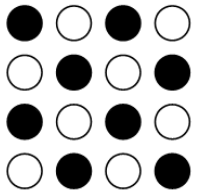
$$SSD = \sum_{i=0}^{M} \sum_{j=0}^{N} (Ori_{i,j} - Dec_{i,j})^2$$

$$SATD = \frac{1}{2} \sum_{i=0}^{3} \sum_{j=0}^{3} |H(Ori_{i,j} - Dec_{i,j})|H^T$$

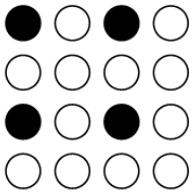
- ✓ Used for block matching;
- ✓ SAD is the most widely used:
  - ✓ Only addition, subtraction and module;
  - ✓ Fast and VLSI suitable;

Pel Decimation

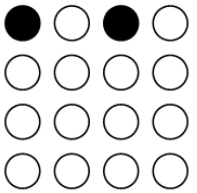
- ✓ Lots of data to process;
- ✓ Even with SAD being simple, the number of operations is high;
  - ✓ Increases as higher definition video will be adopted;
- ✓ It is a performance and power consumption problem;
- ✓ Ways to reduce:
  - ✓ Reducing the search area
  - ✓ **Pel decimation!**
  - ✓ Both strategies combined…
    - ✓ Ex.: APS, GEA and QME;



(a) 2:1



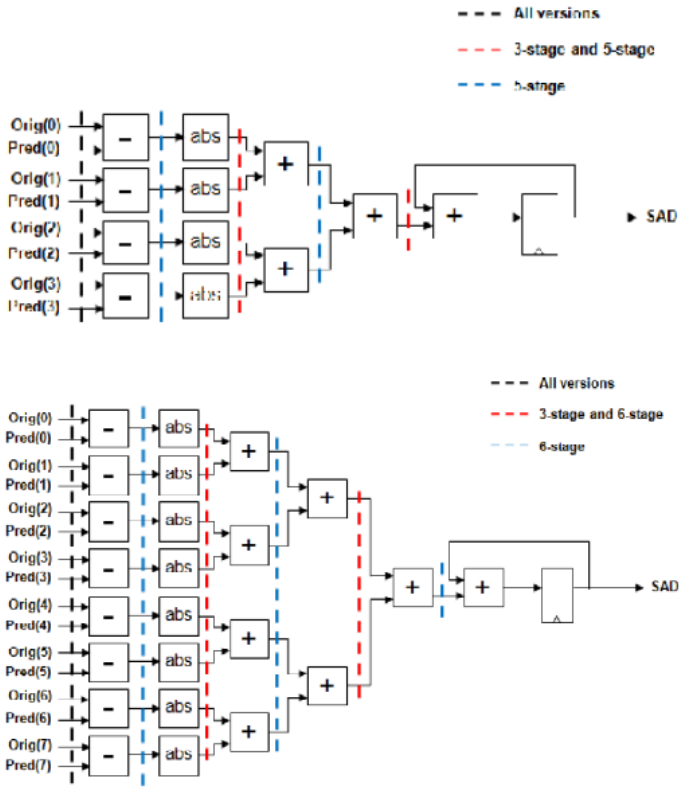
(b) 4:1

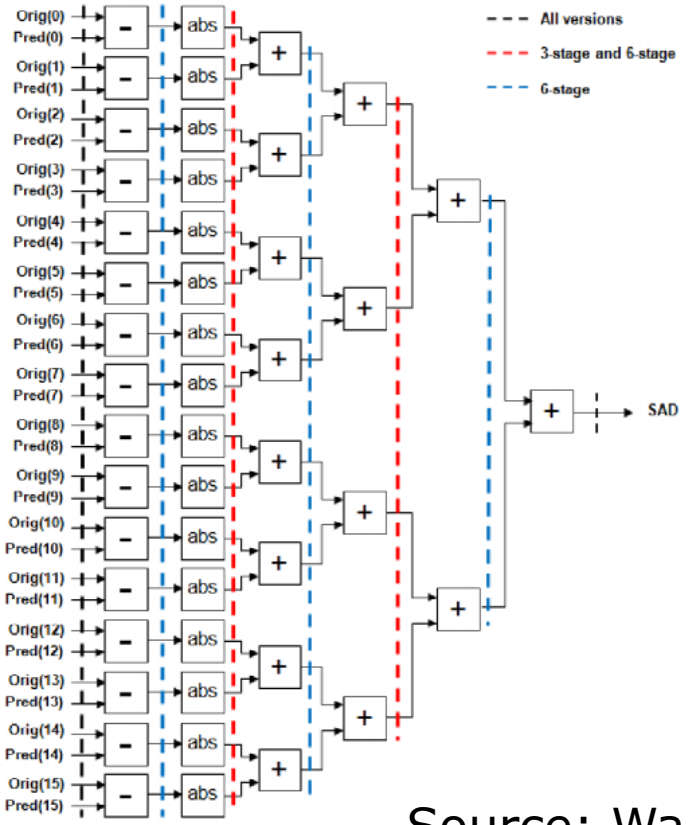


(c) 8:1

SAD Architectures

- ✓ Walter (2011) conducts a study of several full SAD architectures:



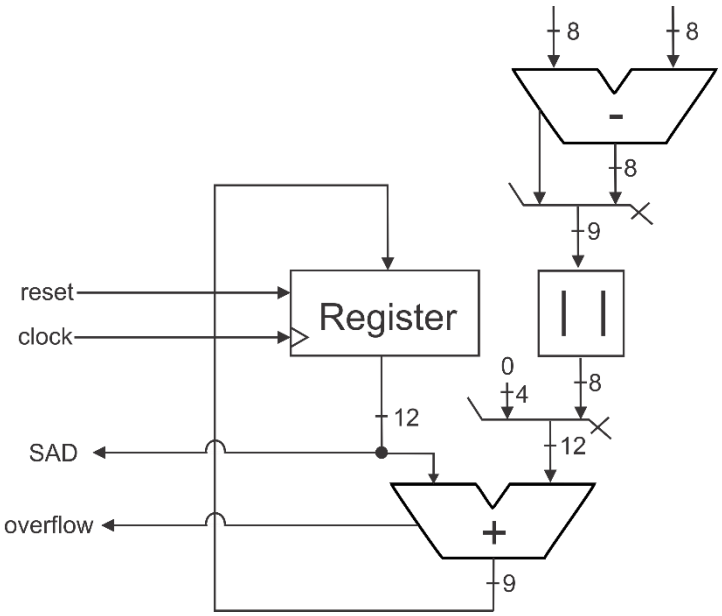


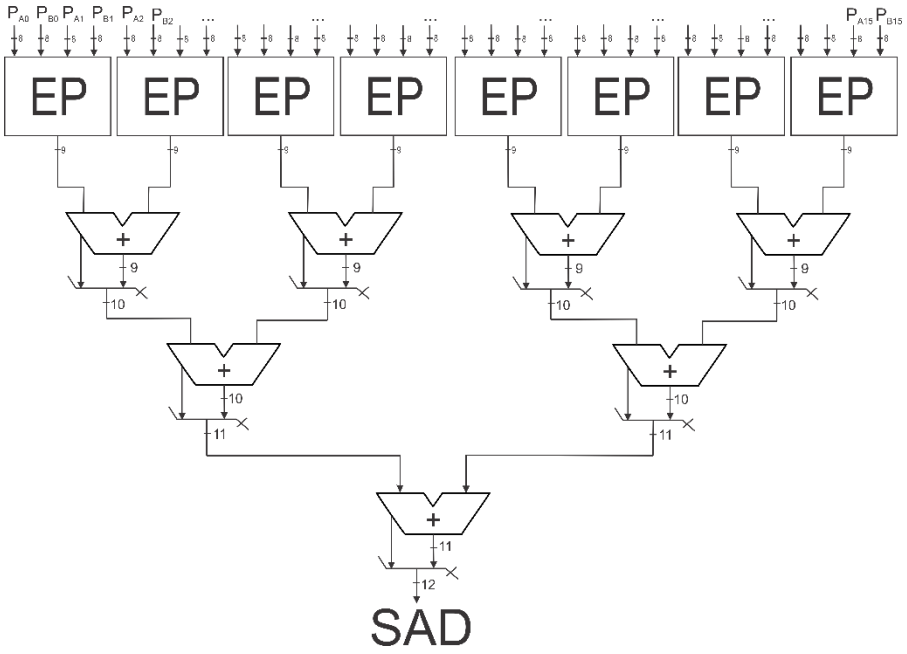
Source: Walter, 2011

Proposed Architecture

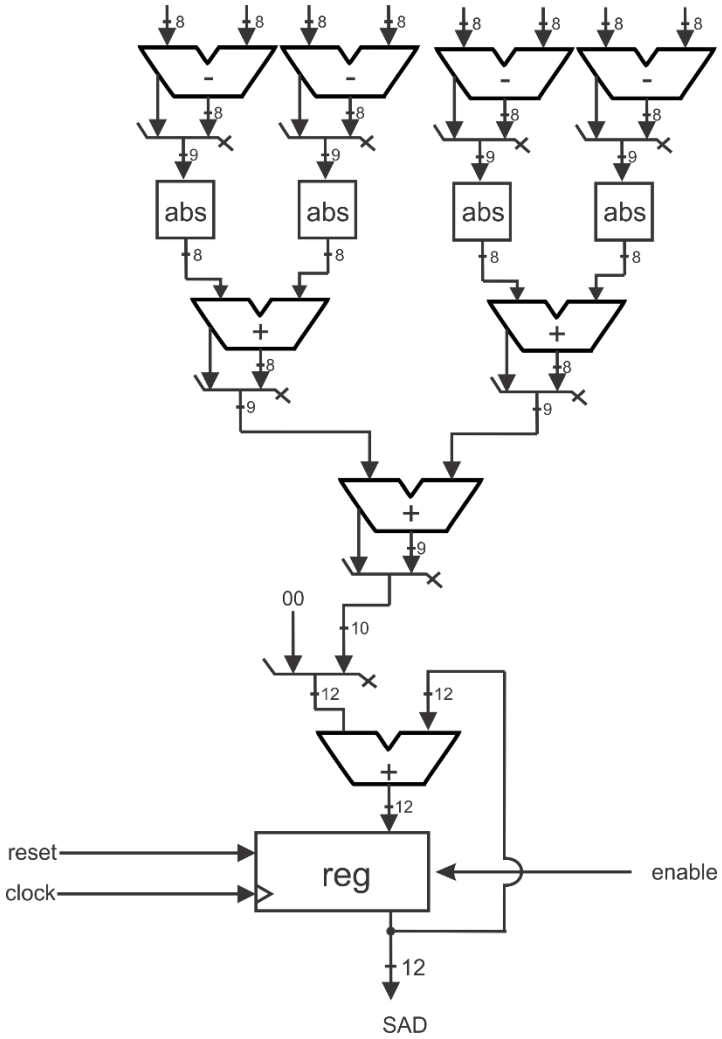
- ✓ Pel decimation reduce quality **but** also reduce time!
  - ✓ Energy efficiency is time dependent…
- ✓ 4x4 block SAD calculation with pel decimation configurability
  - ✓ 1:1 (full), 2:1 and 4:1;
  - ✓ User application can choose between quality/energy saving;
- ✓ Target is energy efficiency:
  - ✓ Energy-efficient architecture;
  - ✓ Low-Vdd/High-Vt synthesis;
  - ✓ Maximum frequency vs. target frequency synthesis.

Which Architecture?





Chosen Datapath



- ✓ Using the best characteristic of each one;
  - ✓ Easy to control subsampling;
  - ✓ Energy efficiency optimized for 4:1 pel decimation;

Synthesis

- ✓ For a fair comparison, two non-configurable architectures were also synthetized using 90nm and 65nm technologies;
  - ✓ 4-input as the same architecture than our configurable.

- ✓ Synthesis list (TSMC 90nm and TSMC 65nm):
  - ✓ Configurable nominal max frequency;
  - ✓ Configurable nominal target frequency;
  - ✓ Configurable LH max freq.;
  - ✓ Configurable LH target freq.;

  - ✓ All the above, but non-configurable.

- ✓ Target frequency: *66.67Mhz*, the same target as the literature for comparison:
  - ✓ Our solution provides less throughput as the state machine is more complex;
  - ✓ But remains with **high** throughput (432Msamples/s) than **recommended** (62Msamples/second) by Walter for **1080p@30fps**!

Synthesis Results I – Target Freq.

		(A)	(B)	(C)	(D)	(E)	(F)	(G)	(H)
	Technology (nm)	90	65	90	65	90	65	90	65
	Frequency (MHz)	66.67	66.67	66.67	66.67	66.67	66.67	66.67	66.67
	Area (μm²)	3025.6	2037.2	3027.7	2020.4	3710.0	2041.2	3717.1	2050.0
Power(μW)	Dynamic	100.2	64.4	99.1	64.1	51.5	40.3	51.2	40.2
	Leackage	6.22	13.01	6.20	12.73	0.58	3.02	0.58	3.03
	Total	106.4	77.4	105.3	76.8	52.1	43.3	51.8	43.2

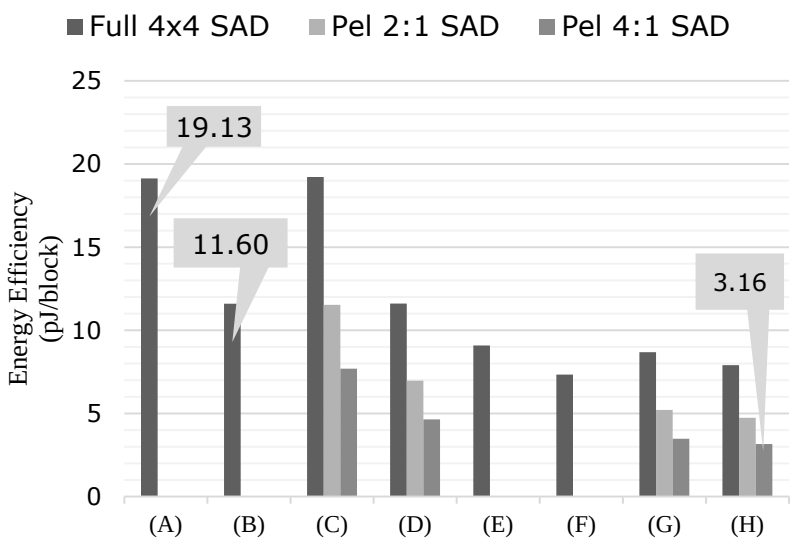
	Architecture			
	Non-config		Config	
	90nm	65nm	90nm	65nm
Nominal	(A)	(B)	(C)	(D)
Low-Vdd/High-Vt	(E)	(F)	(G)	(H)

Synthesis Results II – Max Freq.

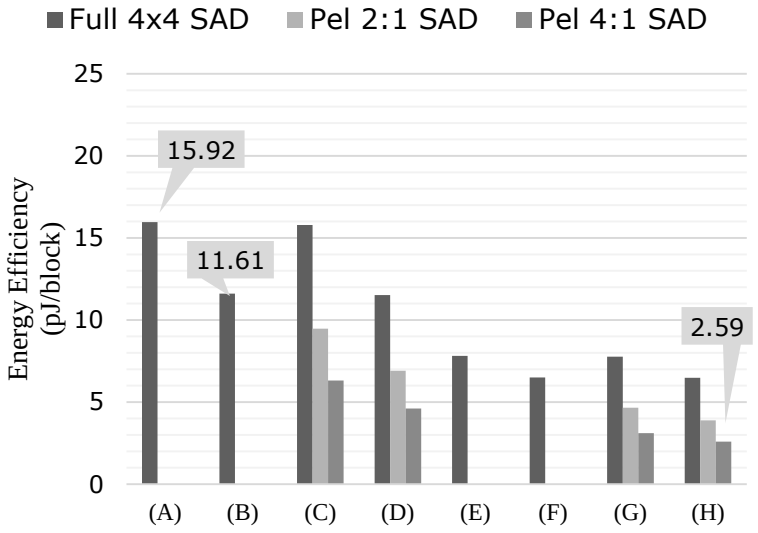
		(A)	(B)	(C)	(D)	(E)	(F)	(G)	(H)
	Technology (nm)	90	65	90	65	90	65	90	65
	Frequency (MHz)	800	1250	800	1250	270.27	675.67	270.27	675.67
	Area (μm²)	5011.8	3114.0	5104.3	3098.0	5845.2	3336.8	5622.9	3728.8
Power(μW)	Dynamic	1517.8	1426.4	1524.9	1427.5	244.5	490.0	233.7	527.1
	Leackage	12.75	24.03	13.05	24.00	1.09	5.73	1.03	6.95
	Total	1530.5	1450.4	1537.9	1451.5	245.6	495.8	234.7	534.0

	Architecture			
	Non-config		Config	
	90nm	65nm	90nm	65nm
Nominal	(A)	(B)	(C)	(D)
Low-Vdd/High-Vt	(E)	(F)	(G)	(H)

Energy Efficiency Results



Energy efficiency for maximum frequency



Energy efficiency for target frequency

	Architecture			
	Non-config		Config	
	90nm	65nm	90nm	65nm
Nominal	(A)	(B)	(C)	(D)
Low-Vdd/High-Vt	(E)	(F)	(G)	(H)

Conclusions

- ✓ This work presented a comparison between two technologic nodes of configurable and non-configurable architectures (90nm and 65nm) for SAD calculation, using or not High-Vdd/Low-Vt;
- ✓ Both technologic nodes synthesis results highlighted that the impact of pel decimation configurability is negligible;
- ✓ Pel decimation brought energy efficiency and latency gains of:
  - ✓ 40% for Full SAD/Pel 2:1
  - ✓ 60% for Full SAD/Pel 4:1
- ✓ The configurable 65nm/LH synthesis using pel decimation 4:1, demanded 7.4 times less energy than the configurable 90nm/NN synthesis with full-sampling.

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Thank you!
Questions?

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