Application of gm/I_D Methodology for Analog Design Using Nanometer-Scale Devices

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***Abstract*— The goal of this paper is to present the application of the gm/I_D methodology for the design of analog integrated circuits using nanometer-scale transistors. The advantage of this methodology is that it is based on the characteristic curve gm/I_D versus the normalization current (I_N) or gate to source voltage for the transistors sizing. There is no need to evaluate complex electrical device models as in traditional design methodology. Moreover, gm/I_D methodology is suitable for low voltage design since it explores all transistor operation regions. As example, the design of a differential amplifier in 32nm node for CMOS, FINFET and CNTFET technologies is presented. The results show that this methodology can be easily adapted for the design of analog circuits over different technologies.**

***Keywords*— Analog design, nanometer-scale, differential amplifier, gm/I_D methodology**

I. INTRODUCTION

With the evolution of the integrated circuits, there is a need to reduce the dimensions of the transistors to accommodate the growing demand for devices with higher speed and lower power consumption. Nowadays, the CMOS technology is dominant over other manufacture technologies, but some device parameters, like the typical thickness of gate oxide layer (Tox) are in the magnitude order of a few nanometers, near the physical limit [1][12]. Therefore, there is a need for exploration of alternatives for CMOS technology, such as FINFET or CNTFET transistors.

In the analog integrated circuits design, the designer uses a specific methodology in order to obtain a sized circuit. In general, the initial values are estimated using device simplified equations, which are simple to work, such as spice model Level 3 for MOSFET. These equations give a straightforward relation between drain current, terminal voltages, and small signal characteristics. With the initial values, electrical simulations are used to evaluate the circuit performance and specifications. Some iterations for fine tuning and re-simulation are performed in order to finish the circuit design.

However, this simplified approach is not suitable for new emerging technologies, which do not have compact electrical models capable to relate current and voltage in a simple form.

To improve the design techniques composed by new nanodevices, different methods must be explored. Besides that, it is necessary a method that explore all operation regions (weak, moderated and strong inversion regions) and that is compatible with low-voltage design.

The main objective of this paper is to show the application of the gm/I_D methodology for the design of analog integrated circuits using deep-submicron technologies for devices such as CMOS, FINFET and CNTFET. As an example, the design of a differential amplifier in 32nm node will be described. Predictive parameters are used to perform electrical simulations for CNTFET [13], FINFET [7] and CMOS technologies.

This work is organised as follows: section II presents the main characteristics of the CMOS, FINFET and CNTFET technologies. Section III explains the proposed methodology based on the gm/I_D curve to design a differential amplifier. Section IV presents the design of a differential amplifier. Finally, section V presents some concluding remarks.

II. NANOMETER-SCALE DEVICES

The CMOS technology is the currently dominant technology for integrated circuits implementation. Free design parameters of a CMOS transistor are the width (W) and length (L) of the channel, as shown in Figure 1. The device miniaturization results in increasing complexity and a proximity of the technological limits. At the same time, this miniaturization leads to more complex device models for modeling short channel effects, which are intensified as the channel geometry shrinks.

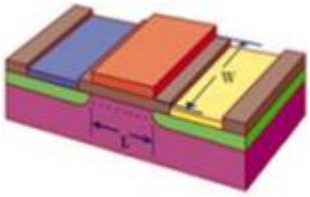

Figure 1 - CMOS transistor structure

The FINFET device features vertical conduction channels directly from planar transistor. It is fabricated on a silicon island, tall and narrow, called finger. The device has a dielectric layer called hard mask (on top of the silicon layer),

which is used to prevent the formation of parasitic channels. The FINFET transistor device is considered a double gate, since the height of the finger is greater than its width. The importance of having multiple gate is the greater transconductance when compared to devices with simple gates [4]. For the design of analog circuits with FINFET technology, the designer has the freedom to vary the dimensions L and the number of FINFETS in parallel for emulating a larger W. Figure 2 shows the structure of a FINFET device [3].

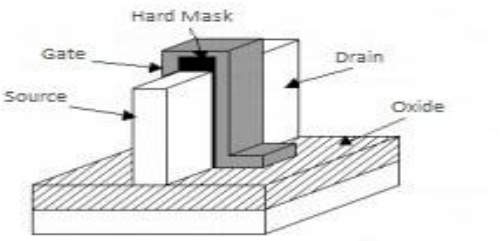

Figure 2 - FINFET transistor structure.

The CNTFET transistor has a structure similar to the CMOS transistor but the transistor channel is replaced by a carbon nanotube, as shown in Figure 3. This replacement brings a ballistic transport of the charge carriers between the drain and source, resulting in more current capacity and velocity [5][6]. Transistor width is fixed, given by the diameter of the nanotube. For larger widths, it is necessary to use a parallel association. The carbon nanotube diameter is obtained with the following equation:

$$D_{CNT} = a\frac{\sqrt{n_1^2 + n_1.n_2 + n_2^2}}{\pi}$$

Here, a_1 and a_2 are the lattice vectors and n_1 and n_2 are multiplier factors that control the rolling direction. The electrical characteristics of a carbon nanotube are based on the nanotube rolling direction. Transistor threshold voltage can be controlled by the correct choice of n_1 and n_2 [2].

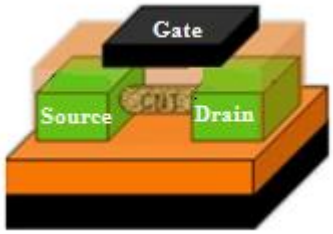

Figure 3 - CNTFET transistor structure.

III. THE gm/I_D METHODOLOGY

The gm/I_D methodology is a design technique that considers the relationship between the ratio of the transconductance gm over DC drain current I_D and the normalized drain current $I_N = I_D/(W/L)$ as a fundamental design tool. The advantages of the using gm/I_D method are:

1) It is strongly related to the performances of analog circuits.
2) It gives an indication of the device operation region.
3) It provides a tool for calculating the transistors dimensions.

This methodology is an immediate way to the design because most of equations that model electrical behavior circuits can be represented in accordance with the relationship gm/I_D [7].

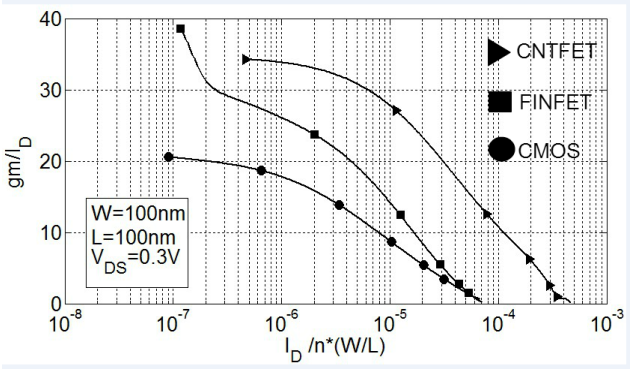

Figure 4 - gm/I_D versus I_N curve for a n-type device in CNTFET, CMOS and FINFET technologies

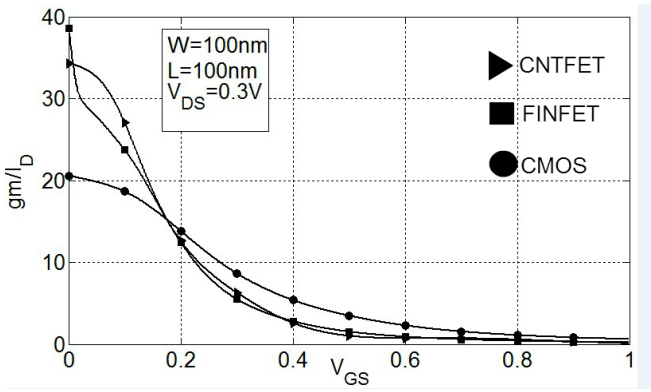

Figure 5 - gm/I_D versus V_{GS} curve for a n-type device in CNTFET, CMOS and FINFET technologies

The gm/I_D ratio is a measure of efficiency to transform current into transconductance. In other words, as higher the value of the gm/I_D, higher will be the transcondutctance to a constant current value [8].

The gm/I_D curve can be observed as the derivative of the logarithmic of I_D with respect to V_{GS}, as shown below:

$$\frac{gm}{I_D} = \frac{1}{I_D}.\frac{\partial I_D}{\partial V_{GS}} = \frac{\partial(\ln(I_D))}{\partial V_{GS}}$$

This derivative is maximum in the weak inversion region, where the dependence of I_D in relation to V_{GS} is exponential. In the strong inversion region it is almost linear because of the velocity saturation effect [9].

According to [10], the gm/I_D ratio is also size independent. The normalized current gm/I_D x I_N is independent of the transistors size. Therefore, the gm/I_D ratio is a unique feature to all transistors of the same type (n-type or p-type), depending on only its technology. Figure 4 and 5 show the simulated gm/I_D versus I_N and gm/I_D versus V_{GS} curves for n-

type CNTFET, CMOS and FINFET technologies in 32nm node. The three technologies presents near the same threshold voltage. It is possible to notice that CNTFET has the higher gm/I_D relationship comparing to the others.

IV. Design of a Differential Amplifier

The differential amplifier is an analog building block that has numerous applications. Its ordinarily function is as the input stage of most operational amplifiers [11]. The differential amplifier circuit is used to amplify the voltage difference between its inputs. In other words, the circuit output will be the voltage difference between the inputs multiplied by a gain. Figure 6 shows the schematics of a differential amplifier. This amplifier is composed by a differential pair (M1 and M2), a current mirror active load (M3 and M4) and a reference current mirror (M5 and M6). For matching constraints, M1=M2, M3=M4 and M5=M6.

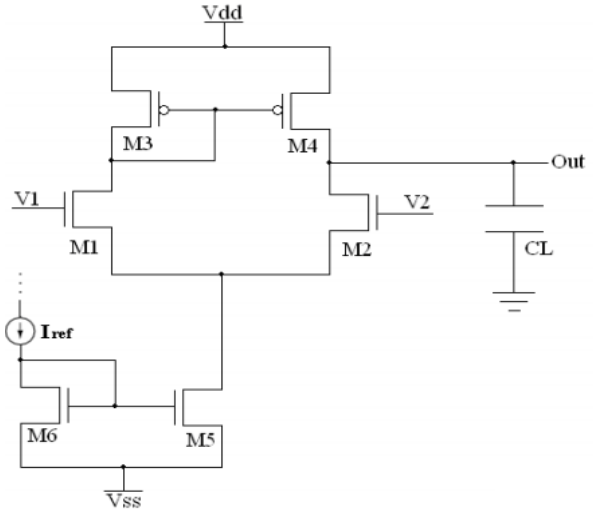

Figure 6 - Schematics of a differential amplifier.

The design of the differential amplifier using the gm/I_D methodology follows the sequence of steps which is illustrated in the design flow of Figure 7. The same procedure can be performed for the three technologies mentioned in this paper. The application of the gm/I_D methodology for the design of the differential amplifier consists in determining the dimensions of the transistor M1 and M3. Design specifications are the following: minimum slew-rate (SR=10V/µs), maximum dissipated power (P_{max} = 1mW) and minimum gain-bandwidth (GBW=10MHz). Environmental constraints are C_L=10pF, V_{DD}=0.45V and V_{SS}=-0.45V. Gate length for all transistors is kept fixed in L=100nm for this design. Because of this, the voltage gain of the circuit was not taken into consideration. With the maximum dissipated power, the maximum current of the circuit is defined according to:

$$I_{ref\,\max} = \frac{P_{\max}}{V_{DD} - V_{SS}}$$

It gives a maximum reference current of 1.11mA. The slew-rate specification determines the minimum current of the circuit:

$$I_{ref\,\min} = SR.C_L$$

So, the minimum current of the circuit is 100µA, which will be used for reference current of the current mirror. Now it is possible to estimate the drain current passing through the transistors, which is half I_{ref}. The minimum value of gm_1 is based on the specification of GBW:

$$gm_1 = GBW.2.\pi.C_L$$

To have a value of at least 10MHz in GBW, the minimum value of gm should be equal to 628µS. So, the minimum value of gm is adopted for the transistor M1, which defines gm/I_D the ratio.

$$\left(\frac{gm}{I_D}\right)_{M1,M2} = 12.56$$

The value of V_{GS} of transistor M1 can be determined by the gm/I_D x V_{GS} curve for n-type transistor. In order to guarantee M1 operating in saturation region, the following relation must be true:

$$V_{GS} \le V_{DS} + V_{TH}$$

Due to the low voltage characteristic of the target technologies, we perform a large signal analysis admitting that $V_{DD} - V_{SS}$ = 0.9V. Distributing over the three series transistors , it gives a V_{DS}=0.3V for M1, M3 and M5.

As the value of V_{th} is 0.13V, all transistors operate in the saturation region if V_{GS} is smaller than 0.43V. In this case, the value of V_{GS} of transistor M1 is larger than 0.43V, otherwise it would have to be redefined, respecting the minimum value of gm_1 previously calculated.

With the I_N value defined for the transistor M1, it is possible to find the width of this transistor:

$$(W)_{M1,M2} = \left(\frac{I_D}{I_N}\right)_{M1,M2} .L$$

The procedure to find the dimension W of the transistor M3 is the same as described previously, whereas the ratio

$$\left(\frac{gm}{I_D}\right)_{M3,M4} = 12.56$$

and the curves consulted are related to the p-type transistor. The design of the current source can be done by the traditional way, since voltages V_{DS5} and V_{GS5} are known from the electrical simulations.

For validation, the AC characteristics of the circuit is simulated and is shown in Figure 8. The final values of the W of the transistors for each technology are shown in Table 1. For the CNTFET version, the width is determined by the number of unit nanotubes in parallel (n) multiplied by the nanotube diameter (which is equal to 3.012nm). The same occurs for the FINFET version, in which the unit channel width is 160nm.

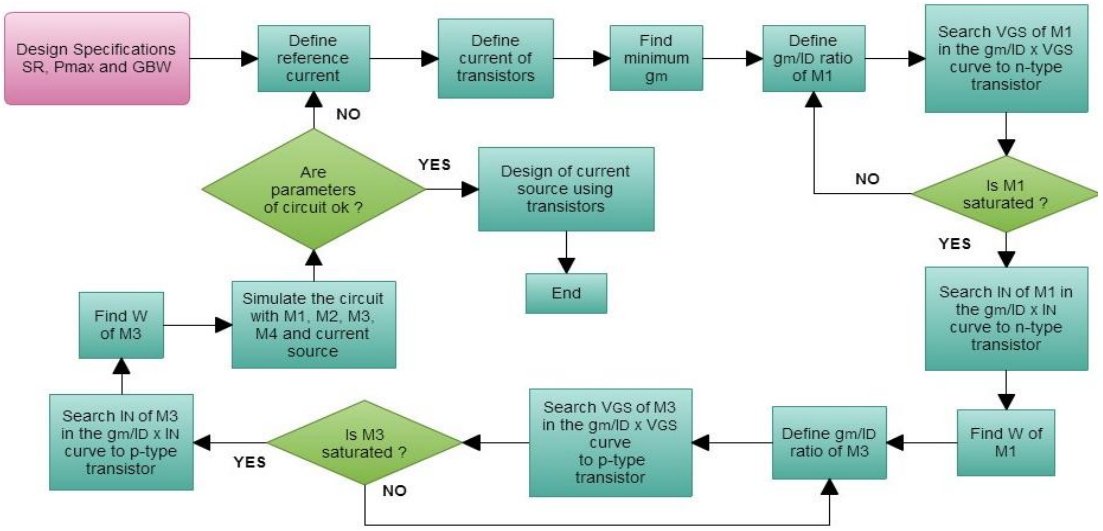

Figure 7 - Complete design flow for the design of a differential amplifier using gm/I_D methodology.

Table1- Gate widths for the designed transistors of the differential amplifier.

Technology	Transistor	Gate width
CMOS	M1, M2	1.08µm
	M3, M4	9.53µm
	M5, M6	0.56µm
FINFET	M1, M2	W=3*160nm=480nm
	M3, M4	W=7*160nm=1120nm
	M5, M6	W=3*160nm=480nm
CNTFET	M1, M2	W=22*3.01nm=66.3nm
	M3, M4	W=22*3.01nm=66.3nm
	M5, M6	W=13*3.01nm=39.2nm

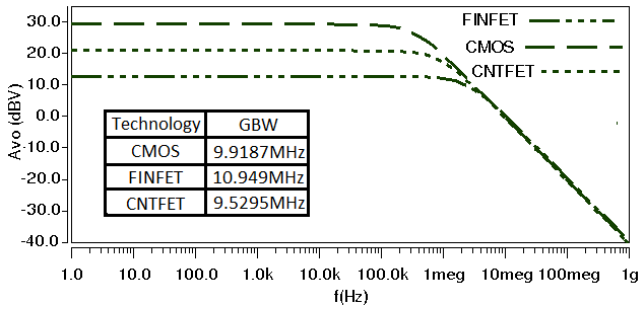

Figure 8 - Bode Diagram for the three versions of the designed differential amplifier.

V. Conclusion

The gm/I_D methodology is suitable for the design of analog blocks composed by nanometer-scale devices such as CMOS, FINFET and CNTFET. The design was validated observing that the *GBW* of the differential amplifier was very close to the specified value for the three technologies, while keeping the same dissipated power.

The gm/I_D methodology proved to be very simple for design since it did not take into consideration hand-made calculations with complex equations for modeling the devices. The curves that relate the gm/I_D with the normalized drain current and V_{GS} is a powerful tool for designing analog blocks in emerging technologies.

VI. Acknowledgments

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VII. References

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