Power Consumption Analysis in CMOS Static Gates

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Abstract — **This paper addresses power consumption in CMOS logic gates through an study considering the design and technology points-of-view. Through SPICE simulations, the relationship between charge/discharge and short-circuit components of dynamic power consumption are investigated both considering different logic gates and its evolution through technology scaling. Experimental results show that dynamic power consumption is still the main source of power dissipation in standard cell based design, whereas the short-circuit component seems to decrease through technology scaling. Static power consumption, on the other hand, keeps growing at each new node, and research effort has to be made to overcome it.**

***Keywords*— CMOS, digital circuits, power dissipation, short-circuit, logic gate.**

I. INTRODUCTION

Energy dissipation is a very critical parameter that has to be taken into account during the design of VLSI circuits. If in the early years of circuit design the main concern was related to performance and die area, submicrometer and nanometer technologies have brought power consumption to a main role. Some of the related problems are the heating in high-performance systems and the battery lifetime in portable applications market.

There are two major forms of design power efficient CMOS circuits: technology and project choices. The former includes research on new materials, reducing supply, threshold voltages, and doping levels. The latter includes algorithms, data encoding style, the use of pipeline, parallelism, clock gating or any other low power technique.

This work carries a study on the impact of both topology and technology choices on power consumption of logic gates used in standard cell libraries. Firstly, the behavior of both dynamic and static power consumption is analyzed in a commercial 0.35 µm CMOS technology. The relationship between the charge/discharge and the short-circuit components of the dynamic power consumption are evaluated taking into account the input slope and the output load of cells as well as the transistors sizing. In the next, the relationship between the dynamic and static power components over the technology scaling is analyzed through the CMOS inverter. Starting with the 0.35 µm until the 32 nm technology nodes, the importance of these two components on the overall performance regarding power consumption is considered.

The reminder of this paper is organized as follows. Section II gives a short background on power consumption of CMOS static gates. Section III analyses the behavior and interaction of power consumption on different logic gates. Section IV discusses the relationship between dynamic and static power consumption through technology scaling. Section V analyses the results, and Section VI brings some final remarks and conclusions.

II. BACKGROUND

Power consumption in digital VLSI circuits can be divided into two different categories: dynamic and static power components. The first one occurs every time the output of a gate changes its logic value. It can be divided in charge/discharge of circuit capacitances and short-circuit caused by a finite slope of the input transition allowing both networks to be on simultaneously. It creates a low resistance path for current between the power rails. This component is responsible for the main contribution to power dissipation of CMOS digital circuits.

The charge/discharge component has a well established form to be modeled. It depends on the frequency of the circuit *f*, the supply voltage V_{DD}, and the value of the node capacitances αC_{node}. The following equation summarizes the discussion:

$$P_{switching} = \alpha C_{node} f {V_{DD}}^2 \quad (1)$$

where the summation of $P_{switching}$ over all the nodes gives the total charge/discharge power consumption of the circuit.

The short-circuit component is less intuitive to be modeled because it depends on both, technology and design parameters. It depends on the threshold $V_{tn(p)}$, and supply voltages V_{DD}, the drive strength of the gate $\beta_{n(p)}$, the frequency of operation *f*, the input slope τ, and the output load α C_L connected to the gate. The following equation describes these dependencies:

$$P_{sc}(\beta n, \beta p, Vtn, Vtp, V_{DD}, \tau, C_L, f, \alpha) \quad (2)$$

where P_{SC} represents the short-circuit power dissipation. Some works treating this power component are [3,4,5,6,7].

Static power consumption is mainly the current that exists when the circuit is not switching or is holding a value. It is composed by all the undesired currents in the circuit due to the devices non-idealities. There are three major components that have significance in the normal operation of digital circuits. They are the subthreshold current, the tunneling gate oxide current and the reverse biased junction current [8], as shown in Fig. 1. The first one is seen in the weak inversion operation region, which happens due to the proximity of the threshold and the V_{DD}. Although this component has always been present, it has gained importance in submicrometer and

nanometer devices. It has an exponential relation with threshold voltage [9]. Gate current is important in technologies with the gate oxide thinner than 20 Angstroms [9]. It occurs due to imperfections or defects in the oxide, and it is important only when the logic gate has several transistors. Reversed biased junction currents occur due to all the reversed biased PN junctions present in the transistors. All these currents are due to geometry or fabrication issues. Generally in circuit design, only the subthreshold current and the gate tunneling current are taking into account on the calculation of the static power consumption.

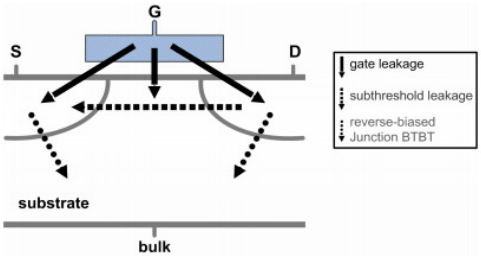

Figure 1 – Major static currents components [8].

III. Influence of Gate Topology on Power Consumption

This section describes the effects of circuit topology on power dissipation of a single logic gate. A 0.35 µm commercial technology is used for modeling the transistors. Starting with the inverter, the importance of the two components of the dynamic power is analyzed regarding the size of the gate, the input slope and the output load. Table I shows the dynamic power energy per cycle for a minimum sized inverter, keeping W_p/W_n = 2 in order to achieve a symmetric gate. The inverter is loaded by four equally sized inverters, the *fo4* rule of about 16 fF [10], and the input has a typical slope for this technology, obtained by the ring oscillator experiment of about 150 ps.

The total dynamic power is calculated through the current supplied by V_{DD} over the entire cycle. When the output transitions from '0' to '1', part of the current is used to charge the capacitances and part is wasted through the NMOS transistor due to the short-circuit. When the output goes from '1' to '0', the charge stored is discharged by the NMOS transistor while V_{DD} supplies a small amount of current due to the short-circuit. Fig. 2 shows the schematic of the CMOS inverter, where C_L stands for the input capacitance of the gates connected to its output.

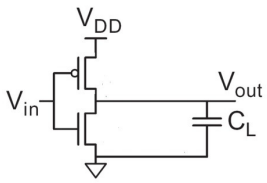

Figure 2 – CMOS inverter schematic.

It is shown that indeed the charge/discharge component represents the main source of the dynamic power dissipation, as predicted in [3]. The next experiment, whose results are depicted in Fig. 3, analyses the impact of the gate sizing on power consumption. Keeping Wp/Wn = 2, the size of the inverter is varied from the minimum width until 50 times this value for the analyzed technology. The inverter is loaded by the *f04* rule.

TABLE I - Dynamic Power Consumption of a Minimum Sized Inverter.

	Energy (fJ)
Charge/discharge	100
Short-circuit	20

It can be seen that both, the short-circuit and the charge/discharge energy increase. Roughly, this can be explained as follows: the charge/discharge component is only proportional to the output capacitance. As long as the *fo4* rule is used, the gate capacitance seen by the inverter output grows linearly with transistor size. It can also be seen that the short-circuit component also increases, but in a slower pace than its counterpart because this component is inversely proportional to the output capacitance C_L.

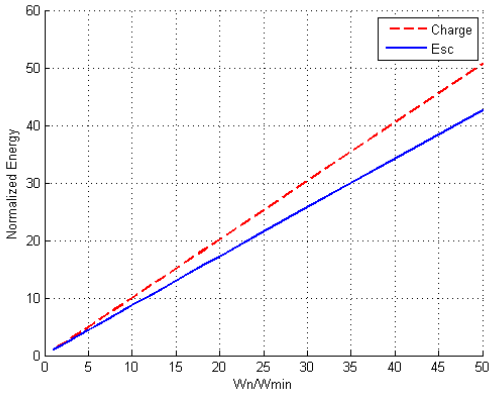

Figure 3 – Dynamic power consumption *vs.* inverter sizing.

The next experiment shows the impact of the input slope on the dynamic power consumption. Using the minimum sized inverter loaded by the *f04* rule, the transition time of V_{in} is varied from 150 ps until 8 ns. As depicted in Fig. 4, the charge/discharge component (dashed line) does not change, as expected by equation (1). The short-circuit (continuous line), in turn grows linearly with the input slope. Intuitively, it happens because the slower the input slope, the more time both networks will be on simultaneously.

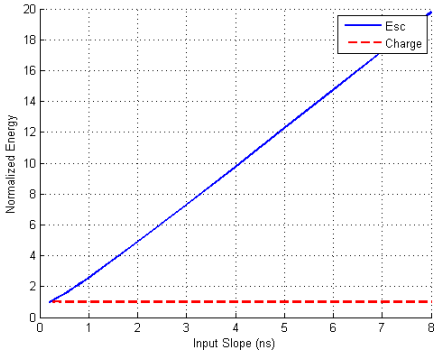

Figure 4 – Influence of input slope in the dynamic power consumption.

Fig. 5 depicts the influence of C_L on the short-circuit of a minimum sized inverter under various input slopes. As can be seen, the short-circuit augments as the output capacitance diminishes. It happens because as the capacitance decreases, less charge has to be removed from the output in order to change the V_{DS} of the block causing the short-circuit. The larger the $V_{DS,}$ the larger the short-circuit current. To reinforce this conclusion, Fig. 6 depicts the short-circuit energy as a function of C_L for some arbitrary input slopes. As expected, the longer the input slope, the greater the short-circuit energy.

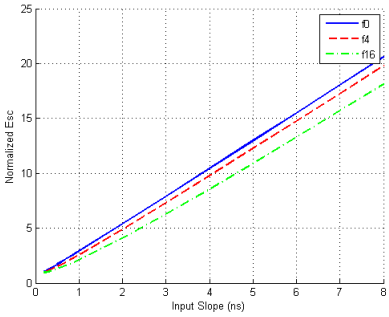

Figure 5: Influence of output capacitance on short-circuit power dissipation.

After the inverter, NAND (NOR) gates are analyzed. They present a similar behavior, caused by the stacked transistors in the pull-down (-up) network, respectively. Fig. 7 shows 2-input NOR (a) and NAND (b) gates. The short-circuit, as explained, depends on various parameters, including the position of the input transitioning. Fig. 8 shows that the closer to the power rails, the greater the short-circuit is in a NOR2 gate. It happens mainly due to the body effect, which can be modeled as an increase in the threshold voltage of the transistor.

Regarding the static power consumption, we observe in Table II that when more than one transistor is off in a stack, the static power consumption decreases by about 30%. It is known as the *stack effect* that is also due to the body effect in the transistor [7]. In the table are the static currents of a minimum sized inverter as well as a minimum sized 2-input NOR gates. It can be seen that, for this technology, the leakage currents are not a significant part of the total power dissipation. In smaller nodes is evident that the body effect is stronger, for instance, in a 32 nm technology the difference in the subthreshold current between a single transistor and 2 stacked transistors is almost 30 times [6]. Although the stack effect is a very effective way of decreasing static currents, there is a tradeoff between this component and area and switching speed.

TABLE II - STATIC POWER CONSUMPTION OF A MINIMUM SIZED INVERTER AND 2-INPUT NOR GATE.

Cell	Input Vector	I_{static} (pA)
INV	0	6.73
	1	7.45
2-input NOR	00	13.5
	01	12.8
	10	7.93
	11	5.93

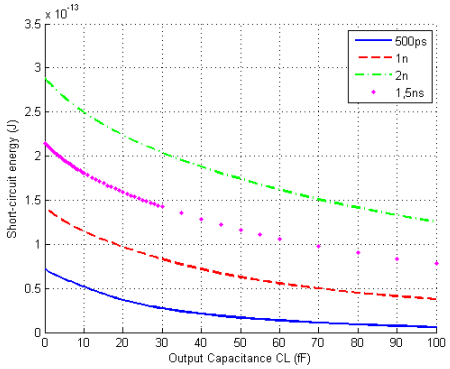

Figure 6: Short-circuit energy *vs.* output capacitance.

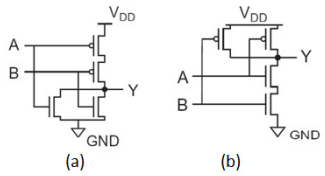

Figure 7: Schematic of 2-input NOR (a) and NAND (b) gates.

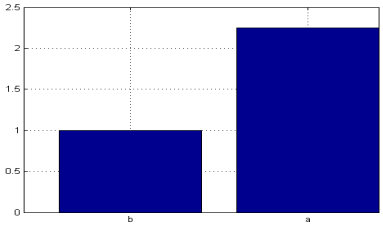

Figure 8: Short-circuit dissipation of a 2-input NOR gate (the results are normalized in relation to the B-input of the NOR gate shown in Fig. 7).

IV. POWER DISSIPATION THROUGH TECHNOLOGY SCALING

In this section, the effects of technology scaling on power dissipation are analyzed through the study of the CMOS inverter. The relationship between the dynamic and static power consumption, as well as a comparison between the two components of the dynamic dissipation are presented. Using as reference the 0.35 µm technology analyzed in the previous section, power consumption is analyzed in 180, 130, 90 and 65 nm commercial technologies, besides a 45 and 32 nm PTM technologies [12].

Fig. 9 shows the dynamic power consumption of a single, minimum sized inverter under a typical input slope and loaded by the *f04* rule. The results are normalized in relation to the 0.35 µm technology. It can be seen that the dynamic power consumption decreases with scaling. It happens because, besides the reduction on voltage supplies, the capacitance that has to be charged decreases with smaller transistors.

Fig. 9 also shows what happens to the short-circuit component. It can be seen that this component decreases faster than the charge/discharge component. It happens mainly because of the ratio between V_t/V_{DD}. It was about 0.2 in early technologies, but it turns around 0.4 in modern nanometer processes. In the case where $V_t/V_{DD} > 0.5$, short-circuit will no longer exists.

The static power consumption, in contrast, becomes a problem as transistor sizes decreases. Table III shows the static currents for minimum sized inverters for each of the studied technologies. As can be seen, the static current density rises from a few pA/µm in the 0.35 µm technology to more than a hundred nA/µm in the 32 nm PTM technology.

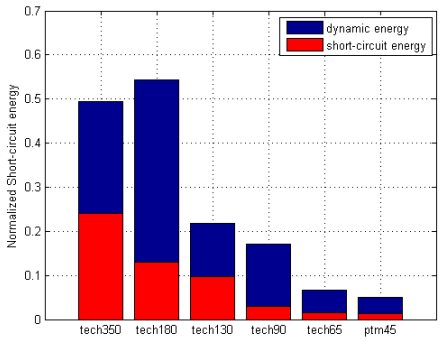

Figure 9: normalized charge/discharge and short-circuit component of dynamic power consumption in the inverter logic gate in several technologies.

TABLE III - STATIC CURRENT DENSITY FROM A 0.35 µm TO A 32 nm NODE TECHNOLOGY.

Tech.	**0.35**	**180**	**130**	**90**	**65**	**45**	**32**
J_{sub}(nA/µm)	0.0087	118.5	6.1	16.9	0.6	79.6	173.9
J_{gate}(nA/µm)	0	0	0	0	0	4.4	4

As predicted, this component becomes a major problem in recent technology nodes. Subthreshold currents grow nearly exponentially while gate currents begin to appear in nanometer devices, below 90 nm nodes. To alleviate the problem of gate current, high-k materials were introduced in modern CMOS processes.

V. FINAL ANALYSIS

The dynamic consumption still is the dominant component in power dissipation, mainly due to the charge/discharge of circuit capacitances. The short-circuit component only becomes a problem when the gate is submitted to large input slopes and/or small output loads. Besides, the trend found in recent technology nodes of reducing power supply faster than the threshold voltages may indicate that this component will lose importance in future technologies since in the case that $V_{DD} < V_{tn} + |V_{tp}|$ the short-circuit no longer exists.

The static power consumption, in contrast, keeps growing with each new technology node. Although transistors have always been imperfect switches, the constantly increase in the number of transistors in a single package along with the severity of these imperfections in submicrometer devices makes this component of dissipation no longer negligible. Both, the subthreshold and gate currents increases exponentially with transistor scaling [9] and other parasitic currents are becoming more important due to the new effects presented by the different fabrication methods. Effort will have to be made to overcome these problems, both in design techniques like power efficient architectures and technology issues like the use of new materials to control these undesired currents.

VI. CONCLUSIONS

Due to the importance of energy dissipation in modern semiconductor industry, a study on power consumption in static CMOS logic gates was carried out in this work. Both, the impact of the gate topology and the technology scaling were taken into account. The two components of power dissipation, dynamic and static, were analyzed. Results show that the dynamic power component is still the main source of power dissipation. For a single logic gate this component decreases at each new node but the increase in the number of transistors per chip maintain the power density inside a chip nearly constant. The short-circuit component seems to lose importance in recent nodes. The static power, in contrast, becomes a problem and keeps gaining importance in recent nodes. Research effort has to be made to keep these currents under control.

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