

Parallel Characterization of Operational Amplifiers for Acceleration of Design Optimization

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Abstract—This paper presents a characterization method for an optimization based tool for analog integrated circuit automatic sizing. This characterization method is based on a set of test benches to estimate the specification values by electrical simulations. These values are used as goals and constraints in the optimization procedure. The proposed method is implemented in Matlab® with a Synopsys HSPICE® interface and is suitable for parallel execution, reducing the optimization time. As design example, this paper shows the application of the methodology for the design of an OTA Miller in 0.25 μ m TSMC fabrication technology. Obtained results show that the parallelization of electrical simulations in 6 cores simultaneously saved more than 14 hours of optimization time.

Keywords—automatic analog design, CAD tool, parallelization.

I. INTRODUCTION

The design automation of analog integrated circuits can be very useful in microelectronics, because it provides an efficient search in the design space, among a set of design constraints, to make it more efficient as possible. Several works have been done in this theme, aiming the development of tools for the automation of time-consuming tasks and complex searches in highly non-linear design spaces [3-6]. An important improvement in the analog design could be the automation of some design stages, such as transistor sizing and layout generation [5], maintaining the interaction with the human designer. The large number of design variables and the consequent large design space turn this task extremely difficult to perform even for most advanced computational systems. Therefore, it is mandatory the use of artificial intelligence with great computational power to solve these problems.

The estimation of circuit specifications is necessary in order to evaluate each generated solution and to explore the design space. This task can be done manually using simplified equations - like spice Level 3 quadratic model - that describe the transistors size in terms of the circuit specifications. Due to equations simplicity, results may not describe the real circuit behavior. Another characteristic is that in these equations, in general, the transistors are operating in strong inversion region, limiting the design space exploration, which is not suitable for low power design.

In order to solve this task and to explore the entire circuit

design space, it is necessary to use a device model that is able to characterize all operation regions, like BSIM4. Also, finding optimized feasible solutions (solutions that reach design constraints) with artificial intelligence heuristics, such as simulated annealing, can be a good alternative.

According to [4], in an automatic sizing tool, specification estimation is the step that consumes more computational time. The evaluation of spice electrical simulations at each iteration contribute for this large computational time, allied to the fact that the number of iterations is usually in the order of thousands in a typical analog optimization process [7].

Another important characteristic is that different electrical simulations in the same iteration are not dependent on each other. Therefore, the electrical characterization is a candidate to be executed in parallel.

In this context, this paper proposes a set of circuit characterization configurations, using electrical simulations, for automatic design of operational amplifiers. These configurations consist of standard simulation testbenches and simulator interfaces for evaluating circuit characteristics. These test benches are implemented in the UCAF tool [7] and are suitable for parallel execution.

As results, this paper presents an OTA Miller design in TSMC 0.25 μ m technology implemented using the UCAF tool with the presented method for circuit characterization. Parallel electrical simulation is explored in order to evaluate total optimization time reduction.

The rest of this paper is organized as follows: section 2 shows the description of UCAF tool; section 3 discusses the circuit characterization method; section 4 shows the results of the OTA Miller design; and section 5 presents some conclusions.

II. UCAF ANALOG INTEGRATED CIRCUIT SIZING TOOL

The implementation of this work is based on the UCAF tool [7]. This tool was implemented in Matlab® and uses artificial intelligence to explore the design space in order to find optimized solutions. These solutions should satisfy some design constraints and to optimize some design specifications, such as power dissipation and gate area minimization. The design methodology of the UCAF tool is based on the design flow

shown in Fig. 1. The inputs of the tool are an initial solution for the circuit, design specifications (constraints and goals) and the fabrication technology parameters. Based in these inputs the optimization methodology, like simulated annealing meta-heuristics, provides values for the circuit variables. These values are design possible solutions. Circuit variables in the sizing process are the transistor channel length (L) and width (W) and the voltages or currents source bias. Each possible solution is evaluated based on the circuit specifications. Based on this evaluation the optimization method exploits the design space to find optimized solutions.

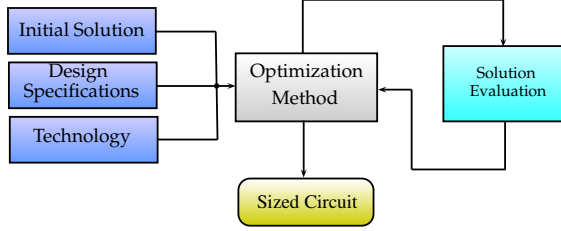


Fig. 1. The design methodology of the UCAF tool.

In the UCAF tool, the solution evaluation is made by means of a cost function, shown in Eq. 1. The first sum represents the objective part of the cost function and the second sum is the constraints part.

$$f_c = \sum_{i=1}^n P_{O_i} \cdot S_i + \sum_{j=1}^n P_{R_j} \cdot f(S_j) \quad (1)$$

S_i is the i^{th} specification of the circuit to be optimized and S_j is the j^{th} specification of the circuit that is constrained in a maximum or minimum value. P_{O_i} and P_{R_j} are values used as weighting purpose. $f(S_j)$ is the constraint function used to measure the distance between the required value and the reached value for the specifications.

The more important part of the solution evaluation is the specification estimation, because the metric to the heuristic design exploration is the values of the specifications. Fig. 2 shows the flow of the specification estimation. The optimization method generates a solution (values for circuit variables). Based on this solution, it is necessary to evaluate the cost function, which is estimated using the specification results generated by circuit characterization. These estimations are made using electrical simulations with specific circuit testbenches. An example is the open loop configuration for voltage gain simulation.

The extraction of the specification from the simulation output is can also be done automatically. Fig. 2 shows the AC simulation result in a Bode diagram, in which the extraction function can obtain the low frequency voltage gain (A_{v0}), the gain-bandwidth product (GBW) and the phase margin. It is necessary to perform electrical simulation and specification extraction for each testbench in order to measure the required specification. This task is executed several times in the optimization process.

Most execution time is spent in the circuit characterization. In Fig. 2 it is possible to see that all the specification are dependent of the generated solution and independent on each other. It allows the execution of all circuit simulations in each iteration in parallel form.

III. CIRCUIT CHARACTERIZATION

This work proposes measuring functions for automatically extracting operational amplifier specifications using standard testbenches presented in [1] and [2].

Several circuit configurations are used to measure the design specifications. In this work, the circuit specification estimation is made through the HSpice® electrical simulator performing AC, DC and Transient analysis using a Matlab interface. Fig. 3 shows the standard testbenches that are used in UCAF tool.

To measure the low-frequency gain (A_{v0}), the gain-bandwidth product (GBW) and the phase margin (PM) an AC analysis is performed. The configuration used for this measure is shown on the Fig. 3(a). The results of this simulation can be plotted as a Bode diagram. From the gain curve of this diagram, A_{v0} and GBW specifications are extracted. In the same way, the phase margin is obtained in the phase curve, as shown in Fig. 4.

To obtain the Input Common Mode Range (ICMR) the amplifier is connected in unity gain configuration, as shown in Fig. 3(b). In this simulation the input voltage is varied from a minimum to a maximum level through a DC analysis. Positive and negative values are obtained from simulation output when the gain is linear.

Fig. 3(c) shows a circuit with a voltage gain of -10 . This circuit is used to measure the output swing (OS) with a DC analysis of input voltage sweep. As the gain is -10 the output level of saturation is obtained. The difference between the minimum and maximum output levels are the OS specification.

To measure the response speed of an amplifier (Slew Rate) the same configuration of ICMR is used. However, the goal of this simulation is the analysis of a step response of the circuit through the verification of the output voltage level in a transient analysis.

The common-mode rejection ratio (CMRR) is given by the ratio of the common voltage (V_{cm}) by the generated output voltage. This specification represents the rejection amount of the input common-mode voltage due to the non-idealities of the amplifier. To measure this specification, an AC analysis is executed using the configuration shown on Fig. 3(e), varying the operation frequency of the common-mode voltage source.

Like the CMRR, the power supply rejection ratio (PSRR) indicates the amplifier rejection capacity in relation to the noise coming from the power supply of the circuit. The circuit used to measure the PSRR is shown in Fig. 3(f). The noise comes in two ways: from the V_{DD} and from V_{SS} power supplies, resulting in positive (PSRR+) and a negative (PSRR-) rejection ratio, respectively. An AC analysis is executed to sweep the frequency of the voltage sources, simulating the noise coming from the power supplies. It is important to notice that these two simulations are performed separately.

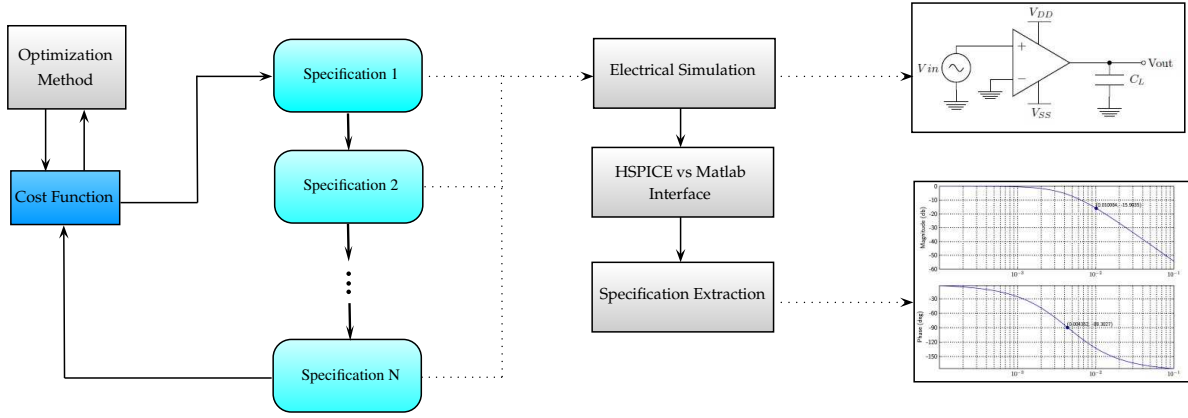


Fig. 2. Automatic Characterization Flow.

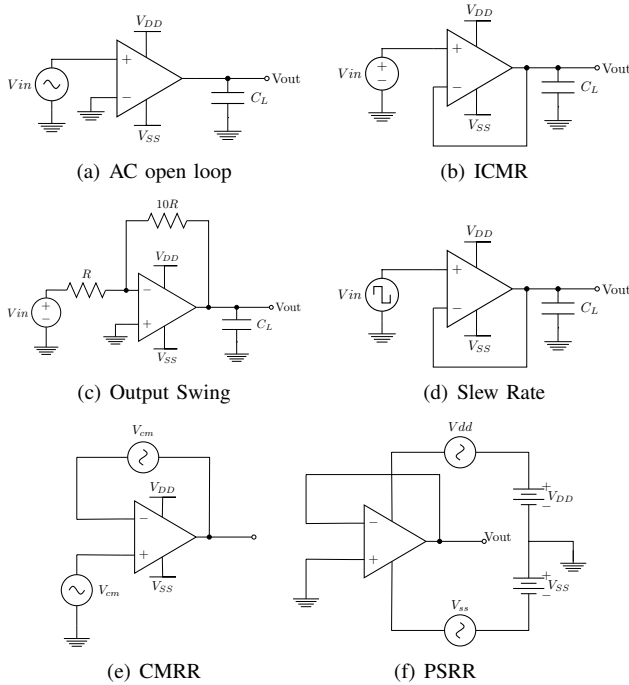


Fig. 3. Implemented testbenches.

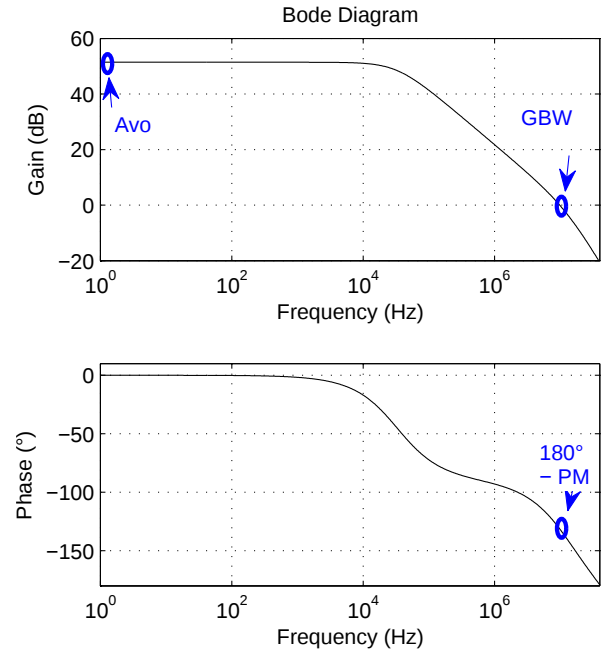


Fig. 4. Bode diagram used to estimate low-frequency gain (A_{v0}), gain-bandwidth product (GBW) and phase margin (PM).

With the a multi-core computer archtechture, the electrical simulation task can be done simultaneously in different processors, since each specification has an independent testbench.

IV. DESIGN ANALYSIS

As an example of using the proposed characterization method, the design of a two-stage CMOS Miller operational transconductance amplifier (OTA) in $0.25\mu\text{m}$ TSMC technology is presented. The schematics of this amplifier is shown in Fig. 5. The Miller OTA is composed by an input differential pair and a current mirror with active load in the first stage. The second stage is composed by an inverter amplifier. Between the first and second stages is connected a compensation capacitor for stability purposes [1]. This design has 12 design free

variables: $W1$, $L1$, $W3$, $L3$, $W5$, $L5$, $W6$, $L6$, $W7$, $L7$, I_B and C_C . The UCAF tool is executed in a Intel core i7 processor with eight physical cores and 8GB of memory. Simulated Annealing algorithm is defined as the optimization heuristic. The required specification values are shown in the second column of the Tab. I. Power dissipation is set as design objective and the remaining specifications are design constraints. The results of the execution in a single processor core is shown in the third column of that table I. These results show that all constraints are met and the power dissipation for the circuit is optimized to $744,5 \mu\text{W}$. The execution time is equal to 1194 minutes.

To analyze the influence of parallel execution in the op-

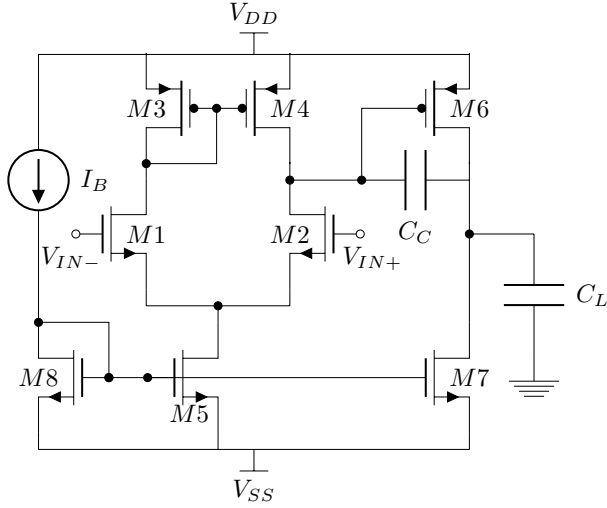


Fig. 5. CMOS OTA Miller schematic.

TABLE I
SPECIFICATIONS OF OTA MILLER DESIGN

Specifications	Required Value	Obtained Value
A_{v0} (dB)	≥ 70.00	81.62
GBW (MHz)	≥ 2.00	2.67
PM ($^{\circ}$)	≥ 50.00	78.01
OS (V)	≥ 2.00	2.33
CMRR (dB)	≥ 70.00	78.58
PSRR+ (dB)	≥ 70.00	84.61
PSRR- (dB)	≥ 70.00	80.60
SR (V/ μ s)	≥ 1.50	4.35
P_{diss} (μ W)	Minimize	744.50
Execution Time (min)	-	1194

timization process, the previous design was repeated using parallel simulations. For this analysis the number of cores (workers) was set in 1, 2, 3, 4 and 6. As this design needs a maximum of 6 simulations in each iteration, the maximum number of cores for parallel optimization is 6. The results of parallel execution are shown in Tab. II. These results demonstrate that parallel execution provides important reduction in the execution time. The faster execution time is 308 minutes, with 6 cores, which gives a speed up of 3.88 in relation to the single core execution time. The saved time, equivalent to more than 14 hours, is extremely relevant and demonstrate that this kind of optimization procedure is highly parallelized.

TABLE II
EXECUTION TIME AND SPEEDUP OF THE PARALLEL SIMULATIONS

Cores	Execution Time(min)	Speed up
1	1194	-
2	616	1.94
3	539	2.22
4	447	2.67
6	308	3.88

V. CONCLUSION

The proposed method for operational amplifier automatic characterization presented good results when included in an automatic sizing tool. As electrical simulations in each optimization iteration are independent, they can be executed in parallel. Execution time is reduced up to 3.88 times in relation to the sequential version, saving more than 14 hours in the optimization design space exploration time, while keeping the near the same number of iterations. As future work, we intend to insert new testbenches in the simulation environment in order to measure different circuit specifications and to expand the methodology to other analog circuits.

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