

Power Optimization of FIR Filters through the Coefficients Reordering using Anedma Heuristic

João G. Rahmeier
UNIPAMPA
Alegrete, RS, Brazil
joao.nizer@gmail.com

Ângelo G. Luz
SENAC
Pelotas, RS, Brazil
angelogl@gmail.com

Sidinei Ghissoni
UNIPAMPA
Alegrete, RS, Brazil
sidineighissoni@unipampa.edu.br

Eduardo A. Costa
UCPEL
Pelotas, RS, Brazil
ecosta@ucpel.tche.br

Abstract—The main goal of this paper is the power optimization in different FIR filters after the ordering of coefficients from a heuristic algorithm named Anedma. Due to the characteristics of these filters, which involve multiplications of input value with appropriate coefficients, the best ordering of these operations can contribute for the reduction of the switching activity, what leads to the minimization of power consumption. The filters were synthesized in 350 and 180 nm XFAB technologies using SYNOPSIS tools, the power estimation was realized at logic level for both sinusoidal and random vectors. The results showed that it is possible to achieve power reduction of up to 4.93% on average after reordering the coefficients.

Keywords—Power optimization, FIR filters, Anedma heuristic.

I. INTRODUCTION

Power consumption in digital signal processing (DSP) systems has gained special attention along the years, mainly due to the proliferation of high-performance portable battery-powered electronic devices. In DSP applications, one of the most basic operations are FIR (Finite Impulse Response) filter computations [1], [2].

In the FIR filter operation, each tap involves getting the appropriate coefficient and data values and performing a multiply-accumulate computation. The larger the number of taps, the more definition we can have on the transfer function implemented by the filter. In FIR filter computation, the summation operation is both commutative and associative, and the filter output is independent of the order of computing the coefficient product. Thus, coefficient ordering has been used as a technique for low power, where all coefficients are ordered in a Fully-Sequential circuit to minimize the transitions in the multiplier input and data bus [3], [4].

Although the techniques presented in [3] and [4] can optimize the ordering of the coefficients, the cost function of the algorithms is calculated for all the combinations over the coefficients, which is limited to a small group of coefficients, where the total number of permutations is calculated in a still reasonable time. However, for a larger number of coefficients, these exhaustive algorithms are less attractive due to the time required to process a higher number of combinations.

In this paper, we use the Anedma heuristic-based algorithms [5] in order to search the best ordering of the coefficients for the power reduction of larger instances of sequential FIR filter architectures.

Although the Anedma algorithm has been used before for the purpose of reducing the Hamming distance between consecutive coefficients in FIR filters [5], for the first time we have observed the impact on reducing power consumption of the FIR filters in two different technologies (350nm and 180nm) by using a commercial tool.

The main results show that depending on the set of coefficients used, based on the guidance given by the Anedma heuristic algorithms, the power consumption of the FIR filter architectures can be reduced significantly.

The present paper is organized as follows. Section II we discuss the FIR filter realization. Section III presents the background concepts of Anedma heuristic. The Experimental results are presented in Section IV, and finally, the paper is concluded in Section V.

II. FIR FILTER REALIZATION

In FIR filter design, a set of coefficients is used in order to perform the FIR filter computations. These coefficients represent values between -1 and 1 in fixed-point representation. The coefficients are computed for a desired frequency response of the FIR filter.

A. FIR Filter Characteristics

FIR filtering is achieved by convolving the input data samples with the desired unit impulse response of the filter. The output $Y[n]$ of an N -tap FIR filter is given by the weighted sum of the latest N input data samples $X[n]$ as shown in Eq.(1).

$$Y[n] = \sum_{i=0}^{N-1} X[n-i]H[i] \quad (1)$$

The Discrete Fourier Transform (DFT) of the required frequency transfer function and some known windowing method obtains the coefficients of the FIR filter (represented by H in Eq.(1).

B. Coefficient Manipulation

In the FIR filter operation, the output is performed by a summation of data-coefficient products, as observed in Eq.(1). Coefficient ordering can be used as a technique for low power because in a FIR filter computation, the summation operation

is both commutative and associative, and the filter output is independent of the order of computing the coefficient product, as can be observed in Eq.(2) and Eq.(3) for a 4th order filter example.

$$Y_n = A_0X_n + A_1X_{n-1} + A_2X_{n-2} + A_3X_{n-3} \quad (2)$$

$$Y_n = A_1X_{n-1} + A_3X_{n-3} + A_0X_n + A_2X_{n-2} \quad (3)$$

In the manipulation of coefficients, the problem is related to find the best ordering for each coefficient by calculating the minimum Hamming distance between consecutive coefficients. In the algorithm presented by [4], the cost function is calculated for all the combinations over the coefficients. As the number of taps was small (eight) the number of permutations was still reasonable. However, for a larger number of coefficients this exhaustive algorithm is less attractive due to the time necessary to process the large number of combinations. Thus, in our work the Anedma heuristic-based algorithms is used in order to get as near as possible the optimal solution for the ordering of a larger number of coefficients.

C. FIR Filter Datapath

In the Direct Form FIR filter implementation, based on Eq.(1), in each clock cycle a new data sample and the corresponding filter coefficient are simultaneously applied to each multiplier. The results of all multipliers are added simultaneously. In our work, we address the implementation of Fully-Sequential architecture. This architecture is a manner to reduce hardware requirements for the FIR filter algorithm. In the sequential implementation the basic idea is to reduce hardware requirements by re-using the hardware as much as possible.

The implemented filters are 16-bit width of input resolution. The set of the used filters are based on [6], where the choice of the set of coefficients is based on the gain curve, the ripple in the passband and a better performance in the stopband.

The structural circuits for original and ordered filters were automatically generated in .BLIF (Berkeley Logic Interchange Format) and converted to .SV (SystemVerilog). It occurred because the original filters had been already described in BLIF format [7]. The arithmetic operators are described in order to obtain a low power consumption, as proposed in [7].

In the sequential implementation a set of multiply-and-add (MAC) operations is performed for each sample of the input data signal, multiplying the N delayed input samples by coefficients and summing up the results together to generate the output signal. The circuit consists on control unit, two multiplexers for selecting both the coefficients and input data, two banks of registers for storing coefficients and inputs, a logical 16-bit multiplier, a 32-bits adder and a 32-bits accumulator register. A block diagram of the filters described is shown in Fig. 1.

Control unit is responsible for selecting the entries and the respective coefficients to perform the multiplications, as well

as cleaning the register accumulator after the output has been stable. The two multiplexers are controlled in order to make available to the multiplier input values and a corresponding coefficient. The multiplications are performed in two's complement. The multiplication result is made available at the input of the 32 bit adder and it is added with the value stored in the accumulator register. The accumulator register with the adder constitutes the weighted sum of Eq. (1), and therefore, at every N -sum the accumulator register is reset by the control system.

We have implemented and analyzed different type of band-pass (BP), band-stop (BS), low-pass (LP) and high-pass (HP) filters with order N equal to 30 and 50.

III. ANEDMA HEURISTIC

This heuristic was created after to observe the feature of the FIR filter coefficients, where usually has several candidates with the same Hamming distance (the lower possible to a given coefficient in analysis). Then, using this heuristic the purpose is that a coefficient which has N candidates with the same Hamming distance to be chosen as a neighbor, make the choice of the lowest important coefficient for the others neighbors, thus making it possible to achieve better results. In this heuristic, N threads are started and each one produces an ordering resulting from the application of the algorithm using a random point as initial element.

When analyzing the Hamming distance between the coefficient in analyze and all the others filters, all coefficients that have the same Hamming distance value that the best candidate, at the end of the search are inserted in a list with the best candidates to this coefficient. If the size of this list is greater than 1, the elements are still available to be selected by other coefficients. However, if the size is one, this unique element is inserted in other list, which name is the list of locked coefficients, guarantying that at least one of the best elements be selected. Then in each search, before inserting a given element in the candidate list, it is verified if this element is no longer inserted in the locked list. For example, when an element has four candidates with the same Hamming distance with respect to a certain coefficient in analysis, instead of staying with any one at random, it gets the least significant for the other coefficients and thereby achieves better solutions.

IV. RESULTS

In this section, we present the results obtained after the coefficients reordering process. Firstly, the filters were described in SystemVerilog and the functional verification in

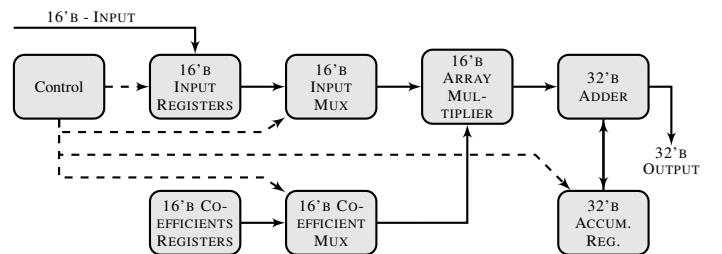


Figure 1: Schematic for FIR filters datapath.

Table I: Power Results - 30c and 50c Filters - Sinusoidal Vectors

FILTER		180nm						350nm							
		POWER (mW)			PERC. REDUCTION (%)			POWER (mW)			PERC. REDUCTION (%)				
		SWTG	INT	TOTAL	SWTG	INT	TOTAL	SWTG	INT	TOTAL	SWTG	INT	TOTAL		
30C	BAND STOP 1	0.777	5.224	6.002				8.574	46.0	54.574					
	BAND STOP 1 - ANEDMA	0.705	5.124	5.829	−9.32	−1.91	−2.87	7.655	44.7	52.355	−10.72	−2.83	−4.07		
	HIGH PASS 1	0.653	5.067	5.721				7.195	43.6	50.795					
	HIGH PASS 1 - ANEDMA	0.544	4.880	5.425	−16.72	−3.69	−5.18	5.830	41.6	47.430	−18.97	−4.59	−6.62		
	LOW PASS 2	0.935	5.391	6.327				10.30	48.5	58.800					
	LOW PASS 2 - ANEDMA	0.829	5.273	6.103	−11.30	−2.19	−3.54	8.998	46.7	55.698	−12.64	−3.71	−5.28		
50C	BAND PASS 1	0.884	7.506	8.390				9.699	64.1	73.799					
	BAND PASS 1 - ANEDMA	0.795	7.391	8.187	−9.97	−1.53	−2.42	7.168	61.0	68.168	−26.10	−4.84	−7.63		
	HIGH PASS 2	0.901	7.520	8.422				8.372	62.7	71.072					
	HIGH PASS 2 - ANEDMA	0.816	7.418	8.235	−9.45	−1.36	−2.22	7.383	61.4	68.783	−11.81	−2.07	−3.22		
	LOW PASS 1	0.709	7.285	7.995				6.324	59.6	65.924					
	LOW PASS 1 - ANEDMA	0.654	7.194	7.849	−7.75	−1.25	−1.83	5.607	58.5	64.107	−11.34	−1.85	−2.76		
AVERAGE REDUCTION					−10.75	−1.99	−3.01						−15.26	−3.31	−4.93

Table II: Power Results - 30c and 50c Filters - Random Vectors

FILTER		180nm						350nm							
		POWER (mW)			PERC. REDUCTION (%)			POWER (mW)			PERC. REDUCTION (%)				
		SWTG	INT	TOTAL	SWTG	INT	TOTAL	SWTG	INT	TOTAL	SWTG	INT	TOTAL		
30C	BAND STOP 1	0.994	5.546	6.540	−6.88	−1.19	−2.06	10.700	49.8	60.500	−7.44	−2.21	−3.13		
	BAND STOP 1 - ANEDMA	0.925	5.480	6.406				9.904	48.7	58.604					
	HIGH PASS 1	0.862	5.382	6.244	−9.29	−2.40	−3.35	9.221	47.2	56.421	−10.41	−3.18	−4.36		
	HIGH PASS 1 - ANEDMA	0.782	5.253	6.035				8.261	45.7	53.961					
	LOW PASS 2	1.163	5.717	6.880	−8.60	−1.42	−2.63	12.600	52.4	65.000	−9.52	−2.67	−4.00		
	LOW PASS 2 - ANEDMA	1.063	5.636	6.699				11.400	51.0	62.400					
50C	BAND PASS 1	1.099	7.823	8.922	−8.37	−1.09	−1.98	11.800	67.9	79.700	−20.71	−4.71	−7.08		
	BAND PASS 1 - ANEDMA	1.007	7.738	8.745				9.356	64.7	74.056					
	HIGH PASS 2	1.162	7.903	9.065	−7.57	−0.97	−1.82	11.000	66.7	77.700	−8.18	−4.71	−7.08		
	HIGH PASS 2 - ANEDMA	1.074	7.826	8.900				10.100	65.8	75.900					
	LOW PASS 1	0.976	7.692	8.668	−5.41	−0.87	−1.38	9.036	63.8	72.836	−6.50	−1.41	−2.04		
	LOW PASS 1 - ANEDMA	0.923	7.625	8.548				8.449	62.9	71.349					
AVERAGE REDUCTION					−7.69	−1.32	−2.20						−10.46	−2.59	−3.82

VCS[®]Synopsys tool was realized based on methodology proposed in [8].

The circuits were synthesized at logic level for XFAB 350nm and 180 nm technologies. The synthesis was performed using the tool Design Compiler[®]from Synopsys. All the simulations were limited by the path delay of the circuits provided by the tool. Thus, the clock frequencies used were 16.5MHz and 15.3MHz for filters with 30 and 50 coefficients, respectively.

Using Synopsys PrimeTime[®]and two sets of 10.000 vectors we estimated the power consumption. As the type of vector has a great influence on power consumption [7], we have presented the results for two type of signals input, i.e., sinusoidal and randomly generated by Matlab[®].

We have observed by the results presented in Tab. I and II, that using Anedma heuristic, all the filters have reduced both switching and internal cell power. The reduction of switching power occurs because it refers to the power dissipated in the output capacitances, according to the frequency of transition into the cell. Thus, the decrease of switching activity caused by the reordering of the coefficients provides a large percentage reduction for this power component. The average percentage reduction was 10.75% and 7.69% for sinusoidal and random vectors respectively.

The reduction of the switching activity also contributes for

the reduction of the internal cell power, because it is dissipated in the charge and discharge of any internal capacitance of the cell and in the short-circuit current during switching transient. However, as the clock network is responsible by the most part of this power consumption, and it is the same for the original and ordered filters, the percentage power reduction caused by coefficient reordering is lesser. Thus, the average percentage reduction was 1.99% and 1.32% for sinusoidal and random vectors respectively.

We have also presented graphical results for sinusoidal and random signals input. The comparisons can be observed in Fig. 2 and 3, where the total power (top value) composed by switching and internal cell power (bottom value) for both set of vectors are presented. Analyzing those figures it is possible to notice that using sinusoidal vectors the filter presented lesser power consumption. This is due to the fact in the sinusoidal vectors increase the correlation between the input data is increased, what impact on the reduction of Hamming distance between the input data. We may also noticed that the use of smaller technology caused the decrease of power consumption due to its own characteristics as low voltage and features for low power.

Area results were not presented but it was almost the same for both filters, due the modifications in filter datapath just change the order that coefficients are provided to the multiplier. So, it is not substantially changed the total area of the design.

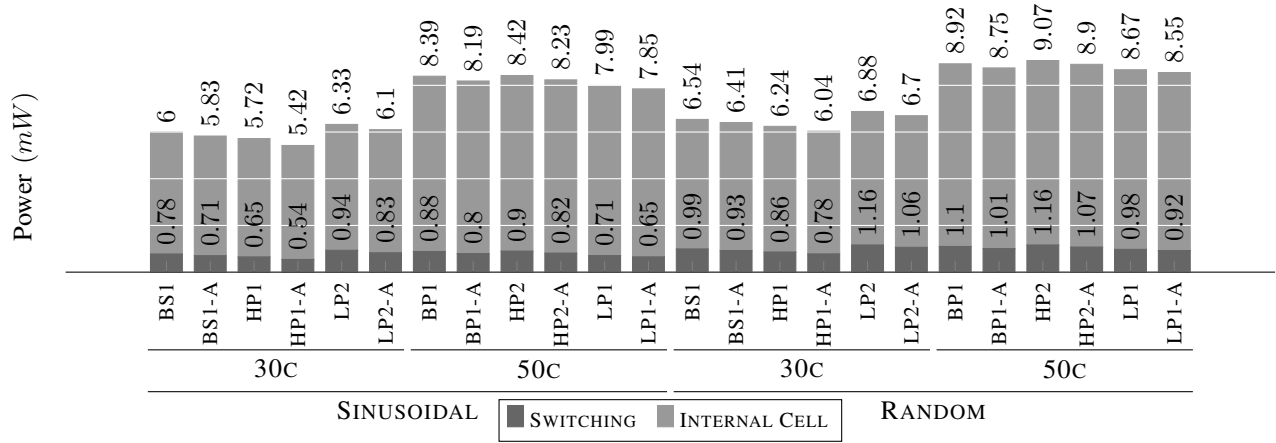


Figure 2: Power results of filters in 180nm with sinusoidal and random vectors.

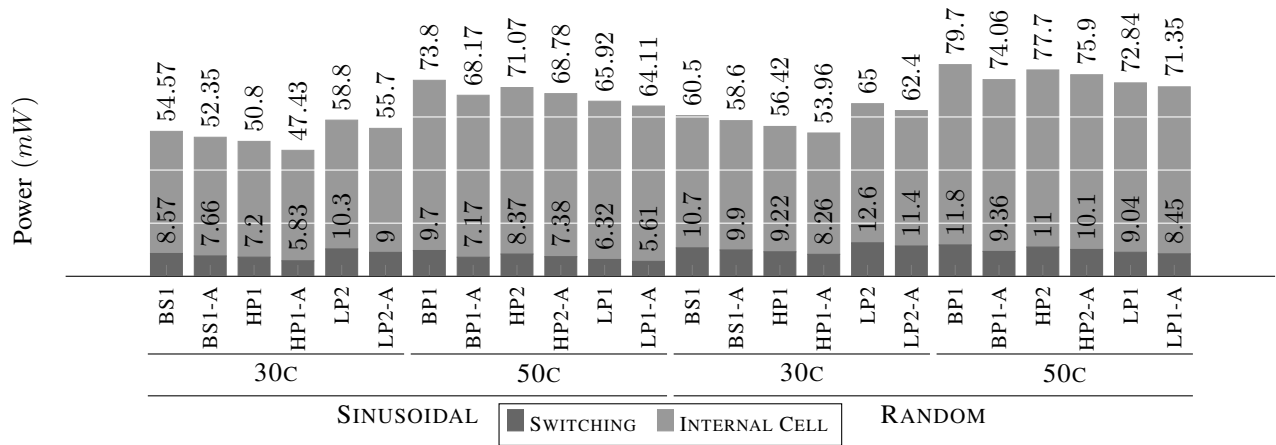


Figure 3: Power results of filters in 350nm with sinusoidal and random vectors.

V. CONCLUSION

In this work the ANEDMA heuristic algorithm was explored for the ordering of FIR filter coefficients. The efficiency of the Anedma algorithm could be proved, because after the reordering of the coefficients, the power consumption of different set of FIR filter could be reduced. As expected the power switching presented the largest power percentage reduction. However, when the absolute values is taken into account, the internal cell power has contributed more to the reduction of the total power of the filters. Therefore, it was possible to conclude that since the set with more correlation between the coefficients is more favorable for the ordering of the coefficients, significant power reduction in the filters can be achievable.

Although our method has been implemented in Filters FIR architectures, we are convinced that it can also be naturally applied to other architecture, as FFT and DCT and will be tested as future work.

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