Aging Effects Analysis in Flip-Flops

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Abstract — This work presents a methodology to analyze aging effects in different flip-flops topologies. As CMOS transistor scaling to nanometer technologies in the last decades, new issues have become major concerns in VLSI design. One of those new issues is aging. Aging effects impact on performance and reliability of CMOS circuits. Flip-flops are one of the main structures in VLSI circuits. Their characteristics impact directly on circuit clock frequency, being also responsible for a large portion of the circuit power consumption. Experimental results show the impact of aging effects in three different FF topologies. An increment up to 15% in delay has been verified.

***Keywords*— Flip-flops, aging effects, BTI, HCI, TDDB, digital circuits, CMOS.**

I. INTRODUCTION

VLSI circuits design has become more challenging with the reduction of devices dimensions. New undesired effects, such as leakage currents, process variability, and radiation have to be overcome to ensure high performance, reliability and low power in digital circuits. Another important effect is related to the wearout mechanisms that cause the transistors aging.

The three main effects associated to aging of the circuits are: time dependent dielectric breakdown (TDDB), bias temperature instability (BTI) and hot carrier injection (HCI). BTI leads to a degradation of the transistor threshold voltage, thus reducing circuit performance [1]. TDDB, on the other hand, is linked to the creation of a conduction path through the gate transistor structure. This conduction path causes a significant increment in power consumption and also affects the circuit delay [2]. HCI, in turn, is caused by a high current in the transistor channel, during the switching, injecting some charges into the gate oxide. HCI also leads to a shift in the transistor threshold voltage [3].

Aging effects impact on performance and reliability of CMOS circuits have been extensively explored in the last years, mainly for combinational circuits [4–6]. In flip-flops (FFs), the aging effects impact on the timing characteristics, such as setup time, hold time and the propagation delay. It may cause major damage to the circuit, since FFs are directly related to maximum circuit clock frequency [7]. Moreover, by being connected to clock tree, FFs have great contribution to the circuit power consumption [8,9]. Related works are more focused in BTI impact in FFs [10-13]. In [10], it is proposed a comparative analysis of four FFs topologies. Particular architecture to run-time failure prediction is suggested in [11]. In [12] and in [13], design techniques are approached to reduce the impact of the BTI effect, proposing dual threshold assignment and suggesting a selective transistor-level sizing, respectively. No relevant work analyzing TDDB and HCI in FF has been found in literature.

In this work, it is proposed an aging analysis of FFs, considering HCI, BTI and TDDB effects. The model used to evaluate aging effects in combinational circuits, proposed by Butzen *et al.* [14], has been exploited herein to application on different FF topologies. More specifically, FFs are characterized under aging impact, and their timing characteristics are compared to identify their aging robustness.

This paper is organized as follows. In Section II, there is a brief review of FF properties and timing characteristics. The aging effects are also reviewed in Section II, focusing in how to identify the stress condition in transistor arrangements. In Section III, the proposed method of analysis is discussed. Section IV presents and discusses the results. Finally, in Section V, the final considerations are presented.

II. BACKGROUND

For a better understanding of this work, some essential concepts are reviewed. In the first part, the timing characteristics of FFs are explored. A discussion about aging effects in CMOS transistors is performed in the second part of this section.

A. Flip-Flops

Flip-flops are one of the main structures in VLSI circuits, since their time characteristics affect the performance of the whole circuit. Therefore, time constraints as setup and hold time and propagation delay need particular attention. The propagation delay Clock-to-Q, T_{CQ}, is minimum when the input data arrives long before the clock edge.

One way to characterize the delay of a FF is through the time period between the arrival of input data (D) and changing on the output value (Q), named T_{DQ}. According to [15], T_{DQ} is taken as FF delay.

T_{DQ} minimum, $T_{DQ,min}$, is achieved by selecting the optimum setup skew. The setup time, $T_{setup,}$ is the optimum setup skew which leads to $T_{DQ,min}$. For the optimum setup skew, T_{CQ} is higher than $T_{CQ,min}$, because for small values of setup skew the FF works in the metastability region [16]. The hold time, T_{hold}, is the hold skew which leads to an increase of 5% in the T_{CQ}[17].

The definitions presented are formalized as follows [15,17,18]:

1) Setup skew: time interval between a transition of the input data before the clock edge and the clock edge.

2) T_{setup}: time constraint; the smallest setup skew allowed.

3) Hold skew: time interval between a transition of the input data after the clock edge and the clock edge.

4) T_{hold}: time constraint, the smallest hold skew allowed.

5) T_{CQ}: Propagation delay from clock edge to the output Q transition, assuming there was no setup time violation.

6) T_{DQ}: time period between input data arrival and output Q transition; T_{DQ} may be defined as :

$$T_{DQ} = T_{CQ} + setup\ skew \quad (1)$$

If $setup\ skew = T_{setup}$, then $T_{DQ} = T_{DQ,min.}$

B. Aging Effects

The aging effects are resulted from a superposition of many individual complex physical processes. Although there is no single physical mechanism that is comprehensive enough to explain all the details related to the transistor degradation, its electrical characteristics more affected by each effect is well established [19]. The transistor severe degradation conditions are also well known [20]. In terms of circuit construction, these two factors are quite relevant to find the most appropriate design solutions.

BTI and TDDB are wearout mechanisms that degrade the transistor when it is in static state. Whereas BTI increases the transistor threshold voltage, so reducing the circuit speed, TDDB degrades the isolation properties of gate dielectric, increasing the tunneling current across the transistor gate terminal. The stress condition associated to those effects is similar, and occurs when the gate voltage of PMOS and NMOS transistors are, respectively, V_g='0' and V_g='1', and gate-to-source voltages are $V_{gs} = -V_{dd}$ and $V_{gs} = +V_{dd}$, as shown in Fig. 1(a) and Fig. 1(b). In the circuit analysis, such stress condition is directly related to the gate signal probability. The transistor arrangement has to be also considered due to the V_{gs} dependence. Several works compute the degradation using only the gate signal probability [1,21]. To achieve more accurate results, this work explores the methodology proposed in [14], that considers both gate signal probability and the transistor arrangement. The concept of transistor stress probability (*TSP*) is introduced in that work. Basically, it is computed by a procedure that identify the transistor stress conditions, as illustrated in Fig. 1(a) and Fig. 1(b), in any transistor network taking into account the signal probability and the device arrangement.

On the other hand, differently from BTI and TDDB, HCI degrades the transistor when it is switching. HCI increases the transistor threshold voltage [3]. Since this phenomenon is associated to carriers flowing through the transistor channel, the higher mobility of electrons, when compared to holes, turn the NMOS devices more susceptible to HCI effect than the PMOS ones. The degradation in NMOS occurs when a rise transition on the gate causes a fall transition into the drain region, as illustrated in Fig. 1(c). The severity of HCI degradation is exponentially related to the transistor drain-to-source voltage (V_{ds}) [14]. Since the transistors connected to the output node are the ones that experience maximum V_{ds}, the gate signal switching information is not enough to compute properly the degradation. The transistor arrangement has to be included in the analysis. The transistor switching stress probability (*TSwP*) considered in this work follows the methodology proposed in [14]. *TSwP* is computed by a procedure that identifies as degraded devices only the switching transistors that experience maximum V_{ds}.

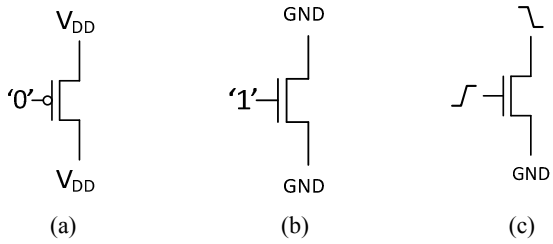

Fig. 1- Transistor under BTI stress in PMOS (a) and NMOS (b), and under HCI stress (c).

III. METHODOLOGY

Aging analysis in sequential circuit differs from combinational one mainly due to the existence of the memorization capacity in internal nodes. Whereas in combinational circuits it is possible find out the logical value in all the circuit nodes only based on the input values, in sequential structures there are unreachable nodes. The voltage value of such unreachable nodes is usually defined by previous state values, so increasing the complexity of the estimation method. The identification of memorization nodes and the computation of all possible combinations are the key factors to provide a more accurate analysis of FF aging robustness. That is the major contribution of this work.

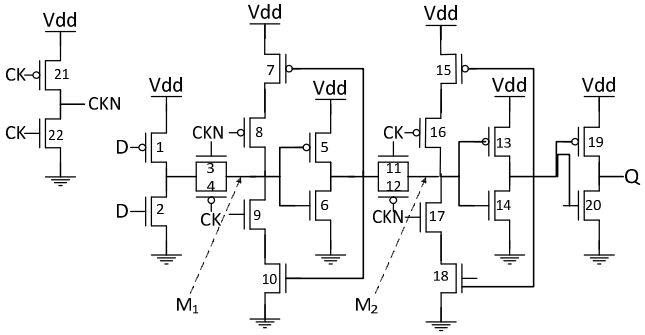

Fig. 2 - Transmission gate flip-flop (TGFF) [18].

Let's take as our case of study the transmission gate flip-flop (TGFF), depicted in Fig. 2 [22], to describe the aging analysis proposed herein. Initially, the first step is to calculate *TSP* and *TSwP* of each device in the circuit. It is evaluated considering all 'D' and 'CK' input signal possibilities, and the values of 'M1' and 'M2' memory nodes, indicated in Fig. 2. It

corresponds to eight combinations for static analysis and sixteen possibilities for switching conditions. *TSP* and *TSwP* values are shown in Table I.

TABLE I - STRESS PROBABILITY VALUES ON DEVICES IN FIG. 2.

Xtor	*TSP*	*TSwP*	Xtor	*TSP*	*TSwP*
1	0.5	0	12	0.25	0
2	0.5	0.25	13	0.5	0
3	0.25	0.125	14	0.5	0.0625
4	0.25	0	15	0.5	0
5	0.5	0	16	0.25	0
6	0.5	0.1875	17	0.25	0
7	0.5	0	18	0.5	0
8	0.25	0	19	0.5	0
9	0.25	0	20	0.5	0.0625
10	0.5	0	21	0.5	0
11	0.25	0.125	22	0.5	0.25

Then, in the second step, the threshold voltage degradation (ΔV_{th}) of each transistor (Xtor) and resistor (R_{GD}) are computed according to the stress probabilities presented in Table I. ΔV_{th} is resulted from the aging effects BTI and HCI. The maximum degradation of 50mV is taken into account for a 32nm technology. This value reflects five years degradation in nanometer technologies [20]. ΔV_{th} is calculated by the following equation:

$$\Delta V_{th} = a \,.\, (TSP \,.\, t)^n + b \,.\, (TSwP \,.\, t)^m \qquad (2)$$

where '*a*' and '*b*' are technology dependent constants, '*t*' is time, '*n*' is the BTI time exponential constant, and '*m*' is the HCI time exponential constant.

The resistors R_{GD} between gate and drain terminals can be used to emulate the gate tunnelling current increment caused by the TDDB effect [2]. Resistor R_{GD} is obtained by the following equation:

$$R_{GD} = K \,.\, (TSP \,.\, t)^p \qquad (3)$$

where '*t*' is time, whereas '*K*' and '*p*' are technology dependent constants. The computed R_{GD} values and ΔV_{th} of each transistor are shown in Table II.

TABLE II - THRESHOLD VOLTAGE DEGRADATION AND GATE-TO-DRAIN RESISTANCE ON DEVICES IN FIG. 2.

Xtor	ΔV_{th}(mV)	R_{GD}(kΩ)	Xtor	ΔV_{th}(mV)	R_{GD}(kΩ)
1	45.81	1595.5	12	40.81	51056.7
2	40.49	1595.5	13	45.81	1595.5
3	31.43	51056.7	14	27.88	1595.5
4	40.81	51056.7	15	45.81	1595.5
5	45.81	1595.5	16	40.81	51056.7
6	37.11	1595.5	17	13.60	51056.7
7	45.81	1595.5	18	15.27	1595.5
8	40.81	51056.7	19	45.81	1595.5
9	13.60	51056.7	20	27.88	1595.5
10	15.27	1595.5	21	45.81	1595.5
11	31.43	51056.7	22	40.49	1595.5

In the final step, the aged FF is characterized electrically and compared to the not aged version. The proposed method can be easily extended to different topologies.

IV. EXPERIMENTAL RESULTS

All experimental results presented in this paper are obtained through HSPICE simulations using 32nm PTM parameters [23]. Three FF topologies have been investigated: TGFF, shown in Fig. 2, a modified TGFF and a transmission gate master-slave flip-flop (TG-MSFF) [10], shown in Fig. 3 and in Fig. 4, respectively.

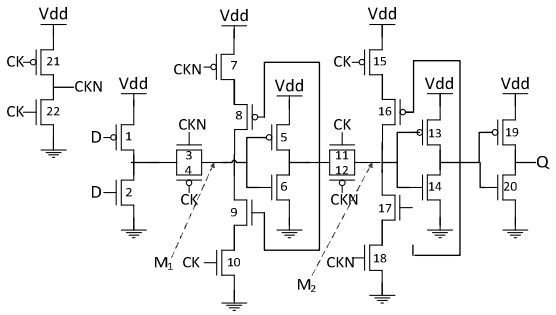

Fig. 3 - Modified transmission gate flip-flop (modified TGFF).

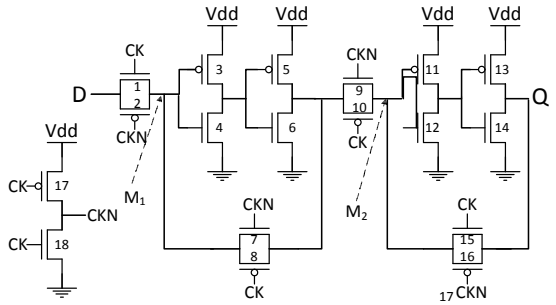

Fig. 4 - Transmission gate master-slave flip-flop (TG-MSFF) [7].

Table III presents $T_{CQ,min}$, $T_{DQ,min}$, *Setup* and *Hold* times with original values (fresh devices) and after transistor aging. Low-to-high (0→1) and high-to-low (1→0) output transitions are considered. The results clearly show the aging impact on FFs, where the delay $T_{DQ,min}$ increases 21% on average.

TABLE III – AGING IN TGFF.

0 → 1	**Setup**	**$T_{CQ,min}$**	**$T_{DQ,min}$**	**Hold**
Original (ps)	16.51	25.94	47.05	-7.11
Aged (ps)	21.51	30.22	56.25	-5.56
Increase	30%	16%	20%	22%
1 → 0				
Original (ps)	28.46	19.60	51.23	-7.34
Aged (ps)	34.69	22.80	62.99	-4.19
Increase (ps)	22%	16%	23%	43%

In order to compare the aging impact on different FF topologies, the delay $T_{DQ,min}$ for a low-to-high transition is taken as example. The results are shown in Fig. 5.After aging degradation, the increment in delay $T_{DQ,min}$ of analyzed

topologies presents different magnitudes. While the degradation causes an increment around 20% in $T_{DQ,min}$ of TGFF and TG-MSFF, the 'Modified TGFF' only experience an increment around 15%. This result increases the importance of the aging analysis in sequential circuits, since the temporal behavior in fresh designs is changed by the aging degradation.

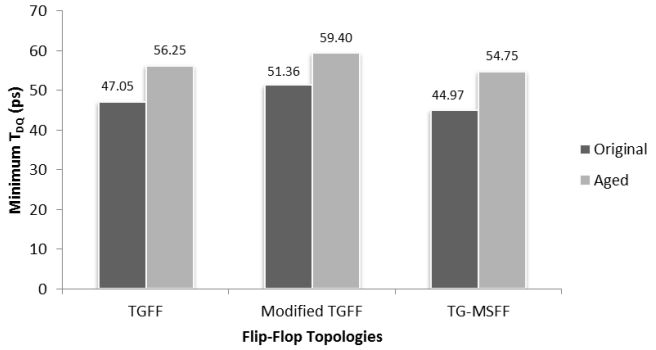

Fig. 5 - Aging of three flip-flop topologies.

V. CONCLUSIONS

In this paper the aging effects in flip-flops are analyzed. The temporal degradation cause by BTI, TDDB and HCI is considered. A model to evaluate aging effects in combinational circuits has been adapted and applied on different flip-flop topologies. We have shown that aging impacts in all the time characteristics of flip-flops. Furthermore, flip-flops topologies are compared and the results show that some ones are much more affected than others.

ACKNOWLEDGEMENTS

Research partially supported by Brazilian funding agencies CAPES, CNPq and FAPERGS, under grant 11/2053-9 (Pronem).

REFERENCES

[1] Paul BC et al. Temporal performance degradation under NBTI: estimation and design for improved reliability of nanoscale circuits. DATE 2006. p. 780–5.

[2] Kaczer B et al. Impact of MOSFET oxide breakdown on digital circuit operation and reliability. IEDM 2000. p. 553–6.

[3] Magnone P et al. Impact of hot carriers on nMOSFET variability in 45 and 65 nm CMOS technologies. IEEE TED 2011;58(8):2347–53.

[4] Quader KN et al. Hot-carrier-reliability design guidelines for CMOS logic circuits. J Solid State Circ 1994;29(3):253–62.

[5] Wang Y et al. Temperature-aware NBTI modeling and the impact of input vector control on performance degradation. DATE 2007. p. 546–51.

[6] Li X et al. Compact modeling of MOSFET wearout mechanisms for circuitreliability simulation. IEEE TDMR 2008;8(8):98–121.

[7] V. Oklobdzija, V. Stojanovic, D. Markovic, and N. Nedovic, Digital System Clocking: High-Performance and Low-Power Aspects. New York: Wiley-IEEE Press, 2003.

[8] N. Nedovic and V. G. Oklobdzija, "Dual-edge triggered storage elements and clocking strategy for low-power systems," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, no. 5, pp. 577–590, May 2005.

[9] M. Alioto, E. Consoli, and G. Palumbo, "Flip-Flop Energy/Performance Versus Clock Slope and Impact on the Clock Network Design," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 6, pp. 1273–1286, Jun. 2010.

[10] K. Ramakrishnan, "Comparative analysis of NBTI effects on low power and high performance flip-flops," in Proc. ICCD, 2008, p. 200.

[11] J. Park and J. Abraham, "An aging-aware flip-flop design based on accurate, run-time failure prediction," in Proc. VLSI Test Symposium (VTS), 2012, p. 294.

[12] V. Rao and H. Mahmoodi, "Analysis of reliability of flip-flops under transistor aging effects in nano-scale CMOS technology," ," in Proc. ICCD, 2011, p. 439.

[13] H. Abrishami and S. Hatami, "NBTI-aware flip-flop characterization and design," in Proc.GLSVLSI'08, 2008, p. 29.

[14] P. F. Butzen, V. Dal Bem, a. I. Reis, and R. P. Ribas, "Design of CMOS logic gates with enhanced robustness against aging degradation," Microelectronics Reliability, vol. 52, no. 9–10, pp. 1822–1826, Sep. 2012.

[15] V. Stojanovic and V. Oklobdzija, "Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems," IEEE Solid-State Circuit, vol. 34, pp. 536–548, Apr. 1999.

[16] L. Kim and R. Dutton, "Metastability of CMOS latch/flip-flop," J. Solid-State Circuits, vol. 25, pp. 942–951, Aug. 1990.

[17] M. Alioto, E. Consoli, and G. Palumbo, "Analysis and Comparison in the Energy-Delay-Area Domain of Nanometer CMOS Flip-Flops: Part I—Methodology and Design Strategies," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 5, pp. 725–736, May 2011.

[18] E. Salman and A. Dasdan, "Exploiting setup–hold-time interdependence in static timing analysis," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 26, no. 6, pp. 1114–1125, 2007.

[19] Bernstein, J. B. et al. Electronic Circuit Reliability Modeling. Microeletron. Reliab. 46 (2006) 1957-1979.

[20] Keane, J. et al. An All-In-One Silicon Odometer for Separately Monitoring HCI, BTI, and TDDB. IEEE JSSC. 45 (2010) 817-829

[21] Wang, W. et al. An efficient method to identify critical gates under circuit aging. ICCAD 2007. 735-740

[22] D. Markovic, B. Nikolic, and R. Brodersen, "Analysis and design of low-energy flip-flops," Proceedings of the 2001 international symposium on Low power electronics and design - ISLPED '01, pp. 52–55, 2001.

[23] Predictive Technology Model. Available: http://ptm.asu.edu/