# Multiple Dynamic Supply Voltage Benchmarks Generator

Marco Terres, Marcelo Johann, Ricardo Reis

*Pgmicro, Universidade Federal do Rio Grande do Sul*
*Av. Bento Gonçalves, 9500, Brazil*
{masmterres, johann, reis}@inf.ufrgs.br

***Abstract* — No public benchmarks for Multiple Dynamic Supply Voltage (MDSV) global routing are available [1], we introduce a tool that modifies benchmarks to be used in our global router. MDSV is a new technique to reduce the dynamic power in Very-Large Scaling Integration (VLSI) circuits. As input this tool uses benchmarks utilized at International Symposium on Physical Design (ISPD'2007) contest and generates as output partitioned benchmarks with voltage islands and four different operation modes. These partitioned benchmarks will be used to evaluate the results of the global router that will be developed under MDSV constraints.**

***Keywords* — Multiple Dynamic Supply Voltage, benchmarks, low power. EDA**

## I. INTRODUCTION

With the process of shrinking of Complemetary Metal-Oxide-Semiconductor (CMOS) technology, most of components and devices are getting smaller and portables. In this circumstance the power consumption began to be an important issue in Very-Large Scaling Integration (VLSI) circuits, mainly in circuits with batteries as energy supply. High power consumption not only leads to short battery life for hand-held devices, but also causes on-chip thermal and reliability problems in general [2].

Studies have shown that power consumption in CMOS circuits consists in two factors. One factor is the charging and discharging of load capacitances, the dynamic power. The other factor is the caused by leakage current through CMOS transistor, the static power [2][3].

For years the principal work to reduce power consumption in academics researches was created techniques to decrease the static power in VLSI circuits.

To handle with these dynamic consumption problems, techniques like Multiple Supply Voltage (MSV) and Multiple Dynamic Supply Voltage (MDSV) were created and new tools needed to be developed. In these tools, the method of make a placement and the routing of the cells demanded a change in algorithms used to solve place and route problems.

The paper is structured in six sections. We show some of our background in Section II, in the Section III we describe the reasons to develop this generator. In Section IV we introduce our methodology and procedure. The results are presented in Section V, conclusions can be seen in the Section VI.

## II. BACKGROUND

Dynamic power has influence of four factors, as we can see in Eq. 1.

$$P_d = \alpha C f V^2 \quad (1)$$

Where C is the load capacitance, V is the supply voltage, f is the frequency and the α is the switching activity. Considering the Eq. 1, dynamic power has a quadratic relationship with supply voltage. Presuming this, techniques used for reduce the power consumption in ways of dynamic power, uses the supply voltage reduction. In this direction, MSV and MDSV were created.

MSV designs were introduced to improve the timing/power consumption trade-off [2]. The main idea behind this technique is reduce the supply voltage of cells, without producing any timing violation in the design. At placement phase you need to group the cells with the same voltage. It is a new factor to be analyzed by the placement algorithms, in addition to reduce congestion, the total wire length and circuit area. There are two ways in to group the cells: row-by-row based and region based [3]. In row-by-row based, the cells with high and low supply voltage are kept in different rows. However, in region based the cells are partitioned in voltage islands. There are numerous researches about these voltage islands generation [2][3].

As MSV designs, MDSV designs use the same technique of supply voltage reduction. The difference is that MDSV designs have various operation modes, like a sleeping and/or a speed mode. These operation modes creates a new factor to be analyzed by global routers algorithms, it is where place level shifters and the signal repeaters, as showed in [1]. The main constraint at placement phase of MDSV design is that the level shifters and the signal repeaters can not be placed inside of shutdown areas, to avoid possible signal problems.

## III. PROBLEM

As in [1], we want use the International Symposium on Physical Design (ISPD'2007) contest benchmarks to evaluate the results of the global router that will be developed under MDSV constraints. Those benchmarks have a large number of nets and grid cells, compared with ISPD'1998 contest benchmarks. Moreover, the routing edges was relaxed with

the addition of obstacles and six routing layers were introduced with explicit vias between them, to better match industry practices [6]. The insertion of vias in the design results in a high penalty to routing costs.

The ISPD'2007 contest utilized 16 benchmarks, those were separated in two sets. The first set consists of a planar routing graph, using the Labyrinth format. The second set is a three-dimensional version of the first set, with additional congestion information [7].

Some difficulties appear since the benchmarks utilized in this contest only have pins locations. Just because this benchmarks were created for global routing and there is no information about the driven cells.

In Fig. 1, we show the structure of the benchmarks utilized at ISPD'2007 contest, where the grid size, number of layers, vertical and horizontal capacity, minimum spacing, via spacing and informations about the tile are specified.

```
grid # # # (x grids, y grids, number of layers)
vertical capacity # # # # # (vertical capacity by default on each layer)
horizontal capacity # # # # #
minimum width # # # # #
minimum spacing # # # # #
via spacing # # # # #
lower_left_x lower_left_y tile_width tile_height

num net #
netname id_# number_of_pins minimum_width
x y layer
x y layer
...
[repeat for the appropriate number of nets]

# capacity adjustments (to model contestion)
column row layer column row layer reduced_capacity_level
[repeat for the number of capacity adjustments]
```

Fig. 1 An example of the benchmarks [6]

For a global router solve the MDSV designs, it need information about the voltage island boundaries and the operation modes. Information like a list of supply voltage used in all of voltage islands in design as the output file of our generator make, Fig. 2.

```
Modo 0

0.8 0   0   0   0.8 1.2 1.2 0.8 1.2 1.2 1.2 1.2 0   0   0   0   0.8
0.8 0.8 1.2 1.2 0.8 0   1.2 1.2 1.2 0.8 0   1.2 0   0   0   1.2 0
0   1.2 1.2 0.8 0.8 0.8 0   1.2 0   0.8 1.2 0.8 0   0.8 1.2 1.2 1.2
0   0   0.8 0   1.2 1.2 0   1.2 0.8 0   0   1.2 0   0.8 0   1.2 0
0   1.2 1.2 0   1.2 0   1.2 0.8 0   1.2 0   0   1.2 0.8 0   0   0.8
0.8 0.8 0.8 0.8 0   0.8 1.2 0.8 0   0.8 1.2 1.2 1.2 1.2 1.2 0   1.2
1.2 0   1.2 1.2 0   1.2 0.8 0   0   1.2 0   0   1.2 0.8 0   0   0.8
1.2 1.2 0.8 1.2 0   0   0.8 0   0.8 0.8 0.8 0.8 0   0   0.8 0   0
1.2 0   0   0   0.8 0   1.2 0.8 1.2 0.8 1.2 0.8 0   0   0.8 0.8 1.2
0.8 0   1.2 0.8 0   0   0.8 0.8 1.2 1.2 1.2 0.8 1.2 1.2 0.8 0.8 0
0   0   0.8 1.2 0.8 0.8 0   0   0.8 0.8 1.2 1.2 0.8 1.2 0   0   1.2
0   0.8 0   0.8 0   1.2 0   0   0   0   0   0   0.8 0.8 0   0   1.2
0   0   0   1.2 1.2 0   0   0.8 1.2 0   1.2 1.2 1.2 0.8 1.2 0   0.8
0   0   1.2 0   1.2 0   1.2 1.2 0   1.2 1.2 1.2 0   0.8 0.8 1.2 0.8
0   0   0.8 1.2 0.8 0.8 0   1.2 0   0   1.2 1.2 0   1.2 0.8 0.8 0
0   1.2 0.8 1.2 1.2 0.8 0.8 1.2 0   0.8 0   0.8 1.2 0   0   0.8 1.2
0   1.2 1.2 1.2 0.8 0   1.2 0.8 0   0.8 1.2 0.8 0.8 0.8 1.2 1.2 0
0   0   1.2 0.8 0   0   0   0   0   1.2 1.2 0   0   1.2 0   0   0
```

Fig. 2 A part of the output file

## IV. PROCEDURE

We used a lexical analyzer with three basic rules: grid, via and net. The lexical files have a structure divided in three sections: definition section, rules section and code section. At code section, we develop the program to analyze and convert ISPD'2007 benchmarks using C++ language.

The program has three functions: initialization, read and partitioning, as can be seen at Fig. 3.

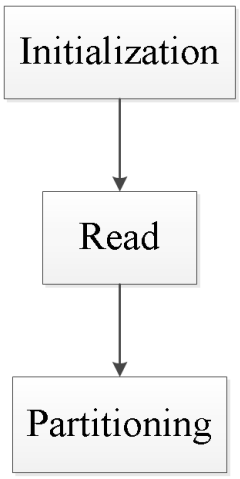


Fig. 3 An overview of the approach

### A. Initialization

In this phase, we create and assign the initial values. Also we pass to our tool the benchmark file to be converted.

### B. Read

In this phase, we use the lexical analyzer to read the benchmark and obtain the information about grid size, tile size, total number of nets and the driver cells pins position.

The tile size multiplied by the grid size give the total size of the cells grid. However, this size is too large and cause some problems with memory allocation. To solve this problem, we only use the grid size to position the cells.

### C. Partitioning

In this phase, we generate the voltage island and create the operation modes. Using the grid size we determined the size of the voltage islands, applying the following equation.

$$S = \sqrt{S_{grid}} \tag{2}$$

Where S is the number and the size of voltage island. $S_{grid}$ is the size of the original grid. By default, we generate four different operation modes, as used Wen-Hao Liu *et al.* The Fig. 2 demonstrated an part of output file, each number indicates the supply voltage of the region. Where the region size is determined by the S, i.e. all regions have square/rectangle shape.

## V. Results

We use our approach to generate the modified benchmark, to run the algorithm we use a setup computer with a Intel® Core™ 2 Quad Q9400 running at 2.66 GHz , 4 GB RAM and using Ubuntu 12.04 64bits as operational system. The Table I presents the results of those benchmarks utilized in ISPD'2007 contest, at #NETS column we numerate the total of nets in the benchmark, at #TIME column we exhibit the time, in seconds, expended by your approach generate the voltage island and the operation modes.

TABLE I
Results of our approach

| Benchmarks | #NETS | #TIME (s) |
|---|---|---|
| Adaptec1.2d | 219794 | 3.947 |
| Adaptec1.3d | 219794 | 3.977 |
| Adaptec2.2d | 260159 | 4.980 |
| Adaptec2.3d | 260159 | 5.021 |
| Adaptec3.2d | 466295 | 10.997 |
| Adaptec3.3d | 466295 | 10.976 |
| Adaptec4.2d | 515304 | 10.961 |
| Adaptec4.3d | 515304 | 10.691 |
| Adaptec5.2d | 867441 | 15.333 |
| Adaptec5.3d | 867441 | 15.080 |
| Newblue1.2d | 331663 | 5.315 |
| Newblue1.3d | 331663 | 5.357 |
| Newblue2.2d | 463213 | 9.516 |
| Newblue2.3d | 463213 | 11.972 |
| Newblue3.2d | 551667 | 17.162 |
| Newblue3.3d | 551667 | 17.499 |

As can observe, each benchmark has a 2d and 3d version. The 2d benchmarks have only two layers, while the 3d benchmarks have six layers. There is no big gap between the timing results of a 2d and 3d benchmark, this observation shows that the program only depends of the number of nets, as can be seen on Fig. 4.

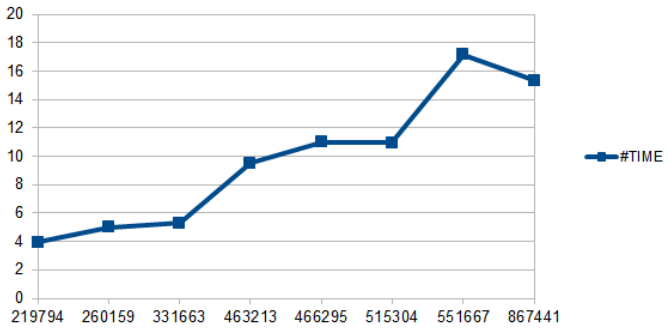


Fig. 4 A graphic #TIME by #NETS of 2d benchmarks

## VI. Conclusions

This work show how important is the power consumption in VLSI designs and demonstrated two techniques used to reduce the dynamic power.

Also we have proposed to create appropriate benchmarks with MDSV informations. These benchmarks will be used to evaluate the results of a further MDSV global router.

## Acknowledgment

The author thanks to CAPES and CNPq for financial support.

## References

[1] Liu, W.-H., Li, Y.-L., & Chao, K.-Y. (2011). "High-quality global routing for multiple dynamic supply voltage designs". *2011 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 263–269. doi:10.1109/ICCAD.2011.6105338.

[2] Wu, H., & Liu, I. (2005). "Post-placement voltage island generation under performance requirement". Computer-Aided Design, …, 309–316. Retrieved from http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1560085.

[3] Ching, R., Young, E., Leung, K., & Chu, C. (2006). "Post-Placement Voltage Island Generation". *2006 IEEE/ACM International Conference on Computer Aided Design*, 641–646. doi:10.1109/ICCAD.2006.320028.

[4] Davoodi, a, & Linderoth, J. T. (2011). "Power-driven global routing for multi-supply voltage domains". *2011 Design, Automation & Test in Europe*, 1–6. doi:10.1109/DATE.2011.5763077.

[5] Igarashi, M., & Usami, K. (1997). "A low-power design method using multiple supply voltages". Low Power …, 36–41. Retrieved from http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=621204.

[6] Moffitt, M., Roy, J., & Markov, I. (2008). The coming of age of (academic) global routing. *Proceedings of the 2008 international symposium on Physical design*, 148. doi:10.1145/1353629.1353662

[7] (2013) The ISPD 2007 Global Routing Contest website. [Online]. Available: http://archive.sigda.org/ispd2007/contest.html

[8] Allani, M., & Agrawal, V. (2012). "An efficient algorithm for dual-voltage design without need for level conversion". *Proceedings of the 2012 44th Southeastern Symposium on System Theory (SSST)*, 51–56. doi:10.1109/SSST.2012.6195150.

[9] *Liu, B., Cai, Y., Zhou, Q., & Hong, X. (2006)*. "Power driven placement with layout aware supply voltage assignment for voltage island generation in dual-vdd designs". *Asia and South Pacific Conference on Design Automation, 2006., 582–587. doi:10.1109/ASPDAC.2006.1594748.*

[10] (2012) flex: The Fast Lexical Analyzer. [Online]. Available: http://flex.sourceforge.net/

[11] (2012) The Lex & Yacc Page. [Online]. Available: http://dinosaur.compilertools.net/