

Study and Development of a Simulation Tool for Optical Lithography

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Abstract— This paper presents a study and the implementation of a optical simulation tool based on wavelets. After this initial study it will be possible to implement resolution enhancement techniques (RET) such as optical proximity correction (OPC) and double patterning. Optical lithography simulation is an essential step to a Design for Manufacturability (DFM) flow. Simulation is used in mask printability enhancement methods. Mask printability is improved by creating a modified mask for which the printed features resemble closely the features on the original mask. However lithography simulation is a compute intense task and a fast simulation is required to allow feasible mask correcting algorithms.

I. INTRODUCTION

Optical lithography is reaching its limits as exposure has reached its own limit at 40nm half-pitch [1]. As the technology advances, the feature size of circuit become smaller even smaller than the light wave-length used to fabricate them. Consequently, the actual drawn features do not match the geometry intended by the designer in the circuit layout.

New lithographic technologies are adopted or under development to alleviate lithography problems. Among them are double and multiple patterning lithography (DPL/MPL), Extreme Ultra-Violet Lithography (EUV), e-beam direct-write (EBDW), directed self-assembly (DSA), among others [2]. Also there is the help from more conventional RET techniques such as OPC.

OPC is one of the methods adopted to reduce the effect of light diffraction. However, the process is time consuming because it requires many iterations of simulations and the results are limited by the original layout quality.

Simulation of optical lithography is used to predict the distortions so that applying RET techniques they can be mitigated or corrected during the project. However lithography simulation is a very compute intensive task. This leads to a quest to develop more efficient methods of optimization in software simulation. Several researches have been made aimed at optimization software, among them are Yu et al. [3] and Rodrigues [4].

This papers presents some basic ideas about optical lithography used to build digital circuits discussing its technical features, limitations and techniques used to overcome such limitations. This paper also shows a tool for lithography sim-

ulation following the implementation presented in the works [4] [5].

The remaining of this paper is divided as follows. Section II presents some related works. Section III explains some fundamentals of optical lithography utilized in the circuit manufacturing. Section IV presents the wavelet optical lithography simulation technique. Section V outlines the simulation tool development. And Section VII draws some conclusion and future works.

II. RELATED WORKS

In this section we present some works in which lithography simulation technique were developed or improved. These works also focus on simulation speedup and present some RET method mainly the optical proximity correction (OPC).

- Cobb [6] performs OPC using a fast aerial image intensity calculation technique derivated from the Hopkins model [7]. Is combines two techniques Sum-Of-Coherent Systems Decomposition and Edge lookup for convolution to achieve higher speedups;
- Yu et al. [3] [8] accelerates their OPC method using intensity based OPC (IB-OPC) in spite of edge placement error (EPE) metric. The authors also simplify the Optical Coherent Approximation (OCA) [9], considering the symmetric properties of lithography systems.
- Rodrigues [4] presents a technique for lithography based on 2D wavelet transform using several new methods to improve the geometry edge detection.

In his thesis, Rodrigues [5] proposes an approximate simulation technique based on the 2D wavelet transform achieving up to 20X speedup enabling fast simulation of large circuits.

The main goal of this work is to show the wavelet method propose by Rodrigues [5] and how it can be used to perform RET.

III. FUNDAMENTALS OF LITHOGRAPHY

Due to the technology scaling the dimensions used to design a circuit became smaller than the wave-length utilized to print them on the wafer. In this way the printed feature does not resemble exactly the intended geometry as can be viewed in Figure 1. Researches have been done in order to utilize

Extreme Ultraviolet Lithography (EUVL) and Electron-Beam Direct-Write (EBDW).

EUVL is very similar to regular lithography, however it uses intense ultraviolet light beams reflected by a set of mirrors. It still have some unsolved issues as the flare effect and the blank defect[2].

EBDW is a promising technology which does not require mask to print features on the wafer. Its most benefitre high-resolution and low costs. However it current implementations sent two rproblems: low ththroughput and hot spots created durind the writing which may cause severe CD (Critical Dimension) distortion [2].

While these technologies are not ready for prime time, lithography limitations are mitigated through resolution enhancement techniques (RET). Figure 1 shows the gap between the wavelength (λ) used in lithography and the feature dimension as the technology advances.

Next some common used RET are presented.

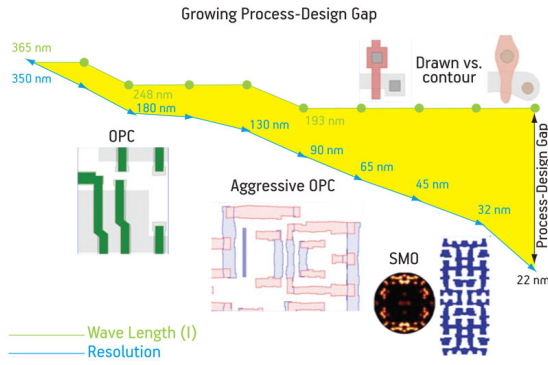


Fig. 1. Gap between the wavelength (λ) and resolution [10]

A. Resolution Limits

Resolution refers to the distinctness of image details, line smoothness and the exact reproduction of the image. Rmin or Critical Dimension (CD) is the minimum half-pitch resolvable by the lithography process.[11]

$$Rmin = K_1 \lambda / NA \quad (1)$$

where λ is an illumination wavelength, NA is a numerical aperture (range of angles by which the system can receiving/emitting light), and k_1 the Rayleigh factor (measures how difficult is the lithography process).

In order to obtain smaller dimensions using optical lithography, one of the following items must be addressed [12]:

- decrease wavelength (λ);
- decrease k_1 ;
- increase numerical aperture (NA).

Although the increasing of NA improve resolution, it worsens the range of defocus (DOF), which is the maximum variation allowed in the focus by the process as it has an inverse square dependency on NA [11]:

$$DOF = \lambda / (2NA^2) \quad (2)$$

B. Resolution Enhancement Technologies (RET)

RET are techniques which modify original masks before they are printed on the wafer aiming to increase the coherence between the intended layout and the actual layout printed. RET utilizes lithography simulation to increase layout resolution.

1) *Optical Proximity Correction*: A well-known and commonly applied RET is Optical Proximity Correction (OPC). OPC adds rectangles at locations where defects may occur as shown in Figure 2. Rectangles are usually added at corners and also where two polygons approach each other.

However, the OPC efficiency also depends on the layout quality itself. A layout with critical paths and critical regions [13] may not be improved via OPC. In fact, OPC can even harm the overall circuit printability.



Fig. 2. Rectangles are usually added at corners [14]

2) *Double Patterning Lithography*: Double patterning lithography (DPL) is another RET. Since 32nm DPL has been seen as a solution to extend dimension shrinking trend, keeping numerical aperture (NA) and the wavelength constant (λ) [1].

For the conventional optical lithography, that is, single patterning lithography, the photoresist layer is exposed only once while for DPL two exposures are necessary. This is accomplished by splitting a single mask into two. By doing so, one can separate dense regions are interleaved in the two layers creating less denser regions.

However DPL creates some difficulties for designers as overlay [15]. Overlay may cause changes in the circuits characteristics like timing, noise and power due to distortion in the layer alignment [15]. DPL has many strategies: litho-etch litho-etch (LELE), litho-freeze, self-aligned double patterning (SADP), dual tone development (DTD), double exposure (DE).

3) *Restricted Design Rule*: Another way to improve printability and hence manufacturability is by using restricted design rules (RDR). RDR are created to avoid critical areas in the circuit design for instance by overestimating the distance between two polygons. Also a common restriction is to allow only straight in the same direction poly lines. Figure 1 presents some RDRs defines and analysed by [14].

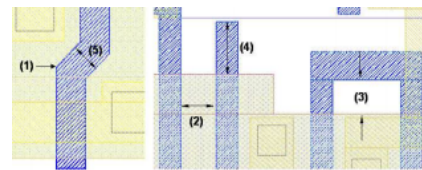


Fig. 3. RDRs defines and analysed by [14]

IV. OPTICAL LITHOGRAPHY SIMULATION USING WAVELET TRANSFORM

Wavelet is a well-known technique in image processing and compression. An example of wavelet is the Mexican hat [5].

The wavelet is used in Equation 3 which is the convolution of the wavelet and the mask. The convolution slides a kernel over the whole image in order to generate a intensity map as seen in Figure 4. The kernel is a 2D matrix and it is created based on sinc^2 function scaled by a .

$$T(x, y, a) = \sum_y \sum_x \psi(x, y, a) * M(x, y) \quad (3)$$

where $T(x,y,a)$ is the transform value at location (x,y) and scale of wavelet a ; the wavelet $\psi(x, y, a)$ is a function of the location and scale; the mask function $M(x,y)$ is a function of the location.

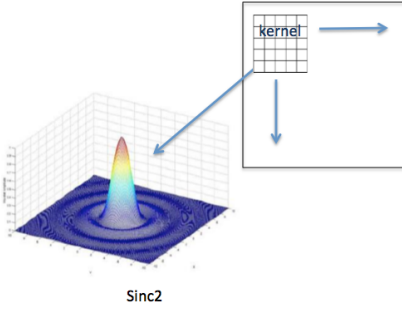


Fig. 4. Convolution process.

The sinc^2 equation was chosen since it matches approximately the pattern generated by the light when reaching the wafer as seen in Figure 5. The pattern is caused due to diffraction of light rays passing through the lens and converging back to focal point of the lens. This effect is called Fraunhofer diffraction.

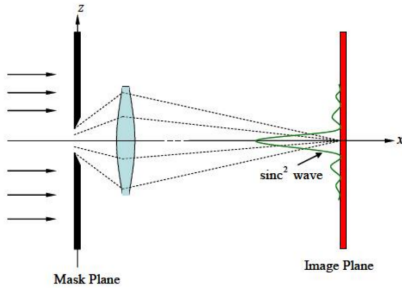


Fig. 5. Fraunhofer diffraction [5]

V. DEVELOPMENT

In this section we discuss some methods created to implement our lithography simulation tool. The tool was developed using Java language.

A. Input

The tool input is a regular text files describing the mask as seen in Figure 6. The first line defines the mask name, the second line stores the mask dimensions and the remaining lines describe mark geometries.

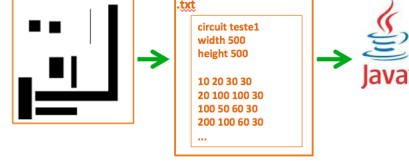


Fig. 6. The tool input is a regular text files describing the mask

B. Convolution

The convolution method slides a kernel over the whole image in order to generate a intensity map as shown in Figure 7. The intensity map provides an estimation of how many light each point of the wafer was expose to. The intensity information is the used to verify if the photoresist in such position was activated. This process is the optical lithography simulation.

Basically the steps to perform the wavelet lithography simulation are

- a kernel with dimension (K) is created based on sinc^2 function scaled by a ;
- the convolution method applies the kernel for every point in the mask;
- the intensity map is created as seen in Figure 7.

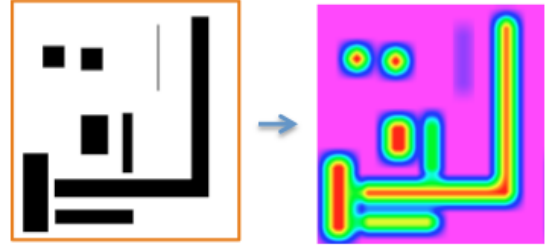


Fig. 7. Intensity map generated by convolution process.

C. EPE

EPE is used as cost measure for OPC. It measures the distance between the intended edge to the printed one as presented in Figure 8.

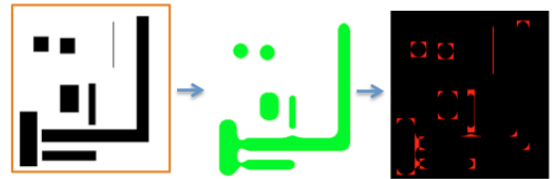


Fig. 8. Designed mask, printed mask and the differences between the two.

D. Edge Detection

To detect edges in our implementation breadth-first search (BFS) was used. BFS looks for edges in a diagonal fashion as shown in Figure 8. The overall edge detection method is as follows

- a list containing points sampled from rectangle edges is created;
- for each point in the list, the nearest edge in the intensity map is searched;

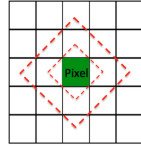


Fig. 9. BFS and the diamond patterns generated around the central point during expansion.

VI. OPTICAL LITHOGRAPHY SIMULATION

Some experiments were executed to test the simulation tool. The main one is to check the intensity map generated as presented in Figure 10.

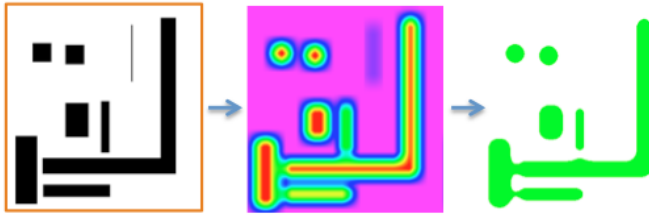


Fig. 10. Intensity map is generated from the original mask and the estimated printed geometries are calculated based on the intensity map.

The edge detection method is presented in Figure 11.

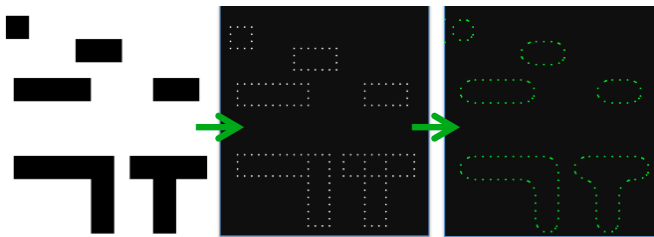


Fig. 11. Edge detection method.

VII. CONCLUSION AND FUTURE WORK

This paper presents some basic ideas about optical lithography used to build digital circuits discussing its technical features, limitations and techniques used to overcome such limitations. This paper also shows a tool for lithography simulation based on the works [4] [5].

As future work we intend to improve the tool runtime. We have made an initial study on OPC using exhaustive search and simulated annealing (SA). We also plan to improve and adapt other techniques RET in our tool.

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