

Analog Acquisition Using Multilevel Statistical Sampling

Adão Souza Jr.^{#1}, Gabriel T. Guimarães*, William Marques[#]

[#]*Curso de Engenharia Elétrica, Instituto Federal Sul-rio-grandense
Pelotas, Brasil*

¹adaojr@pelotas.ifsul.edu.br

Abstract— In this work a systematic approach to the design of over-sampled stochastic ADCs with inherent tolerance to parametric variations is presented. The architecture uses low-cost blocks in order to be highly configurable and almost totally digital, taking benefit from Moore's law. Theoretical analysis results and tradeoffs are discussed, and the approach is validated with a practical implementation.

Keywords— Statistical sampling, analog data acquisition, oversampling converter.

I. INTRODUCTION

A designer of analog to digital converters within mixed-signal systems implemented on CMOS technology must cope with high parametric variations on the electric features of the system elements. This can be a serious issue, since in most architectures ADC accuracy is directly related to the degree of faithfulness of the circuit to its design specifications ([1], [2]).

As one gets to deep-submicron technologies, traditional analog design techniques to increase circuit fidelity to the designed values and self-configurable ADC's become more interesting solutions [2], [3].

Among the desired features such architectures should posses, one can enumerate: (i) use of low-cost, highly variable analog blocks; (ii) to be insensitive to parametric deviations and faults; (ii) to be mainly digital, to follow Moore's law and rely on the strong advantages of digital technologies such as the higher switching speeds and computational power; and (iv) to be flexible enough to provide a wide design space, where resolution, bandwidth, dynamic range and area can be easily adjusted to fit different application needs.

Self-configuration and digital processing have been proposed elsewhere to minimize the cost of analog blocks inside mixed-signal systems, by turning then into modeling problems to be solved in the digital domain [4]. Also, redundancy was combined with self-configuration capabilities to improve the tradeoff between area and resolution for as different class of analog to digital converters [2],[3]. The present paper deals with similar concepts, though the context and the methods employed are rather different.

Traditional stochastic converters presents two main problems: the need for a reference signal with a flat probability distribution (whether uniform noise or a triangular/slope wave) to guarantee acquisition linearity, and very low bandwidth due to the bit-stream digital input. In the present approach, parallel statistical samplers with single and

multi-bit comparator elements are used to override bandwidth limitations, while digital modeling and configuration transfer all linearization issues to the digital domain.

This work is organized as follows: section two reviews the analog data acquisition with one-bit parallel statistical samplers, section three generalizes the results for multi-bit comparators. Issues regarding the linearization model are addressed in section four. Section five compares results using different architectures. Finally considerations are made about the design landscape that emerges and some open issues of research in the sixth and final section.

II. PARALLEL STATISTICAL SAMPLING

Statistical sampling is a process where one can determinate the statistics of a given signal by comparing it to a periodic reference that sweeps the entire signal dynamic range, and which is sampled at random instants within its period [5]. Since the output bit-stream will have a clear relationship to the input, on an over-sampled setup it is possible to estimate the input based on this result.

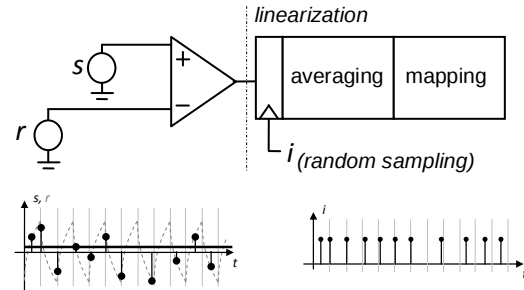


Fig. 1 Statistical sampling setup

In a typical statistical sampling setup (figure 1), reference waveform (r) is compared with the signal of interest (s) using a low cost hard-limiter. Since comparison is a subtraction followed by hard-limiting and assuming the maximum signal frequency (F_s) is much lower than the reference frequency (F_r) the probability of a high level in the output can be estimate applying quantization theory [6].

Once probability distribution of the bit-stream is known, it is possible to estimate the average output. Input values of s can thus be easily calculated from the resulting expression (1), where $E\{\cdot\}$ denotes the expectation operator.

$$\mu(o) = E\{o_+\} - \frac{1}{2} \quad (1)$$

Since the reference is seen by the comparator as the instant values of r at the sampling moments defined by the sequence i , it can be easily shown that if the pseudo-random number generator that determines sampling is uniformly distributed, reference distribution will be equal to the PDF of r .

An uniform PDF implies a linear relationship, which is used in the conventional stochastic acquisition schemes ([7], [8]). Using a reference with any other PDF shape will imply be a non-linear, however well-defined, mapping between $\mu(o)_{t \in T}$ and $s_{t \in T}$, where $\mu(o)$ denotes the average estimator of the output o . Since in mixed-signal systems, digital computational capabilities are often available, knowledge of this relationship may also allow the use of a less costly reference generator block, followed by a digital linearization process.

Resolution is determined by the scattering of the moving average calculated over the output. As this deviation decreases with the square of the number of averages taken $1/\sqrt{N}$, it is possible to exchange resolution and dynamic performance. The exact relationship depends upon reference probability distribution shape.

Traditionally, this is one of the biggest problems with stochastic quantizers, since the number of averages increases exponentially with the demand for resolution. The PSS (Parallel Statistical Sampler) approaches this issue using not one, but several redundant comparators for a single analog reference r [9], [10]. Using a different pseudo-random sampling sequence for each comparator ($i_{1... \beta}$), bit-stream outputs can be made arbitrarily uncorrelated. These outputs can thus be combined to increase the total system resolution. Figure 2 shows how $i_{1... \beta}$ are used to generate several pseudo-random references from a single analog periodic source. Choosing the sampling distribution will also control reference output distribution.

The PSS approach, in order to work properly, needs a self-configuration stage. This stage is used by the system to make the proper adjustments in the linearization model using data from the real implemented circuit. This allows one to determinate the offsets of the multiple comparators (which is essential to permit the use of low cost comparators).

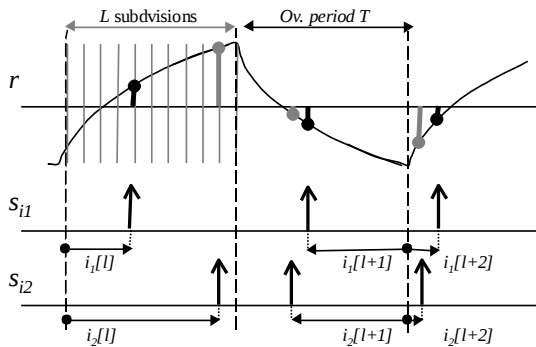


Fig. 2 Generating β uncorrelated references

Once the basic operation of the PSS is well understood and its main advantages are known, one clear question that comes to mind is whether the same approach could be employed using comparator elements with a higher number of bits, and whether there would be any advantage to it.

Figure 3 shows a generalized topology with an arbitrary number β of quantizers, each of them with a number m of different voltage thresholds. The quantizer (CE block) follows a mid-raising characteristic for easy compatibility with the one bit comparator case and is implemented through resistor ladder and m comparators.

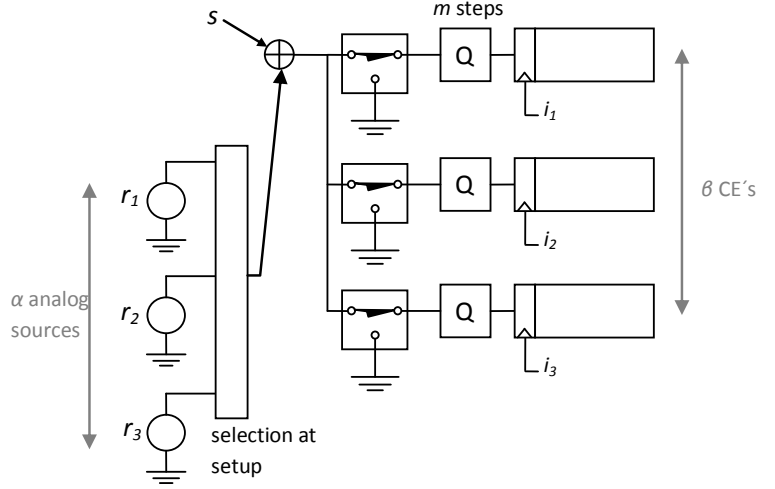


Fig. 3 Generalized Parallel Statistical Sampler -GPSS, architecture. α , β , N , m , τ_{HL} and τ_{HL} are design parameters

Although a single analog reference is required for the circuit to perform an acquisition, due to its low-cost, additional $\alpha-1$ references may be present. This provision increases system tolerance to both parametric and catastrophic faults, as it will be explained in the next section.

For each of comparator output $p_{\beta n}$ ($n=-m/2, \dots, -2, -1, +1, +2, \dots, +m/2$) inside the CE, a probability of a high level $P\{p_{\beta n}\}$ can be calculated. However, in order to estimate the output average of such comparator, one must first determine the probability of each output symbol ($P\{o=n \cdot q\}$) and use (2).

$$\mu(o) = \sum_{n=-m/2}^{+m/2} n \cdot \{P[o \geq n \cdot q] - P[o \geq (n+1) \cdot q]\} \quad (3)$$

Equation (3) shows that the expected output is related to the number of quantization steps and reference probability distribution. Controlling the sampling distribution one can also restrict each of the generated references such as they cover separate sections of the dynamic range.

III. LINEARIZATION AND ANALOG REFERENCES

Assuming our analog reference is modeled by the charge-discharge circuits in figure 2, variations from the designed

values in the charge and discharge constants will change the reference probability distribution and thus the mapping between pulse streams averages and the input. In figures 4 and 5 one can see the impact of a wide variation in these constants in the PDF of r ($P\{r\}$) for a single one-bit sampler.

From the ideal behaviour expected from r , a parametric input-output model can be constructed. Using data from the self-configuration stage to adjust this model one can obtain a good match between with the output from the acquisition, as shown in figure 5b.

Previous work [11] has shown that the mapping approach shows better results at higher acquisition frequencies, although the generator adjustment strategy is rather inexpensive to implement in digital hardware, and provides reasonable results for really low frequency acquisition. Figure 5b shows the linearized outputs using the mapping strategy in the data from figure 5a

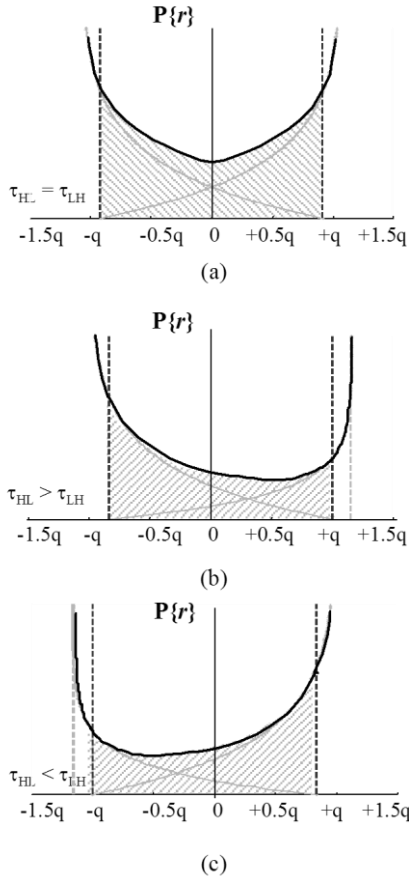


Fig. 4 Reference r PDF variations with generator parameters (τ_{HL} and τ_{LH}).

It can be seen in the plot that the offset of each CE output was not removed yet. However, this must be done before each output is combined. To determinate the offset values in each CE output bit-stream the data input is grounded using the switches and the offset is acquired.

Parameter tracking is an optional procedure extended throughout operation stage. In this operation mode, each one of the active input CE's (the ones with no detected fault) at a time is kept monitoring transitions in the analog reference for any change in parameters. Although not mandatory, this

operation mode together with the use of multiple references may be needed when the system works in an environment prone to severe temperature variations and soft faults due to radiation [10].

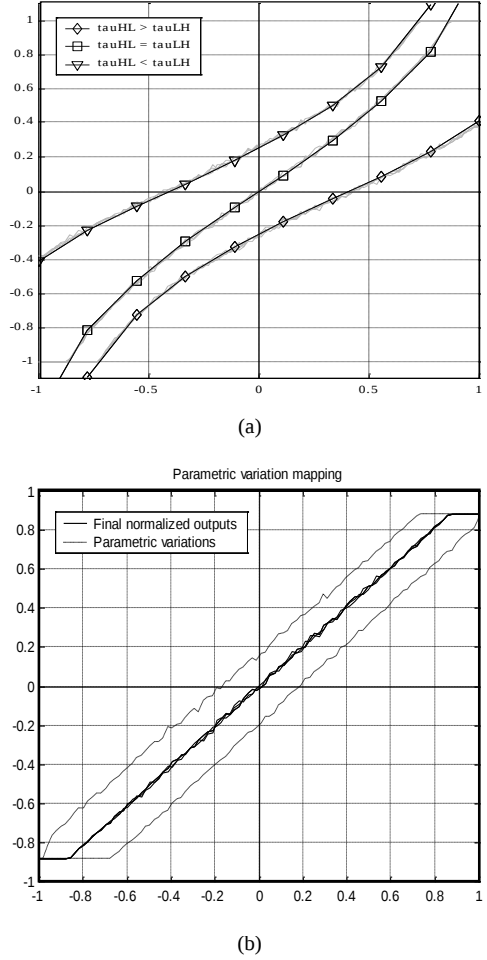


Fig. 5 Matching the linearization model for variations in the generator reference. (b) Linearized output using parametric model of the generator.

Although the generator is a critical element in the circuit, since it is a very simple circuit, one can have redundant units from which one is selected in the configuration stage.

IV. PRACTICAL RESULTS

The first element that has an impact over the output resolution is the generator. Table 1 shows maximum differential non-linearity as a function of the charge-discharge constants.

TABLE 1. RELATIONSHIP BETWEEN DNL AND GENERATOR VARIATION.

Maximum DNL variation with RC parameters (5 bits, 10^5 p-histogram)			
		Values for τ_{LH}	
Values for τ_{HL}	$\tau_{HL}=0.45$	$\tau_{HL}=0.5$	$\tau_{HL}=0.55$
0.45	0.0082	0.0079	0.0077
0.5	0.0080	0.0077	0.0075
0.55	0.0078	0.0076	0.0071

In figure 7a a fixed value for the over-sampling depth and changing the resolution of each single CE was performed, with a variation in the generator parameters: a normalization procedure was employed between the pseudo-random generator and the analog reference

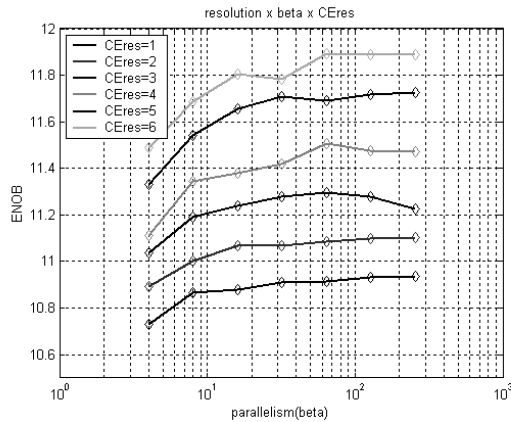


Fig. 6 Features variation with parallelism (β) and CE's resolution: (a) Final ENOB after statistical sampling.

Using a digital prototyping FPGA board a setup with four statistical samplers was assembled. Analog blocks were implemented with discrete comparators and switches. Generator and sampling control was performed by the digital block, while acquisition employed a HP54645D oscilloscope, further tests employed a National Instruments NI Elvis II acquisition board. Using a resistor ladder one could manually select the comparison threshold in each comparator. Combining the digital four outputs one can evaluate the result using a single 2 bits CE with over-sampling. Using an adjusted DC input, acquired data matched the predicted PSS resolution for both situations (4 1-bit CE's PSS and 1 4-bits GPSS).

V. CONCLUSION

In this paper the Generalized Parallel Statistical Sampler was proposed as an approach to the systematic design of stochastic converters. Assuming a formal tool is designed using this architecture as a reference, it would be rather easy for a designer to explore the design landscape by working with just a few parameters. For instance, applications for multiple fault-tolerance may require CE's with a lower resolution, while multi-bit CE's can help applications where the input signal has a higher frequency. Also, as digital modelling allow reference variation a trade-off between analog reference area and parallelism can be established as a function of the technology employed and the allowed degree of redundancy.

Besides that since the circuit is naturally able to self-detect failures and correct non-linearities to a degree future research will experiment using extremely small non-linear pulses as a reference source. A second line of research is to substitute CE

blocks for a composition using gate level elements (e.g. in [3] and [12]) and post-processing techniques. Preliminary tests have shown that it is possible under some conditions to detect and evaluate analog input variations even with totally digital feedback acquisition loops.

Other issues will also be addressed: for design automation of the process it will be important to determinate a good model relating expected feature variation in a given technology and the need for redundancy in the circuit blocks; also this information must be used, together with application characteristics to automatically select the best parameters to adjust the analog acquisition to a given application.

REFERENCES

- [1] Pelgrom, M.J.M., Duinmaijer, A.C.J., and Welbers A.P.G. Matching Properties of MOS transistors, IEEE- Solid State Circuits, vol. 24, pp. 1433-1440, October, 1989.
- [2] Flynn, M.P., and Bogue, I. Using Redundancy to Break the Link Between Accuracy and speed in an ADC. In: Instrumentation and Measurement Technology conference – IMTC2003. pp. 850-853, Vail, USA, May.
- [3] Daly, D. C.; Chandrakasan, A. P. "A 6b 0.2-to-0.9V Highly Digital Flash ADC with Comparator Redundancy" IEEE International Solid-State Circuits Conference, ISSCC. Pp. 554-635, 2008.
- [4] Carro, L.; Negreiros, M.; Jahn, G. P.; Souza Jr, A. A.; Franco, D. "Circuit-Level Considerations for Mixed-Signals Programmable Components". IEEE Design and Test of Computers, 2003
- [5] Souza Jr., A. A.; Carro, L. "An All-Digital ADC for Instrumentation within SOC's". In: V - IFIP VLSI, Germany, 2003.
- [6] Widrow, B. and Kollár, I. "Quantization Noise: Roundoff Error in Digital Computation, Signal Processing, Control, and Communications," Cambridge University Press, Cambridge, UK, 2008. 778 p.
- [7] Wolffenbuttel, R.F., and Kurniawan, W. Stochastic analog-to-digital converter based on the asynchronous sampling of a reference triangle. Instrumentation and Measurement, IEEE Transactions on , v.38, n.1, pp. 10–16, Feb, 1989.
- [8] Vujicic, V.V.; Milovancec, S.S; Pejasevic, M.D.; Pejic, D.V. Zupunski, I.V. "Low Frequency Stochastic True RMS Instrument". IEEE Trans. Inst. Measure., v.48, n.2, April, 1999.
- [9] Souza Jr, A. A.; Carro, L. "Statistical Acquisition for Embedded Instrumentation". In: IEEE Instrumentation and Measurement Technology Conference . IMTC'04, Italy, 2004
- [10] Weaver, S.; Hershberg, B.; Kurahashi, P.; Knierim, D.; Moon, U-K K. "Stochastic Flash Analog-to-Digital Conversion". IEEE Transactions on Circuits and Systems I. vol 57, n.11, pp 2825-2833. November, 2010.
- [11] Souza Jr, A. A.; Carro, L. "Robust Low-Cost Analog Signal Acquisition with Self-test Capabilities." In: The 19th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems - DFT'0, Cannes, 2004.
- [12] Tangel, A. VLSI Implementation of the Threshold Inverter Quantization (TIQ) Technique for CMOS Flash A/D Converter Applications. 1999. 65f. Dissertation (PhD degree), The Pennsylvania State University, Pennsylvania, USA.