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3D IC Design

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Organização Promoção Apoio

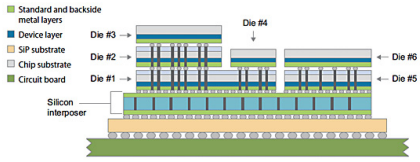
UFRGS CAS SBC IEEE FAPERGS CNPq CEITEC S.A.

Outline

- What is a 3D IC?
- Motivation
- Promises
- Challenges
- Current Technology
  - Process
  - Data Points
  - Examples
- Products
- Market Trends
- CAD Tools
- Research

What is a 3D IC?

- An Integrated Circuit composed of 2 or more layers of active electronics...
- ... stacked on top of each other or mounted side by side (2.5D ICs)



(source: Cadence Design)

- 2.5D ICs are considered by many as 3D Ics – same technologies
- **Key enabler: TSV – Through Silicon Via**

What is a 3D IC?

Related Names:

- 3D SIC – Stacked IC
- SiP, SoP – System in/on Package, from System on Chip (SoC)
- PiP, PoP – Package in/on Package
- SCS - Stacked Chip SoC
- Chip stack MCMs (Multi-Chip Modules)

- This is not Intel's 22nm tri-gate FinFET 3D transistors

Motivation: 1

- **Scaling**: shrinking, packing more electronics in the same space, making them faster, less power, more reliable, with more value
- **Moore's Law**
- **Economics**
- 10B$ foundries
- Need to aggregate value, keep improving...
- **More than Moore**
- Diversification to add value

Microprocessor Transistor Counts 1971-2011 & Moore's Law

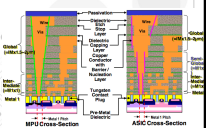
MOS Transistor Scaling
(1974 to present)

S=0.7

[0.5x per 2 Technology Cycles]

Motivation 2:

- Internal (die) – needs more scaling:
  - CI's evolved tremendously as flat surfaces
  - Many metal layers enabled integration
  - Today reaching all limits:
    xtor size, wire delays (GHz), power, yield...
  - The "only" way is to escape vertically

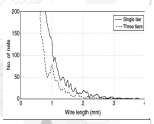


- External (package/PCB) – scaling demands:
  - Dramatic scaling makes dies very far from the PCB
  - Ex: 28nm metal1 pitch compared to a 0.4mmPCB: > 10000 x
  - It translates to huge delay, power, signal integrity problems
  - Performance limitation (memory latency/bandwidth)
- Package/integration must evolve into foundry-like size/processing

Promises of 3D

- Scaling – more componentes/performance in the same area/cost
- System-on-Package – from PCBs to smaller footprints (mobiles)
- Heterogeneous integration – easier analog/digital, diff processes
- Shorter global/average wirelength – homogeneous
- Better timing, bandwidth
- Low power (10-100 times)
- increased yield/integrity (less on PCB)
- Reduced cost with better yield (partitioning)
- Security

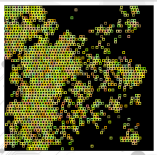
- Ex from Sansumg: 35% smaller, 50% less power, 800% improvement in bandwidth to DRAM



Source: [Davis 2005] IEEE Design & Test special issue on 3D Integration

Challenges

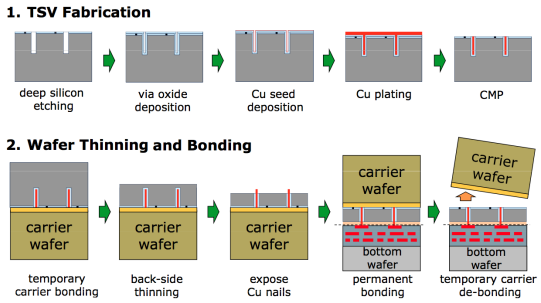
- Yield – many additional steps are needed
- Heat removal – focus of many research works
- **TSV overhead – size, placement, legalization, parasitics, stress**
- Test – depending on the partitioning
- Design Complexity – including CAD complexity
- Lack of standards (new tech) – being addressed
- Heterogeneous technology integration and supply chain (delays)
- Lack of clearly defined ownership (ecosystem/business model)



- **Nevertheless, a revolution happening right now…**

(3-D Chips Grow Up - In 2012, 3-D chips will help extend Moore's Law—and move beyond it. By RACHEL COURTLAND / JANUARY 2012 - http://spectrum.ieee.org/semiconductors/devices/3d-chips-grow-up/0)

Current Technology: Fabrication



Source: Marinissen et al. (IMEC, CascadeMicrotec) IEEE South-West Test Workshop 2011

Current Technology: options

- Face-to-face
- Face-to-back
- Back-to-back

- TSVs of different sizes

- Monolithic
- Chip-on-Chip (or Die-on-Die)
- Chip-on-Wafer (or Die-on-Wafer)
- Wafer-on-Wafer (or on Substrate)
- Ex: TSMC's Co(CoS) and CoW(oS)

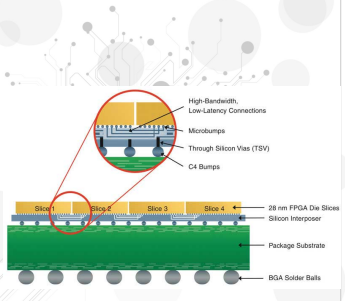
- Integration: gate-level, block-level, heterogeneous

Source: Marinissen et al. (IMEC, CascadeMicrotec) IEEE South-West Test Workshop 2011

Current Technology: Data Points

- BGA - 0.4 a 0.8mm
- C4 bump - 40-250um
- microbump - 5-45um
- TSV - 5-100um
- transistor – 12 to 28nm

(source: Amkor, Yole Development)



(source: Xilinx)

Current Technology: Examples

- Tezzaron
  http://www.tezzaron.com/index.html
- Amkor
  http://www.amkor.com/go/TSV, ThroughSiliconViaTSV3.pdf
- TSMC
  http://www.tsmc.com/english/dedicatedFoundry/services/cowos.htm
- Intel

- JEDEC Solid State Technology Association, formerly known as the Joint Electron Devices Engineering Council (JEDEC) - Standards
  http://www.jedec.org/category/technology-focus-area/3d-ics-0

Products/Designs

- Intel Pentium 4 in two tiers – 2004
- Intel 80-core Teraflop – improved mem communication – 2007

- Many other research designs. Ex:
- The 3D-MAPS Many-Core Processor – 2 tiers F2F – GeorgiaTech
  (2012 - http://arch.ece.gatech.edu/research/3dmaps/3dmaps.html)

- Many SoPs being used on Mobile devices

- Apple A5 is PackageOnPackage
- Apple A6 should use TSMC 3D-IC
- Xilinx Virtex-7 T Family – 6.8B transistor, TSMC 3D-IC, side by side

Market Trends

Main drivers:
- Imaging/Optoelectronics - 20%
- Logic 3D SiP/SoC - 30%
- 3D Wide IO Mem - 15% (important: speed/low power)
- 3d Stacked DRAM - 15%

Other (~5% or less):
- 3D stacked NAND Flash
- MEMS/Sensor
- LED
- RF, Power, Analox, Mixed-Signal

Expected Market:
- 2014 - 2M wafers - 2500 M USD$
- 2017 - 9M wafers

(source: Yole Development)

CAD Tools

- Cadence 3D-IC Solution:
  http://www.cadence.com/solutions/3dic/pages/default.aspx

- Synopsis:
  http://www.synopsys.com/Solutions/EndSolutions/3d-ic-solutions/Pages/default.aspx

- Menthor Graphics:
  http://www.mentor.com/solutions/3d-ic-design/

- Most of these are “aware” of 3D technology, understand it, its libraries, and provide analysis tools
- There is a lot to do for automation, however

Research Opportunities

Fabrication issues:
- Reliability
- Thermal analysis ([T]CAD) / removal

Design/CAD:
- Floorplanning
- Placement
- Routing
- Partitioning
- TSV Legalization
- Architecture exploration (considering physical aspects)

Concluding

- 3D ICs and chip stacking is at its momentum
- You will see a lot of new designs/products using it
- It can keep Moore’s law expectations for the next years

- This is not only for the most advanced billion-dollar process
- Chip stacking is a “replacement” for PCBs, a bridge to advanced scaling

- There is a lot to do...
- There is a lot to learn...
- There is a lot to research on...
- As a breakthrough, it provides opportunities for new people and new companies to jump to the state of the art