

Automatic Design of Micropower Carbon Nanotube Operational Transconductance Amplifiers

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Abstract

This work presents an automatic design procedure for analog integrated blocks composed entirely by Carbon Nanotube Field-Effect Transistors (CNTFETs) as active devices. The proposed design methodology uses a simulation-based optimization engine called UCAF, which was developed initially for the design of CMOS analog blocks. The application for CNTFETs is straightforward and is demonstrated in this paper. Optimization results show that an analog operational transconductance amplifier composed by CNTFETs can achieve even better results in terms of power consumption than the equivalent CMOS version.

1. Introduction

With the evolution of integrated circuits, there is a need to reduce the size of transistors to address the growing demand for equipment with higher speed and lower power consumption. Nowadays, the CMOS integrated circuit technology is dominant over other manufacturing technologies. However, CMOS technology will reach a point where physical conditions will be the limit for the evolution of the manufacturing process of transistors. Thus, it is necessary to constantly search for new materials and technology processes in order to anticipate this limit and provide new alternatives to increase integrated circuits performance, always devising circuits with less power consumption, higher speed and smaller size. However, to achieve faster circuits, it is necessary to design transistors with large capacity to drive current. To this end, a strong replacement candidate for CMOS technology, or additive to this technology, is the carbon nanotube technology, which can be used for the fabrication of transistors with speed 10 to 100 times faster than CMOS technology [1]. However, ever technology replacement generates some paradigm changes, mainly in terms of design methodologies. Well-consolidated CMOS design methodologies must be adapted to new device characteristics or technology constraints.

The ever increasing evolution of technology process for the fabrication of carbon nanotubes and the possibility, in a few years, to the a large scale fabrication of carbon nanotube field-effect transistors (CNTFETs), leads to the necessity of the development of design methodologies which are suitable for the implementation of integrated circuits composed by these devices. In this paper we demonstrate a fully automatic design methodology for operational transconductance amplifiers entirely composed by CNTFETs. We include the new design procedure in the UCAF Framework [2], which was originally developed for analog CMOS design, taking advantage of the modular functions, configurability and optimization algorithms implemented in the tool. The heuristics used to search the high non-linear design space and to find optimized solutions are adequate for the CNTFET design of basic analog integrated blocks. Also, the tool has a friendly user interface, which turns easy the task of inserting new circuit topologies, configuring the optimization procedure and analyzing the results.

2. Carbon Nanotube Field-Effect Transistors

The theory of carbon nanotubes was first described by Ijima [3], and is still in its early stage of development [4][5]. Carbon nanotubes are hollow cylinders composed by one or more concentric layers of carbon atoms similar to a honeycomb lattice. They can be produced from a sheet of graphene rolled up, producing perfect cylinders. Carbon nanotubes are divided into two categories: (i) single-wall nanotubes and (ii) multi-wall nanotubes [3],[7][8], as shown in Fig. 1. This work considers only single-wall nanotubes. Electrical characteristics of a nanotube are defined according to the direction the graphene sheet is rolled up.

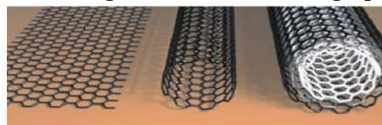


Fig. 1 – Illustration of a sheet of graphene (left), single-wall nanotube (middle) and multi-wall nanotube (right) [9].

We can represent this direction by a chiral vector defined by the following equation:

$$C_h = na_1 + ma_2$$

Here, a_1 and a_2 are unit vectors of the graphene lattice orientation and n and m are integers. According to the direction of the chiral vector, nanotubes receive special denominations: if $n=m$, they are called armchair, while if $m=0$ and $n \neq 0$ they are called zigzag. Otherwise, they are called chiral. The chiral vector also defines if the device will be a conductor (metallic electrical characteristics) or a semiconductor. The diameter D of an ideal nanotube is also dependent on the chiral vector and can be calculated as:

$$D = \frac{a}{\pi} \left(\sqrt{n^2 + m^2 + n.m} \right)$$

where $a=0.246$ nm is the atomic lattice constant. In this work, we use zigzag type nanotubes with $n=19$ and $m=0$, which has semiconducting electrical characteristics and diameter of approximately 1.51nm. The main properties of a carbon nanotube are the high current carrying capacity, high thermal conductivity and reduced charge scattering [6]. This leads to the assumption that they are suitable for the implementation of deep sub-micron devices similar to MOSFETs. So, one of the main promising uses of carbon nanotubes in microelectronics is for the fabrication of CNTFETs.

The structure of a CNTFET is composed by four terminals: gate, drain, source and bulk. The designation of the terminals is identical to a CMOS transistor, due to the fact that both have the same constructive form. The channel region is composed by a carbon nanotube connecting drain to source, as shown in Fig. 2. The source-drain contact materials are typically titanium (Schottky barrier contact) or palladium (quasi-ohmic contact).

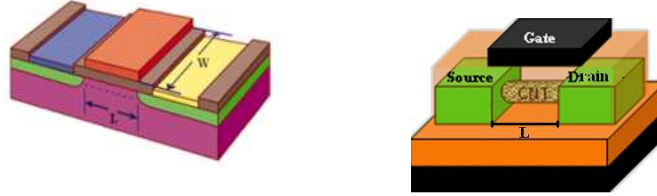


Fig. 2 – Illustration of a CMOS structure (left) and a CNTFET (right).

Analyzing an N-type CNTFET, when a positive potential difference is applied in the gate terminal, there is a current flowing from drain to source if there is a positive potential difference between drain and source. In CNTFETs a quasi-ballistic transport of carriers occurs (due to the carbon nanotube), resulting in a high electric current.

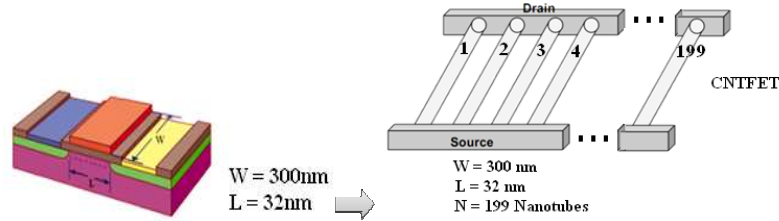


Fig. 3 – Equivalence between CMOS and CNTFET.

The main design issue for the analog designer, when dealing with a carbon nanotube technology, is the sizing of the transistors in order to achieve the desired electrical characteristics. When working with a traditional CMOS technology, the designer of analog integrated circuits in general has the following free variables: W (gate channel width) and L (gate channel length). However, for the CNTFET technology, the diameter of a nanotube is fixed and the channel length is variable. In order to achieve higher currents, it is possible to associate several nanotubes in parallel (N). So, the free variables are L and N . In a CMOS transistor the W can be varied continuously, limited by the resolution of the manufacturing lithography. In the CNTFET technology, the channel width is given by the number of carbon nanotubes that connect the source and drain regions in parallel. Thus, W can be sized only in discrete steps and is given by $W=N.D$, dependent on the number of nanotubes that form the transistor. We can estimate a topological equivalence between both technologies. Taking as basis a CMOS transistor with $W=300$ nm and $L=32$ nm, we can estimate an equivalent CNTFET with the gate composed by a parallel association of 199 nanotubes, each with $D=1.51$ nm and $L=32$ nm, as show in Fig. 3. However, when analyzing the electrical characteristics, this equivalence is lost.

3. The UCAF Tool

The UCAF is a fully configurable simulation-based tool for analog integrated circuit design automation [2]. The general design flow is shown in Fig. 4(a). The tool receives as input design requirements, fabrication

technology parameters and an initial design solution (which can be a previously designed solution or a random initial solution). These information are the inputs for the optimization heuristic algorithm which, based on the free variables bounds, generates an optimized solution for the circuit. As figure of merit, for analyzing the quality of the generated solution, the user must set a cost function, which is calculated based on the specifications obtained by electrical simulations.

UCAF is composed by a user-friendly input/output interface used to insert new circuit topologies, to configure the design procedure and to analyze the evolution of results. This interface is linked to the core of the tool, which contains modular functions implemented in order to automate the design, as shown in Fig. 4 (b). The tool can be used to search for solutions that reach the specification constraints and optimize some specifications, such as power dissipation and gate area, in highly non-linear design spaces. Although UCAF was developed initially for CMOS applications, it is also suitable for the design of CNTFET analog integrated circuits, since the implemented automatic methodology is not dependent on circuit analytical equations.

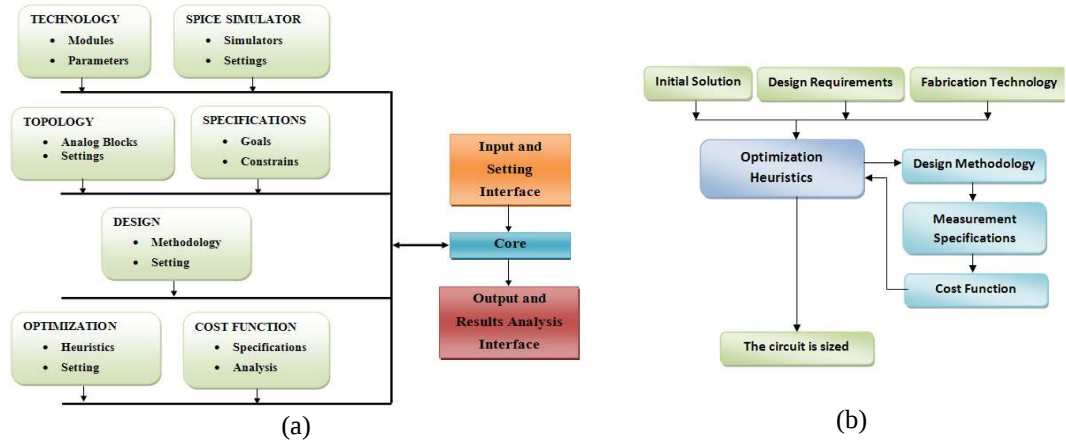


Fig. 4 – (a) Framework block diagram and Analog circuit design automation tool (b).

4. Design of an OTA

As a design example for demonstrating the application of UCAF for automatic design of CNTFET circuits we used a two-stage Miller operational transconductance amplifier (OTA). The schematic of this amplifier is shown in Fig. 5. The Miller OTA is composed by an input differential pair and a current mirror with active load in the first stage. The second stage is composed by an inverter amplifier. Between the first and second stages is connected a compensation capacitor for stability purposes. The main electrical specifications of this circuit are: low frequency gain (A_{v0}), slew rate (SR), phase margin (PM), input common-mode range (ICMR), output swing (OS), power consumption and gate area. We implemented two versions of the Miller OTA: CNTFET and CMOS. Both designs were implemented with UCAF tool and used the same specifications, which are shown in Tab.1. Predictive models for CMOS [10] and CNTFET [9] transistors were used, both for the 32nm technology. Synopsys HSPICE® was the electrical simulator. The Miller amplifier is inserted in the UCAF framework using the user input interface. The tool was configured to explore the design space using Simulated Annealing. In the CMOS version the optimization variables are the W and L of the transistors and in the CNTFET version the variables are N and L . Both designs were generated automatically by UCAF and the results are shown in the third and fourth columns of Tab.1. It is possible to see that most of the design constraints are reached, with the exception of low-voltage gain in the CNTFET version, which is slightly smaller than the desired value. The Tab.2, shows the transistor sizes, sources values and capacitances of the resulting designs.

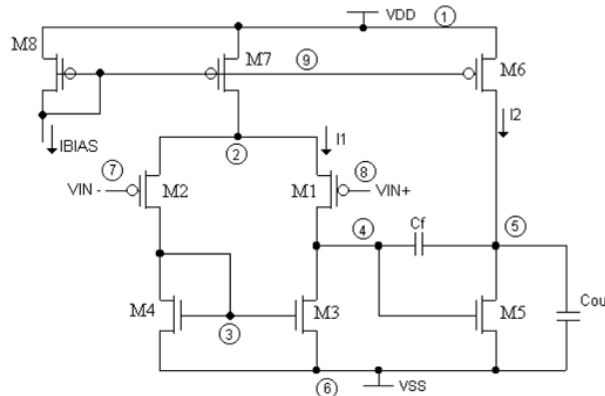


Fig. 5 – Analog Schematics of a two-stage Miller operational transconductance amplifier.

The goal of the optimization provided by UCAF was the minimization of power dissipation. The power dissipation of the CNTFET circuit generated by the tool is about 1.8 times smaller than the equivalent CMOS version.

Tab.1 - Design Results - Specifications

Specification	Design objective	CMOS design	CNTFET design
Slew Rate	$\geq 1\text{V}/\mu\text{s}$	$1\text{V}/\mu\text{s}$	$2.17\text{V}/\mu\text{s}$
ICMR +	$\geq 0.5\text{ V}$	0.6 V	0.88 V
ICMR –	$\leq -0.5\text{ V}$	-0.7 V	-0.80 V
Output Swing+	$\geq 0.8\text{ V}$	0.8 V	0.87 V
Output Swing-	$\leq -0.8\text{ V}$	-0.85 V	-0.87 V
GBW	$\geq 1\text{MHz}$	1.42MHz	5.63 MHz
Gain	$\geq 50\text{ dB}$	60 dB	51.64 dB
Phase Margin	$\geq 60^\circ$	66°	76°
Power Dissipation	Minimize	$43.61\text{ }\mu\text{W}$	$26.31\text{ }\mu\text{W}$

Tab.2 - Design Results – Circuit Parameters

Parameter	CMOS design		CNTFET design	
	W	L	N	L
M1 and M2	$8.38\text{ }\mu\text{m}$	$0.47\text{ }\mu\text{m}$	20000	$0.08\text{ }\mu\text{m}$
M3 and M4	$0.29\text{ }\mu\text{m}$	$0.59\text{ }\mu\text{m}$	413	$4.00\text{ }\mu\text{m}$
M5	$2.15\text{ }\mu\text{m}$	$0.31\text{ }\mu\text{m}$	19333	$0.47\text{ }\mu\text{m}$
M6	$9.99\text{ }\mu\text{m}$	$0.10\text{ }\mu\text{m}$	19333	$0.60\text{ }\mu\text{m}$
M7 and M8	$3.40\text{ }\mu\text{m}$	$0.16\text{ }\mu\text{m}$	1866	$0.25\text{ }\mu\text{m}$
I_{BIAS}	$3\text{ }\mu\text{A}$		$1.81\text{ }\mu\text{A}$	
$V_{\text{DD}}= V_{\text{SS}} $	0.9 V		0.9 V	
C_L	10pF		10pF	
C_F	3pF		3pF	

5. Conclusion

This work described the automatic design procedure of a Miller OTA composed by CNTFETs and the comparison with a CMOS version. The power consumption was optimized, achieving less than $50\text{ }\mu\text{W}$ in both versions. We demonstrated that it is possible to minimize the power consumption in the CNTFET version, taking advantage of the promising electrical characteristics of this type of device. The major contribution of this paper is the direct comparison between both technologies, demonstrating that CNTFET are candidates to compete with the well-established CMOS devices for the implementation of low-power analog circuits when nanotube fabrication challenges will be surpassed, such as yield, mismatch, among others.

6. Referências

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